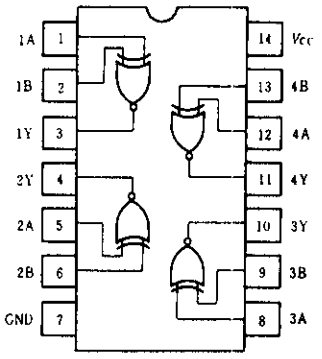
HD74LS266 ●Quadruple 2-input Exclusive-NOR Gates (with open collector outputs)

■PIN ARRANGEMENT



(Top View)

■FUNCTION TABLE

Inputs		Output
A	B	Y
L	L	H
L	H	L
H	L	L
H	H	H

H; high level, L; low level

■RECOMMENDED OPERATING CONDITIONS

Item	Symbol	min	typ	max	Unit
High level output voltage	V_{OH}	—	—	5.5	V
Low level output current	I_{OL}	—	—	8	mA

■ELECTRICAL CHARACTERISTICS (Ta=−20~+75℃)

Item	Symbol	Test Conditions		min	typ*	max	Unit
Input voltage	V_{IH}			2.0	—	—	V
	V_{IL}			—	—	0.8	
Output current	I_{OH}	V_{CC}=4.75V, V_{IH}=2V, V_{IL}=0.8V, V_{OH}=5.5V		—	—	100	μA
Output voltage	V_{OL}	V_{CC}=4.75V, V_{IH}=2V, V_{IL}=0.8V	I_{OL}=4mA	—	—	0.4	V
			I_{OL}=8mA	—	—	0.5	
Input current	I_{IH}	V_{CC}=5.25V, V_I=2.7V		—	—	40	μA
	I_{IL}	V_{CC}=5.25V, V_I=0.4V		—	—	−0.8	mA
	I_I	V_{CC}=5.25V, V_I=7V		—	—	0.2	mA
Supply current	I_{CC}**	V_{CC}=5.25V		—	8	13	mA
Input clamp voltage	V_{IK}	V_{CC}=4.75V, I_{IN}=−18mA		—	—	−1.5	V

* V_{CC}=5V, Ta=25°C

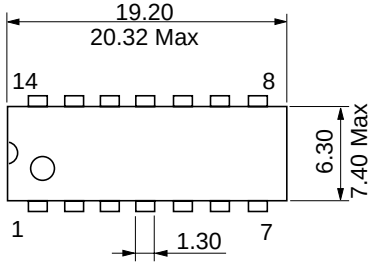
** I_{CC} is measured with one input of each gate at 4.5V, the other inputs grounded, and the outputs open.

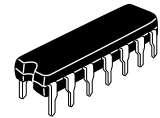
■SWITCHING CHARACTERISTICS (V_{CC}=5V, Ta=25℃)

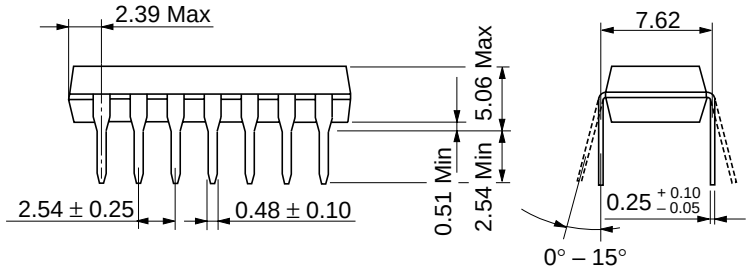
Item	Symbol	Inputs	Test Conditions	min	typ	max	Unit
Propagation delay time	t_{PLH}	A or B	C_L=15pF, R_L=2kΩ	—	18	30	ns
	t_{PHL}			—	18	30	
	t_{PLH}	A or B		—	18	30	
	t_{PHL}			—	18	30	

Note) Refer to Test Circuit and Waveform of the Common Item

Unit: mm

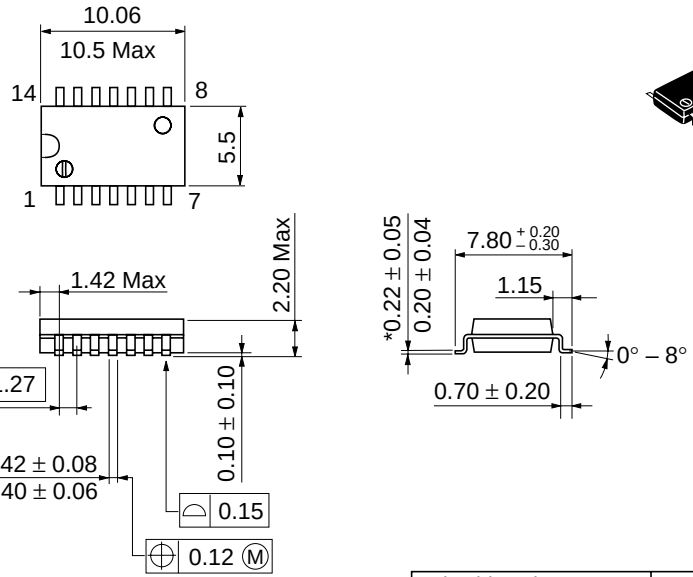


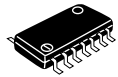




Hitachi Code	DP-14
JEDEC	Conforms
EIAJ	Conforms
Weight (reference value)	0.97 g

Unit: mm

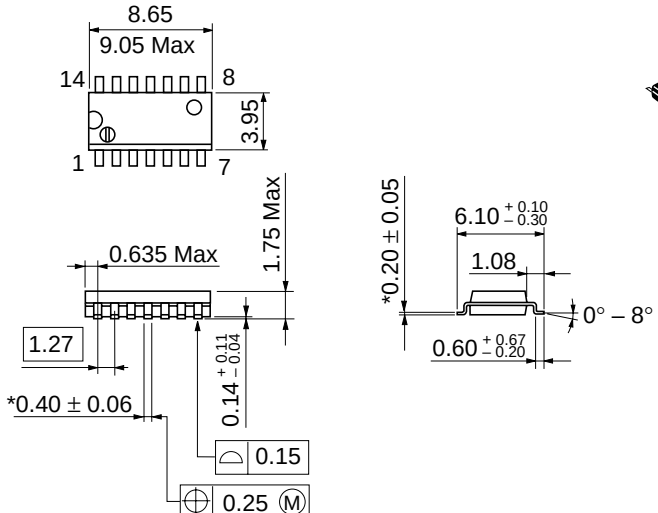




Hitachi Code	FP-14DA
JEDEC	—
EIAJ	Conforms
Weight (reference value)	0.23 g

*Dimension including the plating thickness
Base material dimension

Unit: mm



Hitachi Code	FP-14DN
JEDEC	Conforms
EIAJ	Conforms
Weight (reference value)	0.13 g

*Pd plating

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