DS1221
Nonvolatile Controller x 4 Chip

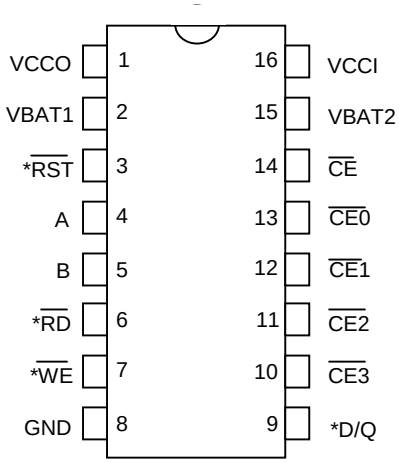
www.dalsemi.com

NOT RECOMMENDED FOR NEW DESIGNS, SEE DS1321 DATASHEET INSTEAD.

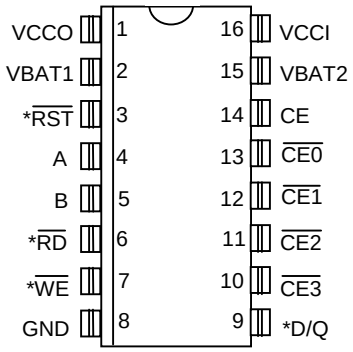
FEATURES

- Converts CMOS RAMs into nonvolatile memories
- Data is automatically protected during power loss
- 2-to-4 decoder provides for up to 4 CMOS RAMs
- Provides for redundant batteries
- Test battery condition on power-up
- Full ±10% operating range
- Unauthorized access can be prevented with optional security feature
- 16-pin 0.3-inch DIP saves PC board space
- Optional 16-pin SOIC surface mount package
- Optional industrial temperature range of -40°C to +85°C available

PIN ASSIGNMENT



DS1221 16-Pin DIP (300-mil)
See Mech. Drawings Section



DS1221 16-Pin SOIC (300-mil)
See Mech. Drawings Section

PIN DESCRIPTION

A, B	- Address Inputs
$\overline{CE}$	- Chip Enable Input
$\overline{CE0}$ - $\overline{CE3}$	- Chip Enable Outputs
V_{BAT1}	- + Battery 1
V_{BAT2}	- + Battery 2
* $\overline{RST}$	- Reset
V_{CCI}	- +5V Supply
V_{CCO}	- RAM Supply
* $\overline{RD}$	- Read Inpu
* $\overline{WE}$	- Write Input
*D/Q	- Data Input/Output

*Used with optional security circuit only and must be connected to ground in all other cases.

DESCRIPTION

The DS1221 Nonvolatile Controller x 4 Chip is a CMOS circuit which solves the application problem of converting CMOS RAMs into nonvolatile memories. Incoming power is monitored for an out-of-tolerance condition. When such a condition is detected, the chip enable outputs are inhibited to accomplish write protection and the battery is switched on to supply RAMs with uninterrupted power. An optional security code prevents unauthorized users from obtaining access to the memory space. The nonvolatile controller/decoder circuitry uses a low-leakage CMOS process which affords precise voltage detection at extremely low battery consumption. By combining the DS1221 with up to four CMOS memories and lithium batteries, nonvolatile operation can be achieved.

CONTROLLER /DECODER OPERATION

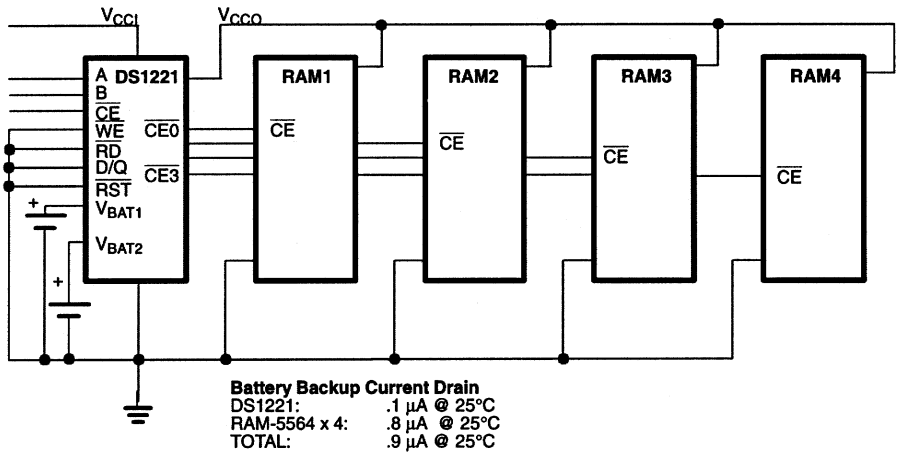
The DS1221 nonvolatile controller performs six circuit functions required to decode and battery-backup a bank of up to four CMOS RAMs. First, a 2-to-4 decoder provides selection of one of four RAMs (see Figure 1). Second, a switch is provided to direct power from the battery or V_{CCI} supply, depending on which is greater, to the V_{CCO} pin. This switch has a voltage drop of less than 0.2V. The third function which the nonvolatile controller provides is power-fail detection. The DS1221 constantly monitors the V_{CCI} supply. When V_{CCI} falls below 4.5 volts, a precision comparator detects the condition and inhibits the RAM chip enables ($\overline{CE0}$ through $\overline{CE3}$). The fourth function of write protection is accomplished by holding all chip enable outputs ($\overline{CE0}$ through $\overline{CE3}$) to within 0.2 volts of V_{CCI} or battery supply. If the Chip Enable Input ($\overline{CE}$) is low at the time power-fail detection occurs, the chip enable outputs are kept in their present state until $\overline{CE}$ is driven high. The delay of write protection until the current memory cycle is completed prevents the corruption of data. Power failure detection occurs in the range of 4.5 to 4.25 volts. During nominal supply conditions the chip enable outputs follow the logic of a 2-to-4 decoder. The fifth function the DS1221 performs is to check battery status to warn of potential data loss. Each time that V_{CCI} power is restored the battery voltage is checked with a precision comparator. If the connected battery voltage is less than 2 volts, the second memory cycle is inhibited. Battery status can, therefore, be determined by performing a read cycle after power-up to any location in memory, verifying that memory location content. A subsequent write cycle can then be executed to the same memory location, altering the data. If the next read cycle fails to verify the written data, the contents of the memories are questionable. The sixth function of the nonvolatile controller provides for battery redundancy. In many applications, data integrity is paramount. In these applications it is often desirable to use two batteries to ensure reliability. The DS1221 provides an internal isolation switch which provides for connection of two batteries. During battery back-up operation the battery with the highest voltage is selected for use. If one battery should fail, the other will automatically take over. The switch between batteries is transparent to the user. A battery status warning will occur if both batteries are less than 2.0 volts. If only one battery is used, the second battery input must be grounded. Figure 2 illustrates the connections required for the DS1221 in a typical application.

NONVOLATILE CONTROLLER/DECODER Figure 1

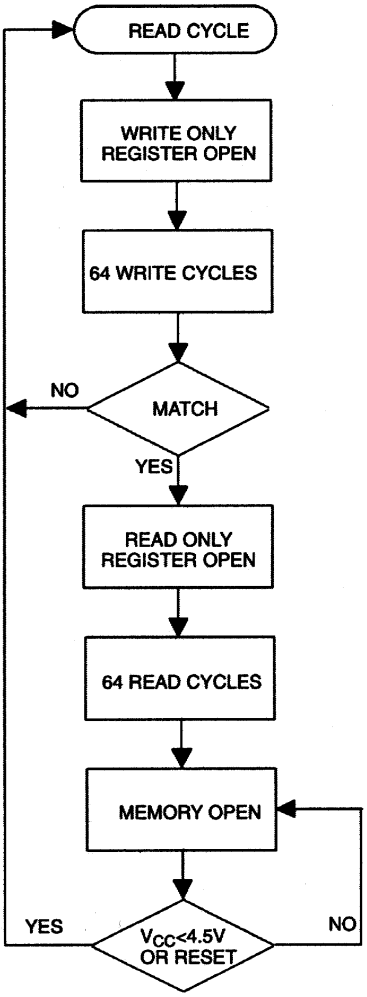
	INPUTS			OUTPUTS			
V_{CCI}	$\overline{CE}$	B	A	$\overline{CE0}$	$\overline{CE1}$	$\overline{CE2}$	$\overline{CE3}$
>=4.5	H	X	X	H	H	H	H
<4.25	X	X	X	H	H	H	H
>=4.5	L	L	L	L	H	H	H
>=4.5	L	L	H	H	L	H	H
>=4.5	L	H	L	H	H	L	H
>=4.5	L	H	H	H	H	H	L

H = High Level
L = Low Level
X = Irrelevant

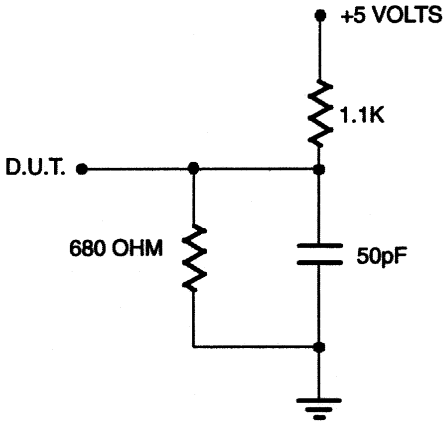
TYPICAL APPLICATION Figure 2



SECURITY SEQUENCE Figure 3



OUTPUT LOAD Figure 4



ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground	-0.3V to +7.0V
Operating Temperature	0°C to 70°C
Storage Temperature	-55°C to +125°C
Soldering Temperature	260°C for 10 seconds
Short Circuit Output Current	20 mA

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS (0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V_{CCI}	4.5	5.0	5.5	V	1
Logic 1 Input	V_{IH}	2.2		V_{CC}+0.3	V	1
Logic 0 Input	V_{IL}	-0.3		+0.8	V	1
Battery Input	V_{BAT1}, V_{BAT2}	2.0		4.0	V	1, 2

DC ELECTRICAL CHARACTERISTICS (0°C to 70°C; V_{CC} = 4.5 to 5.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Current	I_{CCI}			5	mA	3
Supply Voltage	V_{CCO}	V_{CC}-0.2			V	1
Supply Current	I_{CCO1}			80	mA	4, 10
Input Leakage	I_{IL}	-1.0		+1.0	µA	
Output Leakage	I_{LO}	-1.0		+1.0	µA	
$\overline{CE0}$ - $\overline{CE3}$, DQ Output @ 2.4V	I_{OH}	-1.0			mA	5
$\overline{CE0}$ - $\overline{CE3}$, DQ Output @ 0.4V	I_{OL}			4.0	mA	5
V_{CC} Trip Point	V_{CCTP}	4.25	4.37	4.50	V	1

(0°C to 70°C; V_{CC} < 4.25V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
$\overline{CE0}$ - $\overline{CE3}$ Output	V_{OHL}	V_{CC}-0.2 V_{BAT}-0.2			V	
V_{BAT1} or V_{BAT2} Battery Current	I_{BAT}			0.1	µA	3
Battery Backup Current @ V_{CCO} = V_{BAT} - 0.5V	I_{CCO2}			100	µA	6, 7, 10

CAPACITANCE

(t_A = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}			5	pF	
Output Capacitance	C_{OUT}			7	pF	

AC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{CC} = 4.5 to 5.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
$\overline{CE}$ Propagation Delay	t_{PD}	5	15	25	ns	5
$\overline{CE}$ High to Power-Fail	t_{PF}			0	ns	
Address Setup	t_{AS}	20			ns	9

(0°C to 70°C; V_{CC} < 4.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Recovery at Power-Up	t_{REC}	2	5	10	ms	
V_{CC} Slew Rate 4.5 - 4.25V	t_F	300			µs	
V_{CC} Slew Rate 4.25 - 3V	t_{FB}	10			µs	
V_{CC} Slew Rate 4.25 - 4.5V	t_R	0			µs	
$\overline{CE}$ Pulse Width	t_{CE}			1.5	µs	7, 8

NOTES:

1. All voltages are referenced to ground.

2. Only one battery input is required.

3. Measured with V_{CCO} and $\overline{CE0}$ - $\overline{CE3}$ open.

4. I_{CCO1} is the maximum average load which the DS1221 can supply to the memories.

5. Measured with a load as shown in Figure 4.

6. I_{CCO2} is the maximum average load current which the DS1221 can supply to the memories in the battery back-up mode.

7. Chip enable outputs $\overline{CE0}$ - $\overline{CE3}$ can only sustain leakage current in the battery back-up mode.

8. t_{CE} max. must be met to ensure data integrity on power loss.

9. t_{AS} is only required to keep the decoder outputs glitch-free. While CE is low, the outputs ($\overline{CE0}$ - $\overline{CE3}$) will be defined by inputs A and B with a propagation delay of t_{PD} from an A or B input change.

10. For applications where higher currents are required, please see the DS1259 Battery Manager Chip data sheet.

SECURITY OPTION

When activated by Dallas Semiconductor, the security option prevents unauthorized access. A sequence of events must occur to gain access to the memories (Figure 3). First, a dummy read cycle or a 200 ns active low reset pulse is executed to initialize the sequence. Second, a 64-bit access code must be consecutively written to the DS1221 using the write enable signal ($\overline{WE}$), the chip enable signal ($\overline{CE}$), and the data input/output signal (DQ). The code is written to the DS1221 without regard to the address. Actual RAM locations are not written, as the security option is intercepting the data path until access is granted. Instead, a special 64-bit write only register is written. Following the 64 write cycles, the register is compared to a 64-bit pattern uniquely defined by the user and programmed into the DS1221 by Dallas Semiconductor at the time of manufacture. This pattern can only be interrogated by an intelligent controller within the DS1221 and cannot be read by the user. If a read cycle occurs before 64 write cycles are completed, the security sequence is aborted. When a correct match for 64 bits is received, the third part of the security sequence begins by reading a 64-bit read only register. This register consists of 64 bits also defined by the user and programmed into the DS1221 by Dallas Semiconductor at the time of manufacture. For each of the 64 read cycles, 1 bit of the user-defined read only register is driven onto the DQ line. This phase also requires that the 64 read cycles be consecutive. The data being read from the read only register can be used by software to determine if the DS1221 will be permitted to be used with that particular system. After the 64^{th} read cycle has been executed the DS1221 is unlocked and all subsequent memory cycles will be passed through and will become actual memory accesses based upon address inputs. If V_{CC} falls below 4.5 volts or the reset line is driven low, the entire security sequence must be executed again in order to access memory locations.

NOTE:

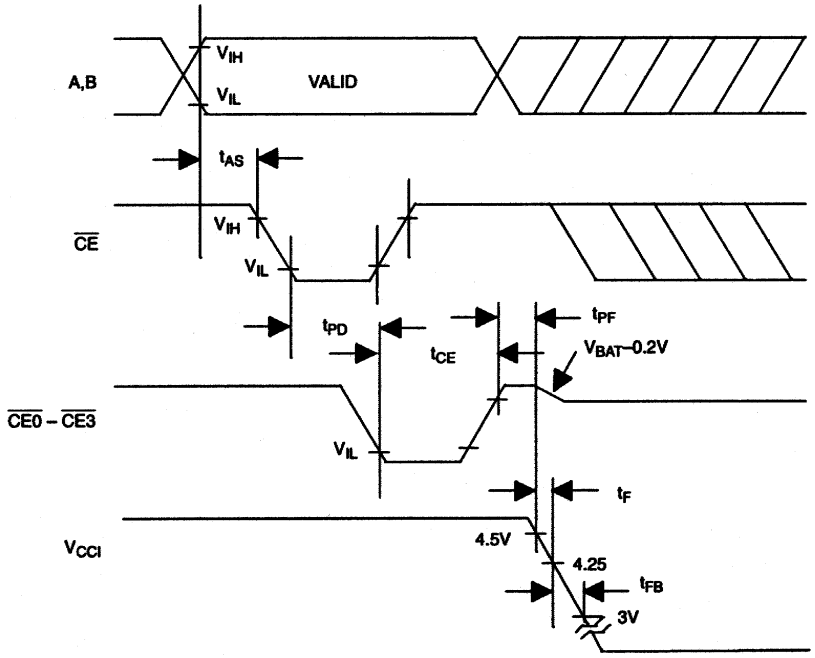
Contact Dallas Semiconductor sales office for code assignments.

SECURITY OPTION
AC ELECTRICAL CHARACTERISTICS

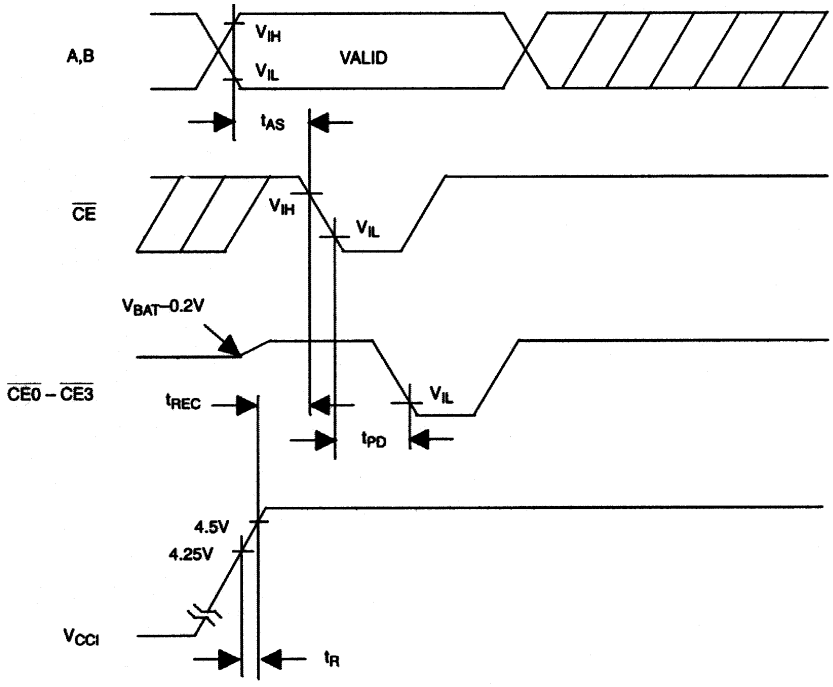
(0°C to 70°C; V_{CC} = 5V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Read Cycle Time	t_{RC}	250			ns	
$\overline{CE}$ Access Time	t_{CO}			200	ns	
$\overline{RD}$ Access Time	t_{OE}			100	ns	
$\overline{CE}$ to Output Low Z	t_{COE}	10			ns	
$\overline{RD}$ to Output Low Z	t_{OEE}	10			ns	
$\overline{CE}$ to Output High Z	t_{OD}			100	ns	
$\overline{RD}$ to Output High Z	t_{ODO}			100	ns	
Read Recovery	t_{RR}	50			ns	
Write Cycle	t_{WC}	250			ns	
Write Pulse Width	t_{WP}	170			ns	
Write Recovery	t_{WR}	50			ns	
Data Setup	t_{DS}	100			ns	
Data Hold Time	t_{DH}	0			ns	
$\overline{CE}$ Pulse Width	t_{CW}	170			ns	
Reset Pulse Width	t_{RST}	200			ns	

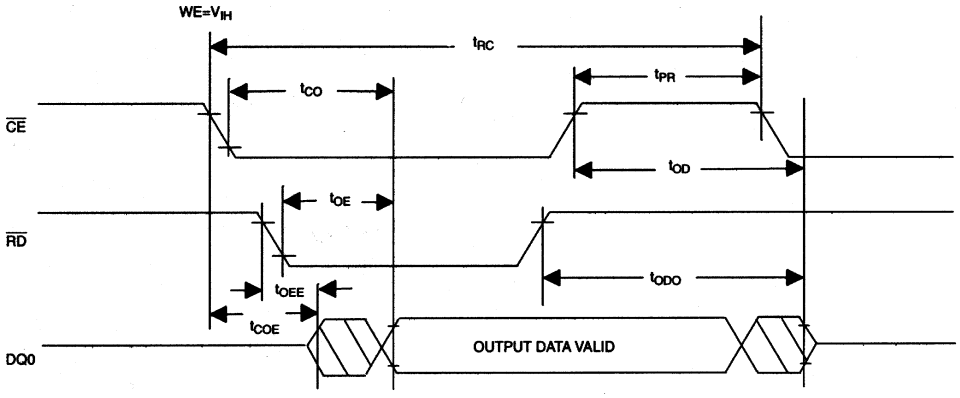
POWER-DOWN Figure 5



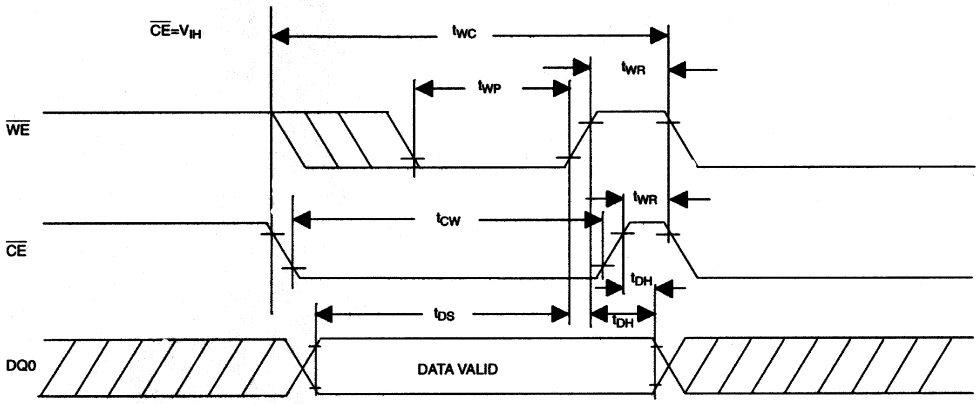
POWER-UP Figure 6



READ CYCLE TO SECURITY OPTION Figure 7



WRITE CYCLE TO SECURITY OPTION Figure 8

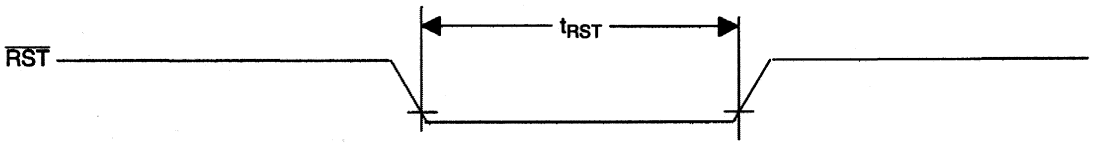


NOTES:

1. t_{DH} and t_{DS} are functions of the first occurring edge of $\overline{WE}$ or $\overline{CE}$.

2. t_{WR} is a function of the latter occurring edge of $\overline{WE}$ or $\overline{CE}$.

RESET FOR SECURITY OPTION Figure 9



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