

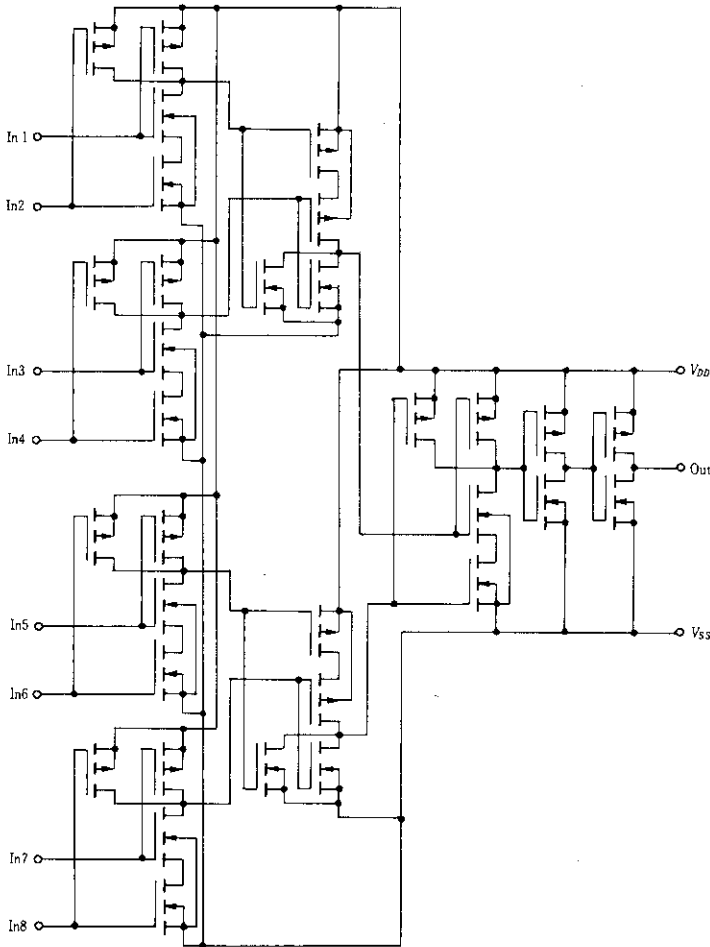
HD14068B

8-input NAND Gate

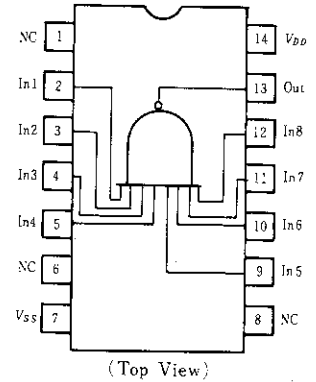
FEATURES

- Quiescent Current = 0.5nA typ/pkg @5V
- Noise Immunity = 45% of V_{DD} typ
- Capable of Driving One Low-power Schottky TTL Load Over the Rated Temperature Range
- Pin-for Pin Replacements for CD4068B and MC14068B Series

CIRCUIT SCHEMATIC



PIN ARRANGEMENT



ELECTRICAL CHARACTERISTICS

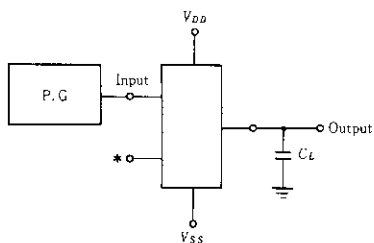
Characteristic	Symbol	Test Conditions	-40°C		25°C			85°C		Unit
			min	max	min	typ	max	min	max	
Output Voltage	V _{OL}	V _{in} = V _{DD}	—	0.05	—	0	0.05	—	0.05	V
		10	—	0.05	—	0	0.05	—	0.05	
		15	—	0.05	—	0	0.05	—	0.05	
	V _{OH}	V _{in} = 0	4.95	—	4.95	5.0	—	4.95	—	V
		10	9.95	—	9.95	10	—	9.95	—	
		15	14.95	—	14.95	15	—	14.95	—	
Input Voltage	V _{IL}	V _{out} = 4.5V	—	1.5	—	2.25	1.5	—	1.5	V
		V _{out} = 9.0V	—	3.0	—	4.50	3.0	—	3.0	
		V _{out} = 13.5V	—	4.0	—	6.75	4.0	—	4.0	
	V _{IH}	V _{out} = 0.5V	3.5	—	3.5	2.75	—	3.5	—	V
		V _{out} = 1.0V	7.0	—	7.0	5.50	—	7.0	—	
		V _{out} = 1.5V	11.0	—	11.0	8.25	—	11.0	—	
Output Drive Current	I _{OH}	V _{OH} = 2.5V	-2.5	—	-2.1	-4.2	—	-1.7	—	mA
		V _{OH} = 4.6V	-0.52	—	-0.44	-0.88	—	-0.36	—	
		V _{OH} = 9.5V	-1.3	—	-1.1	-2.25	—	-0.9	—	
	I _{OL}	V _{OL} = 0.4V	0.52	—	0.44	0.88	—	0.36	—	mA
		V _{OL} = 0.5V	1.3	—	1.1	2.25	—	0.9	—	
		V _{OL} = 1.5V	3.6	—	3.0	8.8	—	2.4	—	
Input Current	I _{in}	15	—	±0.3	—	±0.00001	±0.3	—	±1.0	μA
Input Capacitance	C _{in}	—	—	—	5.0	7.5	—	—	—	pF
Quiescent Current	I _{DD}	Zero Signal, per Package	—	1.0	—	0.0005	1.0	—	7.5	μA
		—	—	2.0	—	0.0010	2.0	—	15.0	
		—	—	4.0	—	0.0015	4.0	—	30.0	
Total Supply Current*	I _T	Dynamic + I _{DD} , C _L = 50pF, f = 1 kHz	—	—	—	0.3	—	—	—	μA
		—	—	—	—	0.6	—	—	—	
		—	—	—	—	0.9	—	—	—	

* To calculate total supply current at frequency other than 1kHz.
 @ V_{DD} = 5.0V I_T = (0.3 μA/kHz) f + I_{DD} @ V_{DD} = 10V I_T = (0.6 μA/kHz) f + I_{DD} @ V_{DD} = 15V I_T = (0.9 μA/kHz) f + I_{DD}

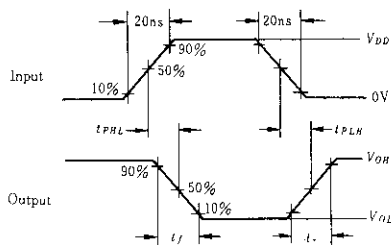
SWITCHING CHARACTERISTICS (C_L = 50pF, T_a = 25°C)

Characteristic	Symbol	V _{DD} (V)	min	typ	max	Unit
Output Rise Time	t _r	5.0	—	100	200	ns
		10	—	50	100	
		15	—	40	80	
Output Fall Time	t _f	5.0	—	100	200	ns
		10	—	50	100	
		15	—	40	80	
Propagation Delay Time	t _{PLH}	5.0	—	200	400	ns
		10	—	80	160	
		15	—	60	120	
	t _{PHL}	5.0	—	200	400	ns
		10	—	80	160	
		15	—	60	120	

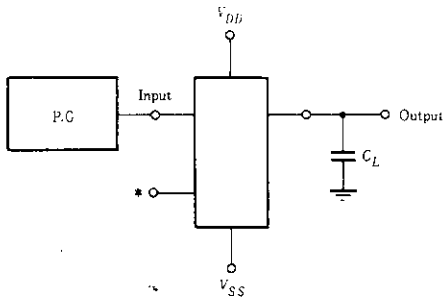
SWITCHING TIME TEST CIRCUIT



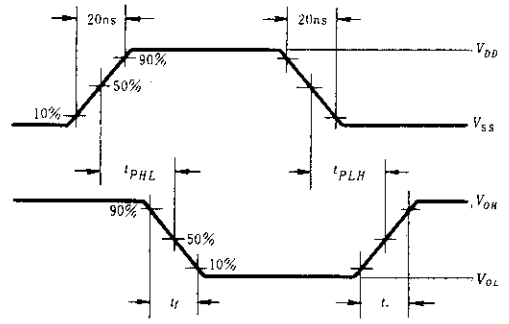
*: All unused inputs of AND, NAND gates must be connected to V_{DD}.

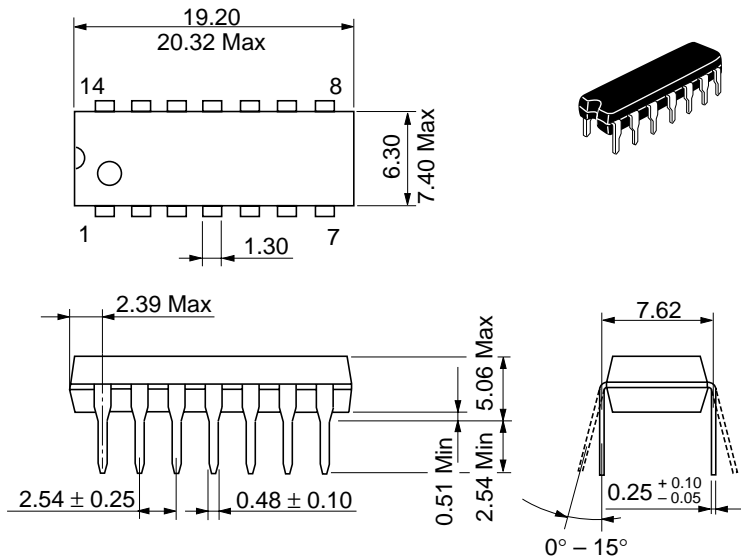


■ SWITCHING TIME TEST CIRCUIT

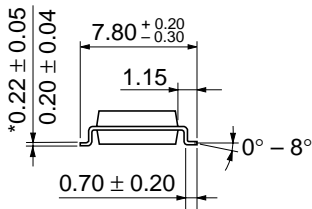
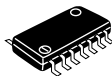
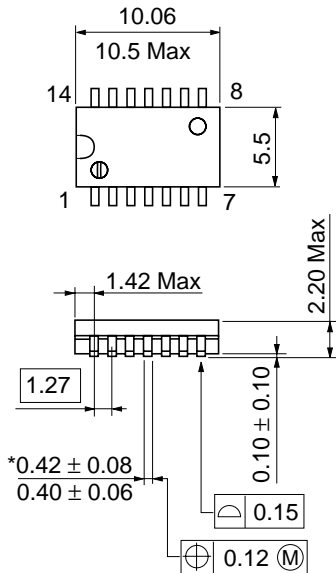


* All unused inputs of AND, NAND gates must be connected to V_{DD} .



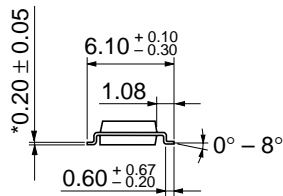
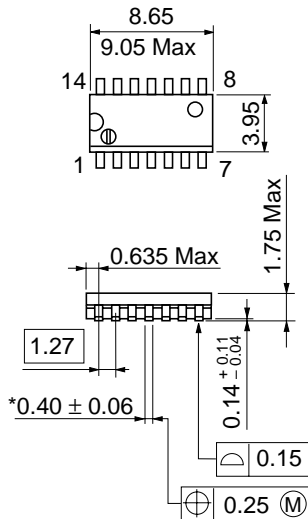


Hitachi Code	DP-14
JEDEC	Conforms
EIAJ	Conforms
Weight (reference value)	0.97 g



Hitachi Code	FP-14DA
JEDEC	—
EIAJ	Conforms
Weight (reference value)	0.23 g

*Dimension including the plating thickness
Base material dimension



Hitachi Code	FP-14DN
JEDEC	Conforms
EIAJ	Conforms
Weight (reference value)	0.13 g

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