

# HD74AC283/HD74ACT283

## 4-bit Binary Full Adder with Fast Carry

# HITACHI

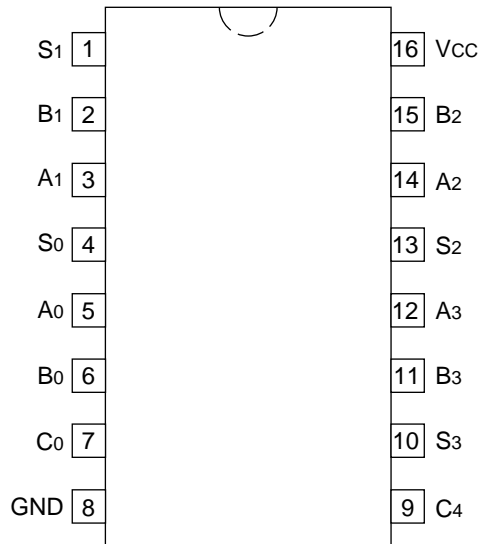
### Description

The HD74AC283/HD74ACT283 high-speed 4-bit binary full adder with internal carry lookahead accepts two 4-bit binary works ( $A_0 - A_3$ ,  $B_0 - B_3$ ) and a Carry input ( $C_0$ ). It generates the binary Sum outputs ( $S_0 - S_3$ ) and the Carry output ( $C_4$ ) from the most significant bit. The HD74AC283/HD74ACT283 will operate with either active High or active Low operands (positive or negative logic).

### Features

- Outputs Source/Sink 24 mA
- HD74ACT283 has TTL-Cmpatible Inputs

### Pin Arrangement



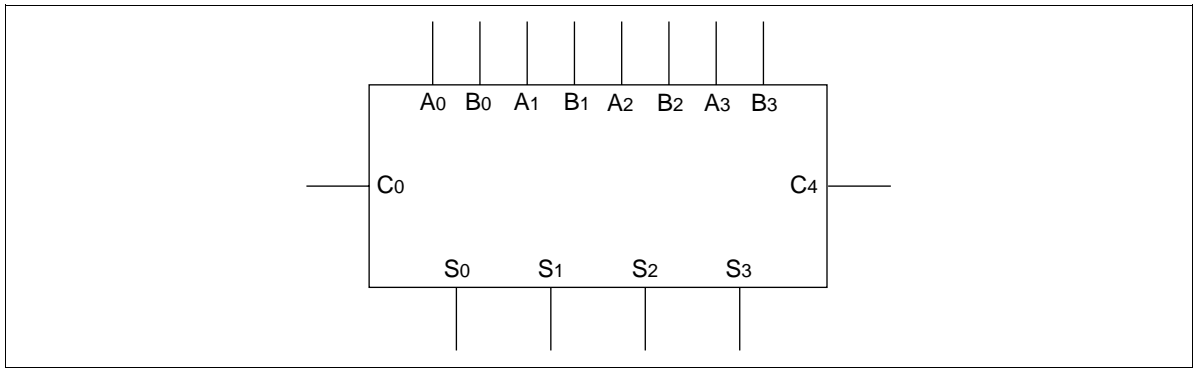
(Top view)

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# HD74AC283/HD74ACT283

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## Logic Symbol



## Pin Names

- A<sub>0</sub> – A<sub>3</sub> A Operand Inputs
- B<sub>0</sub> – B<sub>3</sub> B Operand Inputs
- C<sub>0</sub> Carry Input
- S<sub>0</sub> – S<sub>3</sub> Sum Outputs
- C<sub>4</sub> Carry Output

## Functional Description

The HD74AC283/HD74ACT283 adds two 4-bit binary words (A plus B) plus the incoming Carry (C<sub>0</sub>). The binary sum appears on the Sum (S<sub>0</sub> – S<sub>3</sub>) and outgoing carry (C<sub>4</sub>) outputs. The binary weight of the various inputs and outputs is indicated by the subscript numbers, representing powers of two.

$$2^0 (A_0 + B_0 + C_0) + 2^1 (A_1 + B_1) + 2^2 (A_2 + B_2) + 2^3 (A_3 + B_3) = S_0 + 2S_1 + 4S_2 + 8S_3 + 16C_4$$

Where (+) = plus

Interchanging inputs of equal weight does not affect the operation. Thus C<sub>0</sub>, A<sub>0</sub>, B<sub>0</sub> can be arbitrarily assigned to pins 5, 6 and 7 for DIPS. Due to the symmetry of the binary add function, the HD74AC283/HD74ACT283 can be used either with all inputs and outputs active High (positive logic) or with all inputs and outputs active Low (negative logic). See Figure a. Note that if C<sub>0</sub> is not used it must be tied Low for active High logic or tied High for active Low logic.

Due to pin limitations, the intermediate carries of the HD74AC283/HD74ACT283 are not brought out for use as inputs or outputs. However, other means can be used to effectively insert a carry into, or bring a carry out from, an intermediate stage. Figure b shows how to make a 3-bit adder. Tying the operand inputs of the fourth adder (A<sub>3</sub>, B<sub>3</sub>) Low makes S<sub>3</sub> dependent only on, and equal to, the carry from the third adder. Using somewhat the same principle Figure c shows a way of dividing the HD74AC283/HD74ACT283 into a 2-bit and a 1-bit adder. The third stage adder (A<sub>2</sub>, B<sub>2</sub>, S<sub>2</sub>) is used merely as a means of getting a carry (C<sub>10</sub>) signal into the fourth stage (via A<sub>2</sub> and B<sub>2</sub>) and bringing out the carry from the second stage on S<sub>2</sub>. Note that as long as A<sub>2</sub> and B<sub>2</sub> are the same, whether High or Low, they do not influence S<sub>2</sub>. Similarly, when A<sub>2</sub> and B<sub>2</sub> are the same the carry into the third stage does not influence the carry out of the third

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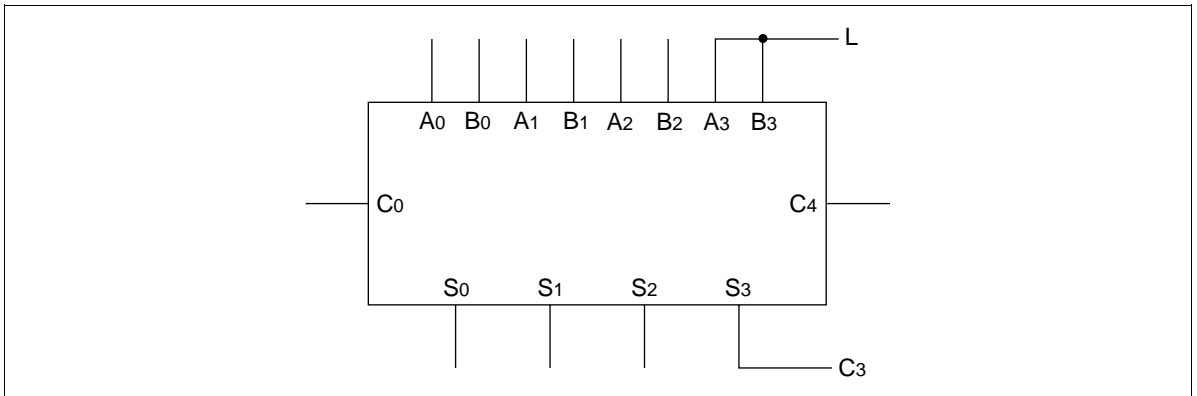
stage. Figure d shows a method of implementing a 5-input encoder, where the inputs are equally weighted. The outputs  $S_0$ ,  $S_1$  and  $S_2$  present a binary number equal to the number of inputs  $I_1 - I_5$  that are true. Figure e shows one method of implementing a 5-input majority gate. When three or more of the inputs  $I_1 - I_5$  are true, the output  $M_5$  is true.

**Fig. a Active HIGH versus Active LOW Interpretation**

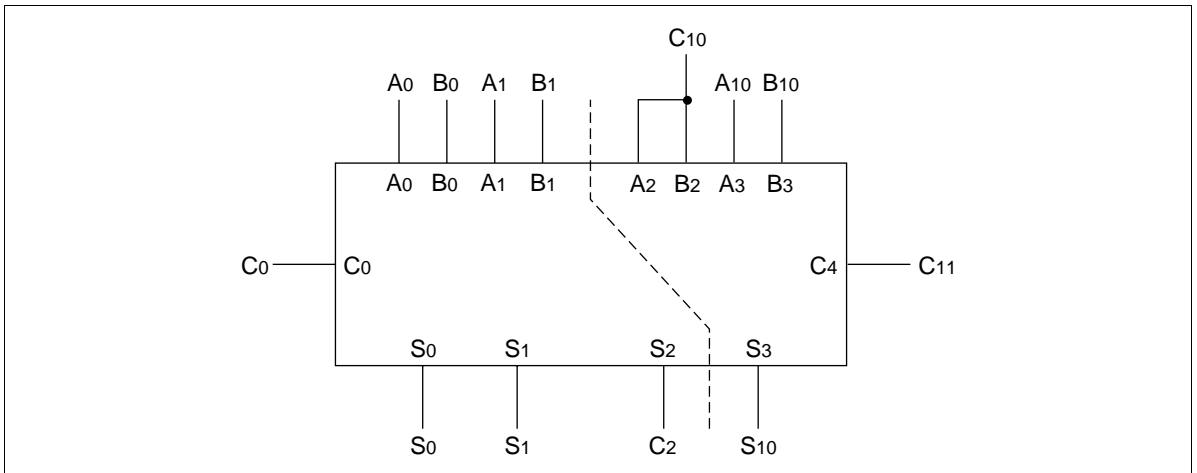
	$C_0$	$A_0$	$A_1$	$A_2$	$A_3$	$B_0$	$B_1$	$B_2$	$B_3$	$S_0$	$S_1$	$S_2$	$S_3$	$C_4$
Logic levels	L	L	H	L	H	H	L	L	H	H	H	L	L	H
Active HIGH	0	0	1	0	1	1	0	0	1	1	1	0	0	1
Active LOW	1	1	0	1	0	0	1	1	0	0	0	1	1	0

Active HIGH:  $0 + 10 + 9 = 3 + 16$

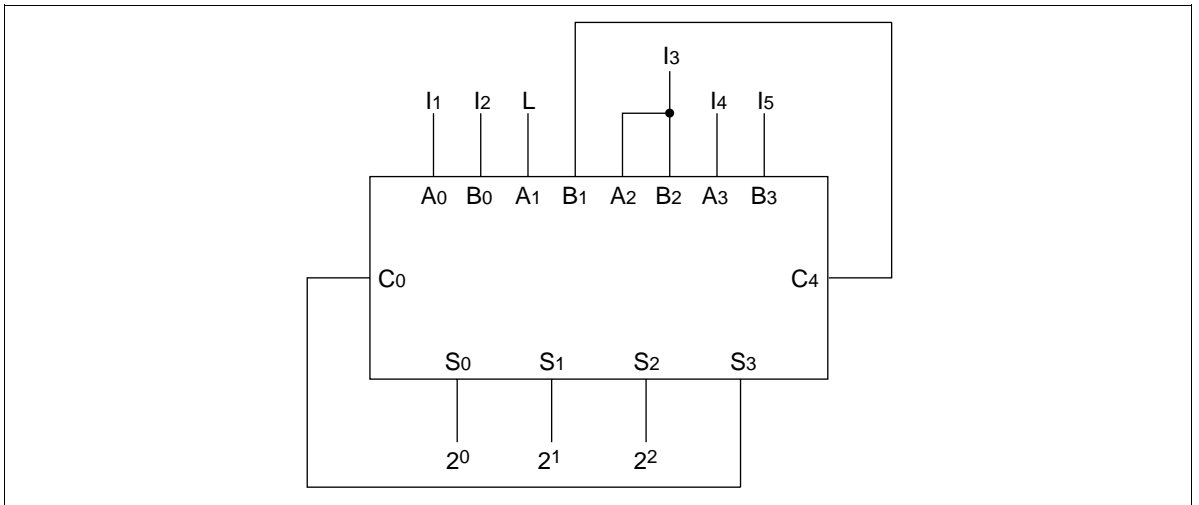
Active LOW:  $1 + 5 + 6 = 12 + 0$



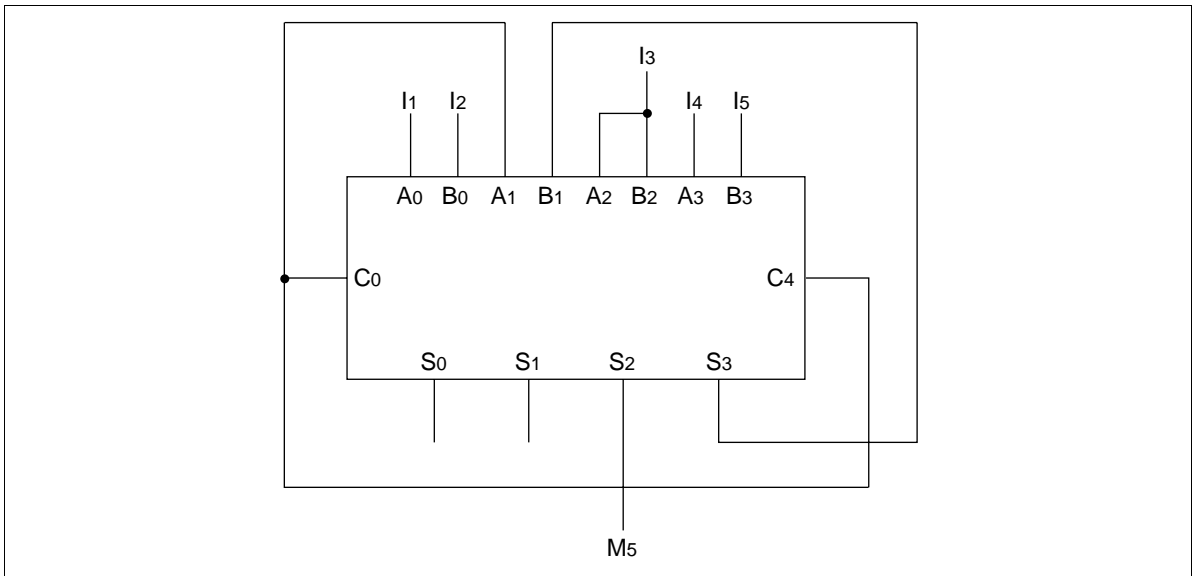
**Fig. b 3-bit Adder**



**Fig. c 2-bit and 1-bit adders**

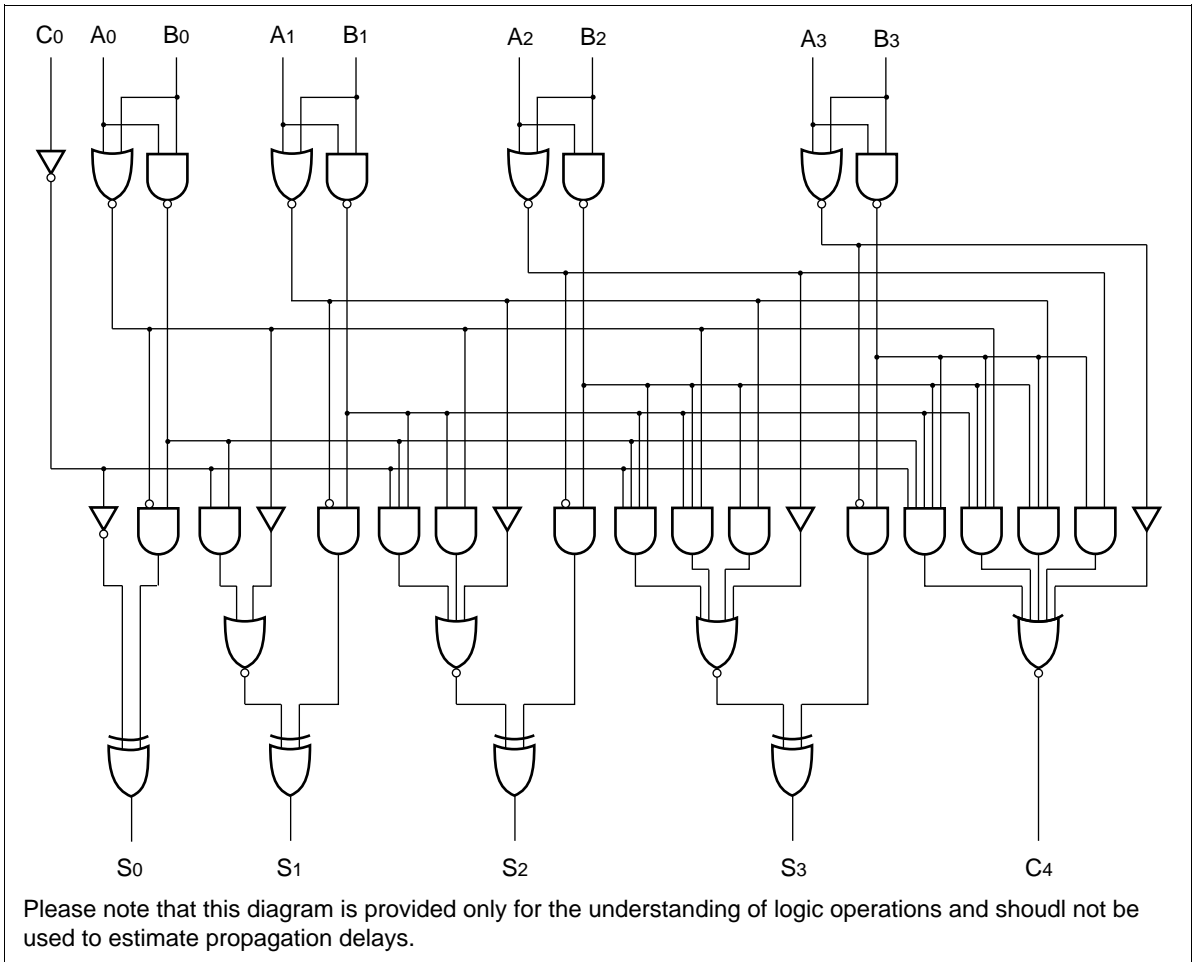


**Fig. d 5-Input Encoder**



**Fig. e 5-Input Majority Gate**

Logic Diagram



DC Characteristics (unless otherwise specified)

Item	Symbol	Max	Unit	Condition
Maximum quiescent supply current	$I_{CC}$	80	$\mu A$	$V_{IN} = V_{CC}$ or ground, $V_{CC} = 5.5 V$ , $T_a = \text{Worst case}$
Maximum quiescent supply current	$I_{CC}$	8.0	$\mu A$	$V_{IN} = V_{CC}$ or ground, $V_{CC} = 5.5 V$ , $T_a = 25^\circ C$
Maximum $I_{CC}/\text{input}$ (HD74ACT283)	$I_{CCT}$	1.5	mA	$V_{IN} = V_{CC} - 2.1 V$ , $V_{CC} = 5.5 V$ , $T_a = \text{Worst case}$

# HD74AC283/HD74ACT283

## AC Characteristics: HD74AC283

Item	Symbol	V <sub>cc</sub> (V)* <sup>1</sup>	Ta = +25°C C <sub>L</sub> = 50 pF			Ta = -40°C to +85°C C <sub>L</sub> = 50 pF		Unit
			Min	Typ	Max	Min	Max	
Propagation delay	t <sub>PLH</sub>	3.3	1.0	11.5	15.0	1.0	16.5	ns
C <sub>0</sub> to S <sub>n</sub>		5.0	1.0	9.5	11.5	1.0	12.5	
Propagation delay	t <sub>PHL</sub>	3.3	1.0	10.5	14.0	1.0	15.5	ns
C <sub>0</sub> to S <sub>n</sub>		5.0	1.0	8.5	10.5	1.0	11.5	
Propagation delay	t <sub>PLH</sub>	3.3	1.0	14.0	17.0	1.0	18.5	ns
A <sub>n</sub> or B <sub>n</sub> to S <sub>n</sub>		5.0	1.0	11.5	13.5	1.0	14.5	
Propagation delay	t <sub>PHL</sub>	3.3	1.0	13.5	16.5	1.0	18.0	ns
A <sub>n</sub> or B <sub>n</sub> to S <sub>n</sub>		5.0	1.0	11.0	13.0	1.0	14.0	
Propagation delay	t <sub>PLH</sub>	3.3	1.0	9.5	12.5	1.0	15.5	ns
C <sub>0</sub> to C <sub>4</sub>		5.0	1.0	7.5	9.5	1.0	10.5	
Propagation delay	t <sub>PHL</sub>	3.3	1.0	10.0	13.0	1.0	14.0	ns
C <sub>0</sub> to C <sub>4</sub>		5.0	1.0	8.0	10.0	1.0	11.0	
Propagation delay	t <sub>PLH</sub>	3.3	1.0	11.5	14.5	1.0	16.0	ns
A <sub>n</sub> or B <sub>n</sub> to C <sub>4</sub>		5.0	1.0	9.5	11.5	1.0	12.5	
Propagation delay	t <sub>PHL</sub>	3.3	1.0	12.0	15.0	1.0	16.5	ns
A <sub>n</sub> or B <sub>n</sub> to C <sub>4</sub>		5.0	1.0	10.0	12.0	1.0	13.0	

Note: 1. Voltage Range 3.3 is 3.3 V ± 0.3 V  
Voltage Range 5.0 is 5.0 V ± 0.5 V

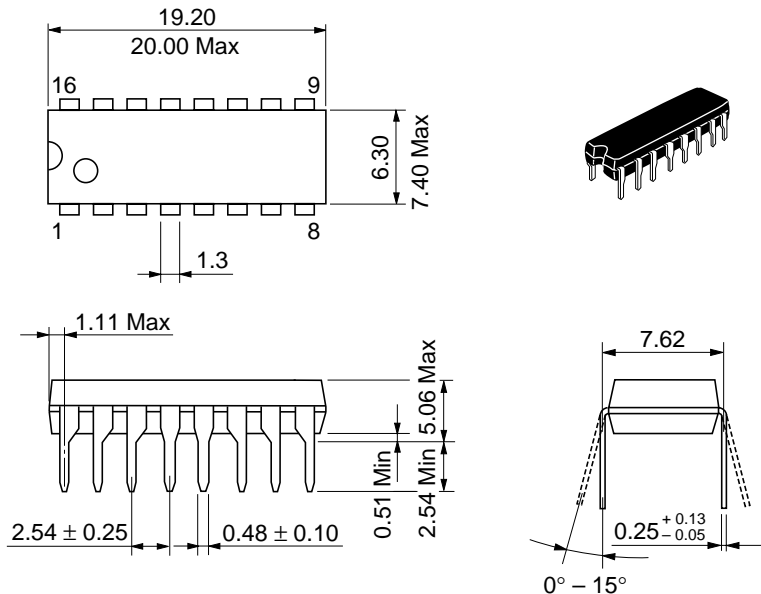
**AC Characteristics: HD74ACT283**

Item	Symbol	V <sub>CC</sub> (V)* <sup>1</sup>	Ta = +25°C C <sub>L</sub> = 50 pF			Ta = -40°C to +85°C C <sub>L</sub> = 50 pF		Unit
			Min	Typ	Max	Min	Max	
Propagation delay C <sub>0</sub> to S <sub>n</sub>	t <sub>PLH</sub>	5.0	1.0	11.5	13.5	1.0	14.5	ns
Propagation delay C <sub>0</sub> to S <sub>n</sub>	t <sub>PHL</sub>	5.0	1.0	10.0	12.0	1.0	13.0	ns
Propagation delay A <sub>n</sub> or B <sub>n</sub> to S <sub>n</sub>	t <sub>PLH</sub>	5.0	1.0	13.0	15.0	1.0	16.5	ns
Propagation delay A <sub>n</sub> or B <sub>n</sub> to S <sub>n</sub>	t <sub>PHL</sub>	5.0	1.0	12.0	14.0	1.0	15.5	ns
Propagation delay C <sub>0</sub> to C <sub>4</sub>	t <sub>PLH</sub>	5.0	1.0	9.0	11.0	1.0	12.0	ns
Propagation delay C <sub>0</sub> to C <sub>4</sub>	t <sub>PHL</sub>	5.0	1.0	10.0	12.0	1.0	13.0	ns
Propagation delay A <sub>n</sub> or B <sub>n</sub> to C <sub>4</sub>	t <sub>PLH</sub>	5.0	1.0	11.0	13.0	1.0	14.0	ns
Propagation delay A <sub>n</sub> or B <sub>n</sub> to C <sub>4</sub>	t <sub>PHL</sub>	5.0	1.0	11.5	13.5	1.0	14.5	ns

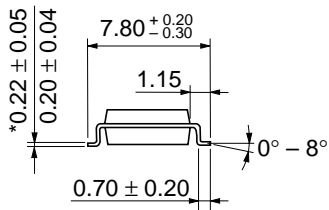
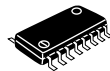
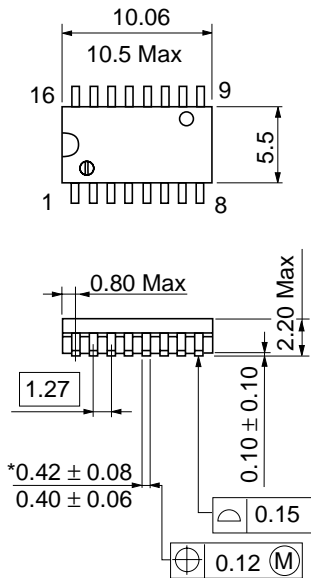
Note: 1. Voltage Range 5.0 is 5.0 V ± 0.5 V

**Capacitance**

Item	Symbol	Typ	Unit	Condition
Input capacitance	C <sub>IN</sub>	4.5	pF	V <sub>CC</sub> = 5.5 V
Power dissipation capacitance	C <sub>PD</sub>	60.0	pF	V <sub>CC</sub> = 5.0 V

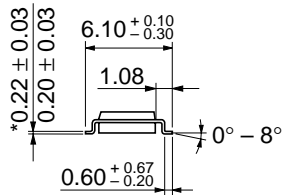
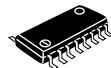
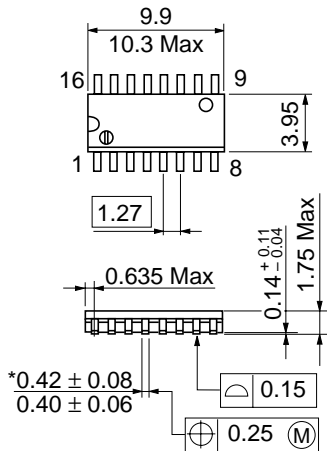


Hitachi Code	DP-16
JEDEC	Conforms
EIAJ	Conforms
Weight (reference value)	1.07 g



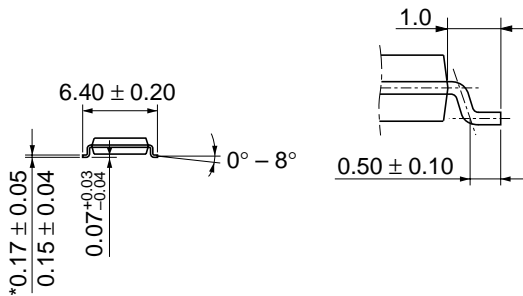
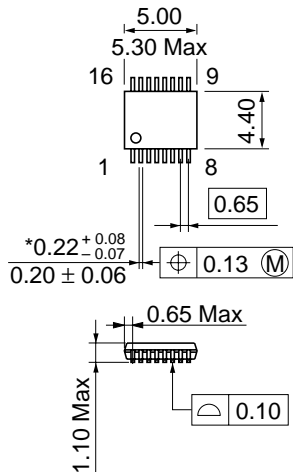
\*Dimension including the plating thickness  
Base material dimension

Hitachi Code	FP-16DA
JEDEC	—
EIAJ	Conforms
Weight (reference value)	0.24 g



\*Dimension including the plating thickness  
 Base material dimension

Hitachi Code	FP-16DN
JEDEC	Conforms
EIAJ	Conforms
Weight (reference value)	0.15 g



\*Dimension including the plating thickness  
 Base material dimension

Hitachi Code	TTP-16DA
JEDEC	—
EIAJ	—
Weight (reference value)	0.05 g

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