

Am25S10

Four-Bit Shifter with Three-State Outputs

DISTINCTIVE CHARACTERISTICS

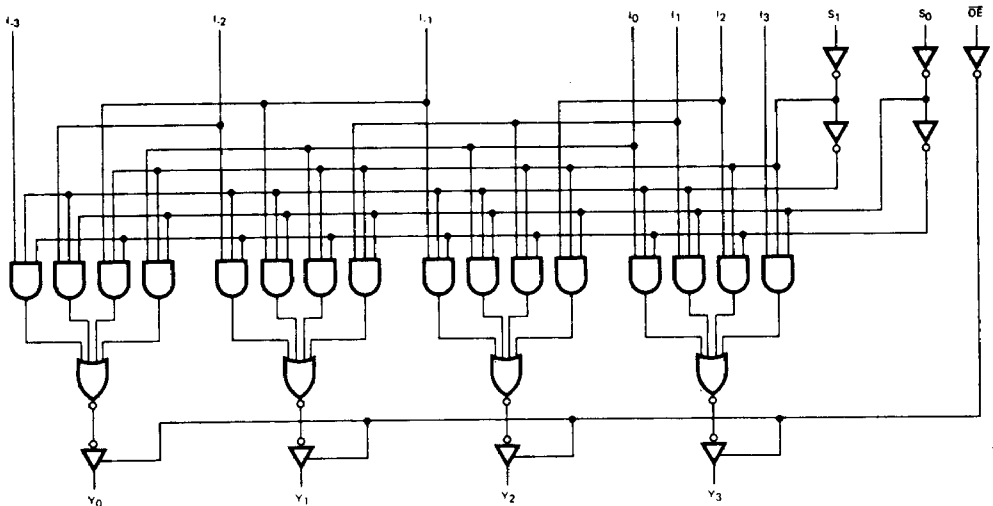
- Shifts 4-bits of data to 0, 1, 2 or 3 places under control of two select lines.
- Three-state outputs for bus organized systems.
- 6.5ns typical data propagation delay
- Alternate source is 54S/74S950

GENERAL DESCRIPTION

The Am25S10 is a combinatorial logic circuit that accepts a four-bit data word and shifts the word 0, 1, 2 or 3 places. The number of places to be shifted is determined by a two-bit select field S_0 and S_1 . An active-LOW enable controls the three-state outputs. This feature allows expansion of shifting over a larger number of places with one delay.

By suitable interconnection, the Am25S10 can be used to shift any number of bits any number of places up or down. Shifting can be logical, with logic zeroes pulled in at either or both ends of the shifting field; arithmetic, where the sign bit is repeated during a shift down; or end around, where the data word forms a continuous loop.

BLOCK DIAGRAM

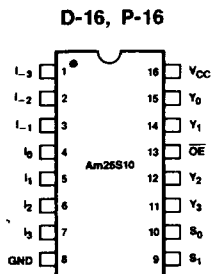


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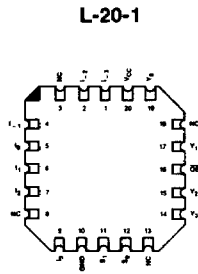
RELATED PRODUCTS

Part No.	Description
Am2901	Bit Slice ALU
Am2903	Superslice
Am29501	Multiport Pipeline Processor

CONNECTION DIAGRAM Top View



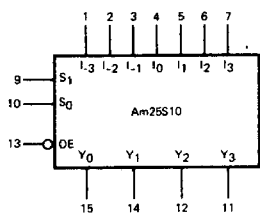
CD004060



CD004050

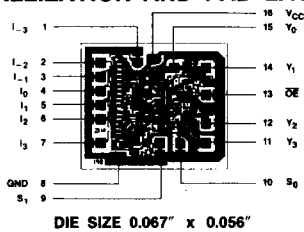
Note: Pin 1 is marked for orientation

LOGIC SYMBOL



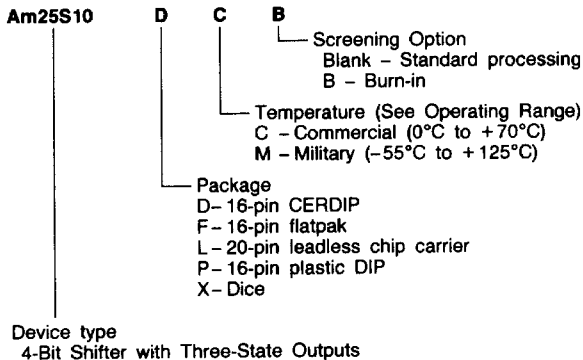
LS000750

METALLIZATION AND PAD LAYOUT



ORDERING INFORMATION

AMD products are available in several packages and operating ranges. The order number is formed by a combination of the following: Device number, speed option (if applicable), package type, operating range and screening option (if desired).



Valid Combinations	
Am25S10	PC DC, DM LC, LM FM XC, XM

Valid Combinations

Consult the AMD sales office in your area to determine if a device is currently available in the combination you wish.

PIN DESCRIPTION

Pin No.	Name	I/O	Description
	I_i	I	The seven data inputs of the shifter.
13	\overline{OE}		Enable. When the enable is HIGH, the four outputs are in the high impedance state. When the enable is LOW, the selected I_i inputs are present at the outputs.
10, 9	S_0, S_1	I	Select inputs. Controls the number of places the inputs are shifted.
11, 12, 14, 15	Y_i	O	The four outputs of the shifter.

LOADING RULES (In Unit Loads)

Input/Output	Pin Nos.	Input Unit Load (Note 1)	Fan-out		
			Output HIGH		Output LOW
			XM	XC	
I-3	1	1	-	-	-
I-2	2	1.5	-	-	-
I-1	3	1.5	-	-	-
I_0	4	1.5	-	-	-
I_1	5	1.5	-	-	-
I_2	6	1.5	-	-	-
I_3	7	1	-	-	-
GND	8	-	-	-	-
S_1	9	1	-	-	-
S_0	10	1	-	-	-
Y_3	11	-	40	130	10
Y_2	12	-	40	130	10
\overline{OE}	13	1	-	-	-
Y_1	14	-	40	130	10
Y_0	15	-	40	130	10
VCC	16	-	-	-	-

A Schottky TTL Unit Load is defined as 50 μ A at 2.7V at the HIGH and -2.0mA at 0.5V at the LOW.

Note 1. The fan-in on I_2, I_1, I_0, I_1 and I_2 will not exceed 1.5 Unit Loads when measured at $V_{IL} = 0.5V$. As V_{IL} is decreased to a 0V, the input current I_{IL} MAX. increases to -4, -6, -8, -6 and -4mA respectively due to the decrease in current sharing with the internal select buffer outputs.

LOGIC EQUATIONS

$$Y_0 = \overline{S_0}\overline{S_1}I_0 + S_0\overline{S_1}I_1 + \overline{S_0}S_1 I_2 + S_0S_1I_3$$

$$Y_1 = \overline{S_0}\overline{S_1}I_1 + S_0\overline{S_1}I_0 + \overline{S_0}S_1 I_1 + S_0S_1I_2$$

$$Y_2 = \overline{S_0}\overline{S_1}I_2 + S_0\overline{S_1}I_1 + \overline{S_0}S_1 I_0 + S_0S_1I_1$$

$$Y_3 = \overline{S_0}\overline{S_1}I_3 + S_0\overline{S_1}I_2 + \overline{S_0}S_1 I_1 + S_0S_1I_0$$

TRUTH TABLE

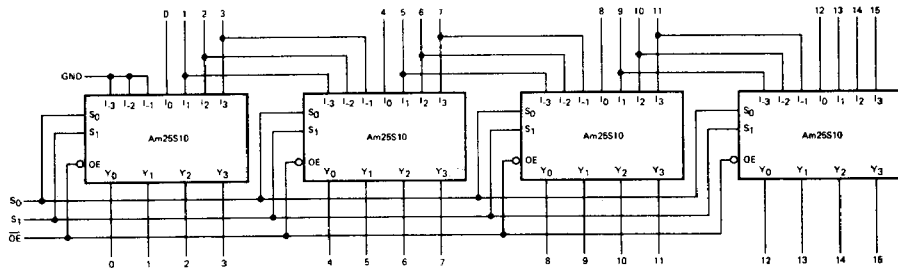
\overline{OE}	S_1	S_0	I_3	I_2	I_1	I_0	I_1	I_2	I_3	Y_3	Y_2	Y_1	Y_0
H	X	X	X	X	X	X	X	X	X	Z	Z	Z	Z
L	L	L	D_3	D_2	D_1	D_0	X	X	X	D_3	D_2	D_1	D_0
L	L	H	X	D_2	D_1	D_0	D_1	X	X	D_2	D_1	D_0	D_1
L	H	L	X	X	D_1	D_0	D_1	D_2	X	D_1	D_0	D_1	D_2
L	H	H	X	X	D_0	D_1	D_2	D_3		D_0	D_1	D_2	D_3

H = HIGH
L = LOW

X = Don't Care
Z = High Impedance State

D_n at input I_n may be either HIGH or LOW and output Y_m will follow the selected D_n input level.

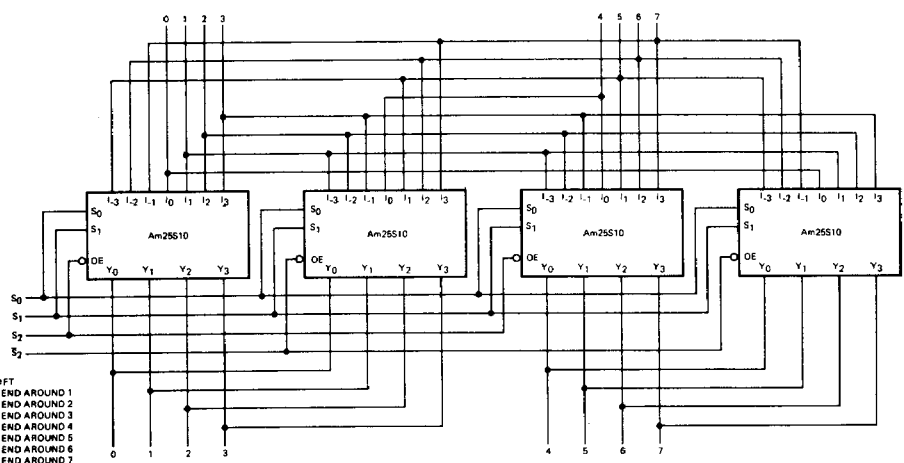
APPLICATIONS



S₁ S₀
 L L NO SHIFT
 L H SHIFT 1 PLACE
 H L SHIFT 2 PLACES
 H H SHIFT 3 PLACES

AF001240

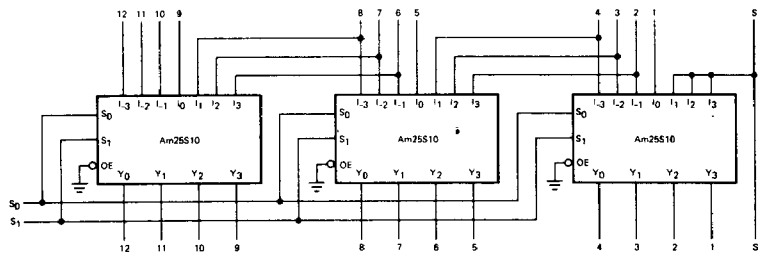
16-Bit Shift-Up 0, 1, 2, or 3 Places.



S₂ S₁ S₀
 L L L NO SHIFT
 L L H SHIFT END AROUND 1
 L H L SHIFT END AROUND 2
 L H H SHIFT END AROUND 3
 H L L SHIFT END AROUND 4
 H L H SHIFT END AROUND 5
 H H L SHIFT END AROUND 6
 H H H SHIFT END AROUND 7

AF001230

8-Bit End Around Shift 0, 1, 2, 3, 4, 5, 6, 7 Places



AF001250

13-Bit 2's Complement Scaler

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	-65°C to +150°C
(Ambient) Temperature Under Bias	-55°C to +125°C
Supply Voltage to Ground Potential	
Continuous	-0.5V to +7.0V
DC Voltage Applied to Outputs For	
High Output State	-0.5V to +V _{CC} max
DC Input Voltage	-0.5V to +5.5V
DC Output Current, Into Outputs	30mA
DC Input Current	-30mA to +5.0mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices	
Temperature	0°C to +70°C
Supply Voltage	+4.75V to +5.25V
Military (M) Devices	
Temperature	-55°C to +125°C
Supply Voltage	+4.5V to +5.5V

Operating ranges define those limits over which the functionality of the device is guaranteed.

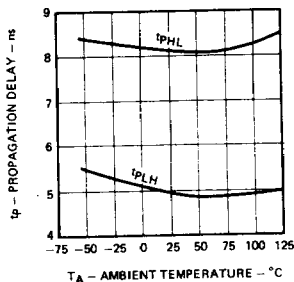
DC CHARACTERISTICS over operating range unless otherwise specified

Parameters	Description	Test Conditions (Note 2)	Min	Typ (Note 1)	Max	Units
V _{OH}	Output HIGH Voltage	V _{CC} = MIN., V _{IN} = V _{IH} or V _{IL} , X _M I _{OH} = -2mA	2.4	3.4		Volts
		X _C I _{OH} = -6.5mA	2.4	3.2		
V _{OL}	Output LOW Voltage	V _{CC} = MIN., I _{OL} = 20mA, V _{IN} = V _{IH} or V _{IL}			0.5	Volts
V _{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs	2.0			Volts
V _{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs			0.8	Volts
V _I	Input Clamp Voltage	V _{CC} = MIN., I _{IN} = -18mA			-1.2	Volts
I _{IL} (Note 3)	Unit Load Input LOW Current	V _{CC} = MAX., V _{IN} = 0.5V			-2.0	mA
I _{IH} (Note 3)	Unit Load Input HIGH Current	V _{CC} = MAX., V _{IN} = 2.7V			50	μA
I _O	Off State (High Impedance) Output Current	V _{CC} = MAX., V _O = 2.4V, V _O = 0.5V			50	μA
					-50	
I _I	Input HIGH Current	V _{CC} = MAX., V _{IN} = 5.5V			1.0	mA
I _{SC}	Output Short Circuit Current (Note 4)	V _{CC} = MAX., V _{OUT} = 0.0V	-40		-100	mA
I _{CC}	Power Supply Current	V _{CC} = MAX., All outputs open, All inputs = GND		60	85	mA

- Notes: 1. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
 2. For conditions shown as MIN. or MAX., use the appropriate value specified under Operating Ranges for the applicable device type.
 3. Actual input currents = Unit Load Current x Input Load Factor (See Loading Rules).
 4. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.

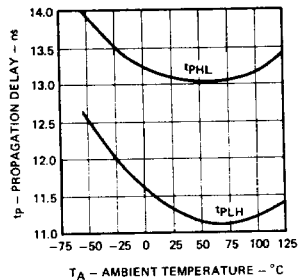
PERFORMANCE CURVES SWITCHING CHARACTERISTICS

Data to Output (Typical)



OP001390

Select to Output (Typical)

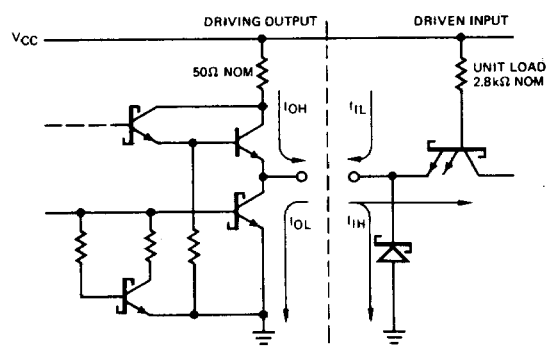


OP001400

SWITCHING CHARACTERISTICS ($T_A = +25^\circ\text{C}$)

Parameters	Description	Test Conditions	Min	Typ	Max	Units	
t_{PLH}	Data Input to Output	$V_{CC} = 5.0\text{V}, C_L = 15\text{pF}, R_L = 280\Omega$		5	7.5	ns	
t_{PHL}				8	12		
t_{PLH}	Select to Output			11	17	ns	
t_{PHL}				13	20		
t_{ZH}	Output Control \overline{OE} to Output					19.5	ns
t_{ZL}						21	
t_{HZ}	Output Control \overline{OE} to Output	$V_{CC} = 5\text{V}, C_L = 5\text{pF}, R_L = 280\Omega$		5	8	ns	
t_{LZ}					10		15

**SCHOTTKY INPUT/OUTPUT
CURRENT INTERFACE CONDITIONS**



IC000370

Note: Actual current flow direction shown.

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