

Integrated Device Technology, Inc.

# FAST CMOS 8-BIT IDENTITY COMPARATOR

**IDT54/74FCT521**  
**IDT54/74FCT521A**  
**IDT54/74FCT521B**  
**IDT54/74FCT521C**

## FEATURES:

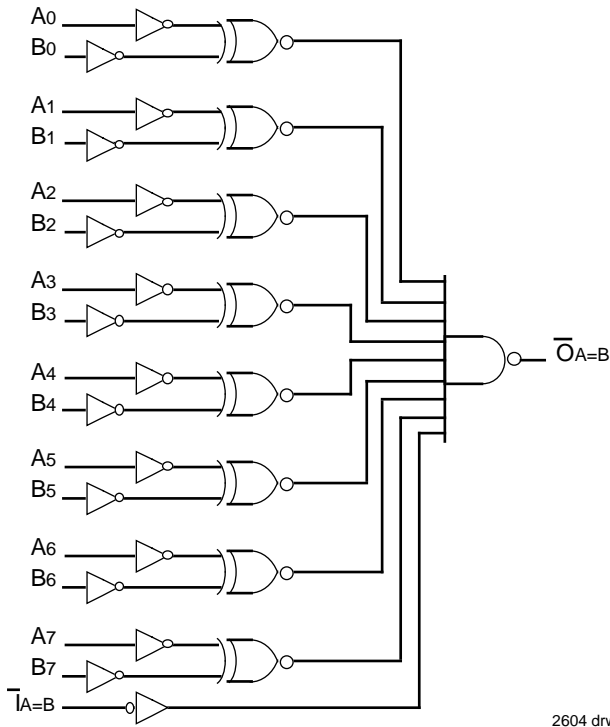
- IDT54/74FCT521 equivalent to FAST™ speed
- IDT54/74FCT521A 35% faster than FAST
- IDT54/74FCT521B 50% faster than FAST
- IDT54/74FCT521C 60% faster than FAST
- Equivalent to FAST output drive over full temperature and voltage supply extremes
- IOL = 48mA (commercial), and 32mA (military)
- CMOS power levels (1mW typ. static)
- TTL input and output level compatible
- CMOS output level compatible
- Substantially lower input current levels than FAST (5µA max.)

- Product available in Radiation Tolerant and Radiation Enhanced versions
- JEDEC standard pinout for DIP and LCC
- Military product compliant to MIL-STD-883, Class B

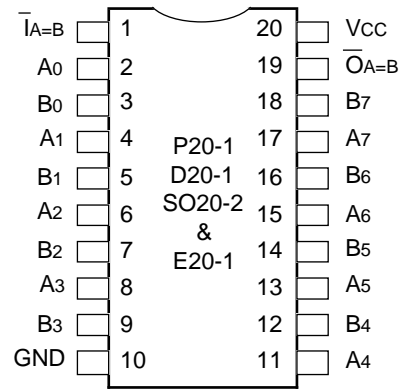
## DESCRIPTION:

The IDT54/74FCT521/A/B/C are 8-bit identity comparators built using an advanced dual metal CMOS technology. These devices compare two words of up to eight bits each and provide a LOW output when the two words match bit for bit. The expansion input  $\bar{I}_A = B$  also serves as an active LOW enable input.

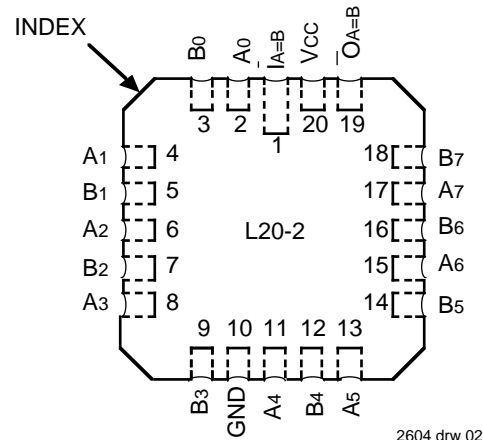
## FUNCTIONAL BLOCK DIAGRAM



## PIN CONFIGURATIONS



**DIP/SOIC/CERPACK  
TOP VIEW**



**LCC  
TOP VIEW**

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**MILITARY AND COMMERCIAL TEMPERATURE RANGES**

**MAY 1992**

**PIN DESCRIPTION**

Pin Names	Description
A0 - A7	Word A Inputs
B0 - B7	Word B Inputs
$\bar{I}A = B$	Expansion or Enable Input (Active LOW)
$\bar{O}A = B$	Identity Output (Active LOW)

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**FUNCTION TABLE<sup>(1)</sup>**

INPUTS		OUTPUT
$\bar{I}A = B$	A, B	$\bar{O}A = B$
L	A = B*	L
L	A ≠ B	H
H	A = B*	H
H	A ≠ B	H

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**NOTE:**

- H = HIGH Voltage Level  
L = LOW Voltage Level  
\*A0 = B0, A1 = B1, A2 = B2, etc.

**ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>**

Symbol	Rating	Commercial	Military	Unit
VTERM <sup>(2)</sup>	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
VTERM <sup>(3)</sup>	Terminal Voltage with Respect to GND	-0.5 to Vcc	-0.5 to Vcc	V
TA	Operating Temperature	0 to +70	-55 to +125	°C
TBIAS	Temperature Under Bias	-55 to +125	-65 to +135	°C
TSTG	Storage Temperature	-55 to +125	-65 to +150	°C
PT	Power Dissipation	0.5	0.5	W
IOUT	DC Output Current	120	120	mA

**NOTES:**

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- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed VCC by +0.5V unless otherwise noted.
- Input and VCC terminals only.
- Outputs and I/O terminals only.

**CAPACITANCE** (TA = +25°C, f = 1.0MHz)

Symbol	Parameter <sup>(1)</sup>	Conditions	Typ.	Max.	Unit
CIN	Input Capacitance	VIN = 0V	6	10	pF
COUT	Output Capacitance	VOUT = 0V	8	12	pF

**NOTE:**

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- This parameter is measured at characterization but not tested.

### DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:  $V_{LC} = 0.2V$ ;  $V_{HC} = V_{CC} - 0.2V$

Commercial:  $T_A = 0^\circ C$  to  $+70^\circ C$ ,  $V_{CC} = 5.0V \pm 5\%$ ; Military:  $T_A = -55^\circ C$  to  $+125^\circ C$ ,  $V_{CC} = 5.0V \pm 10\%$

Symbol	Parameter	Test Conditions <sup>(1)</sup>	Min.	Typ. <sup>(2)</sup>	Max.	Unit	
$V_{IH}$	Input HIGH Level	Guaranteed Logic HIGH Level	2.0	—	—	V	
$V_{IL}$	Input LOW Level	Guaranteed Logic LOW Level	—	—	0.8	V	
$I_{IH}$	Input HIGH Current	$V_{CC} = \text{Max.}$	$V_i = V_{CC}$	—	—	5	$\mu A$
			$V_i = 2.7V$	—	—	5 <sup>(4)</sup>	
$I_{IL}$	Input LOW Current		$V_i = 0.5V$	—	—	-5 <sup>(4)</sup>	
			$V_i = GND$	—	—	-5	
$V_{IK}$	Clamp Diode Voltage	$V_{CC} = \text{Min.}, I_N = -18mA$	—	-0.7	-1.2	V	
$I_{OS}$	Short Circuit Current	$V_{CC} = \text{Max.}^{(3)}, V_O = GND$	-60	-120	—	mA	
$V_{OH}$	Output HIGH Voltage	$V_{CC} = 3V, V_{IN} = V_{LC} \text{ or } V_{HC}, I_{OH} = -32\mu A$	$V_{HC}$	$V_{CC}$	—	V	
		$V_{CC} = \text{Min.}$ $V_{IN} = V_{IH} \text{ or } V_{IL}$	$I_{OH} = -300\mu A$	$V_{HC}$	$V_{CC}$		—
			$I_{OH} = -12mA \text{ MIL.}$	2.4	4.3		—
			$I_{OH} = -15mA \text{ COM'L.}$	2.4	4.3		—
$V_{OL}$	Output LOW Voltage	$V_{CC} = 3V, V_{IN} = V_{LC} \text{ or } V_{HC}, I_{OL} = 300\mu A$	—	GND	$V_{LC}$	V	
		$V_{CC} = \text{Min.}$ $V_{IN} = V_{IH} \text{ or } V_{IL}$	$I_{OL} = 300\mu A$	—	GND		$V_{LC}^{(4)}$
			$I_{OL} = 32mA \text{ MIL.}$	—	0.3		0.5
			$I_{OL} = 48mA \text{ COM'L.}$	—	0.3		0.5

**NOTES:**

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at  $V_{CC} = 5.0V$ ,  $+25^\circ C$  ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
4. This parameter is guaranteed but not tested.

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**POWER SUPPLY CHARACTERISTICS**  $V_{LC} = 0.2V$ ;  $V_{HC} = V_{CC} - 0.2V$

Symbol	Parameter	Test Conditions <sup>(1)</sup>		Min.	Typ. <sup>(2)</sup>	Max.	Unit
I <sub>CC</sub>	Quiescent Power Supply Current	$V_{CC} = \text{Max.}$ $V_{IN} \geq V_{HC}$ ; $V_{IN} \leq V_{LC}$		—	0.2	1.5	mA
$\Delta I_{CC}$	Quiescent Power Supply Current TTL Inputs HIGH	$V_{CC} = \text{Max.}$ $V_{IN} = 3.4V^{(3)}$		—	0.5	2.0	mA
I <sub>CCD</sub>	Dynamic Power Supply Current <sup>(4)</sup>	$V_{CC} = \text{Max.}$ Outputs Open One Input Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$	—	0.15	0.25	mA/ MHz
I <sub>C</sub>	Total Power Supply Current <sup>(5)</sup>	$V_{CC} = \text{Max.}$ Outputs Open $f_i = 10\text{MHz}$ One Bit Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT) $V_{IN} = 3.4V$ $V_{IN} = \text{GND}$	—	1.7	4.0	mA
				—	2.0	5.0	

**NOTES:**

2604 tbl\* 04

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at  $V_{CC} = 5.0V$ ,  $+25^\circ\text{C}$  ambient.
- Per TTL driven input ( $V_{IN} = 3.4V$ ); all other inputs at  $V_{CC}$  or  $\text{GND}$ .
- This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
- $I_C = I_{\text{QUIESCENT}} + I_{\text{INPUTS}} + I_{\text{DYNAMIC}}$   
 $I_C = I_{CC} + \Delta I_{CC} \text{DHNT} + I_{CCD} (f_{CP}/2 + f_i N_i)$   
 $I_{CC} = \text{Quiescent Current}$   
 $\Delta I_{CC} = \text{Power Supply Current for a TTL High Input } (V_{IN} = 3.4V)$   
 $\text{DH} = \text{Duty Cycle for TTL Inputs High}$   
 $N_T = \text{Number of TTL Inputs at DH}$   
 $I_{CCD} = \text{Dynamic Current Caused by an Input Transition Pair (HLH or LHL)}$   
 $f_{CP} = \text{Clock Frequency for Register Devices (Zero for Non-Register Devices)}$   
 $f_i = \text{Input Frequency}$   
 $N_i = \text{Number of Inputs at } f_i$   
 All currents are in milliamps and all frequencies are in megahertz.

**SWITCHING CHARACTERISTICS OVER OPERATING RANGE**

Symbol	Parameter	Condition <sup>(1)</sup>	IDT54/74FCT521		IDT54/74FCT521A		IDT54/74FCT521B		IDT54/74FCT521C				Unit						
			Com'l.		Mil.		Com'l.		Mil.		Com'l.			Mil.					
			Min. <sup>(2)</sup>	Max.	Min. <sup>(2)</sup>	Max.	Min. <sup>(2)</sup>	Max.	Min. <sup>(2)</sup>	Max.	Min. <sup>(2)</sup>	Max.		Min. <sup>(2)</sup>	Max.				
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay An or Bn to $\overline{O_A} = B$	$C_L = 50\text{pF}$ $R_L = 500\Omega$	1.5	11.0	1.5	15.0	1.5	7.2	1.5	9.5	1.5	5.5	1.5	7.3	1.5	4.5	1.5	5.1	ns
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay $ A = B$ to $\overline{O_A} = B$		1.5	10.0	1.5	9.0	1.5	6.0	1.5	7.8	1.5	4.6	1.5	6.0	1.5	4.1	1.5	4.5	ns

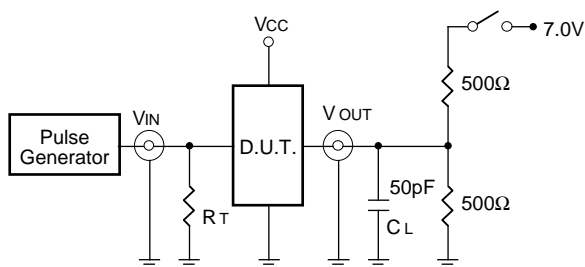
**NOTES:**

2604 tbl\* 07

- See test circuit and waveforms.
- Minimum limits are guaranteed but not tested on Propagation Delays.

## TEST CIRCUITS AND WAVEFORMS

### TEST CIRCUITS FOR ALL OUTPUTS



### SWITCH POSITION

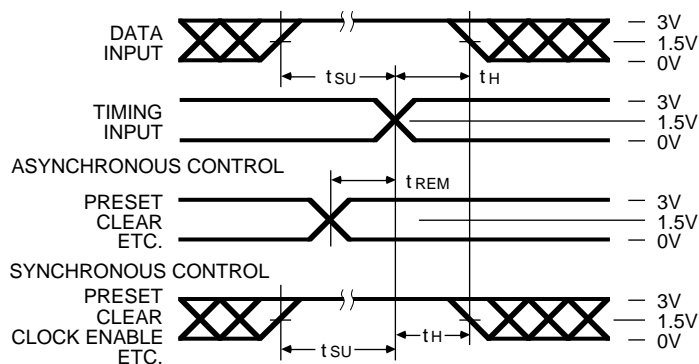
Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Tests	Open

#### DEFINITIONS:

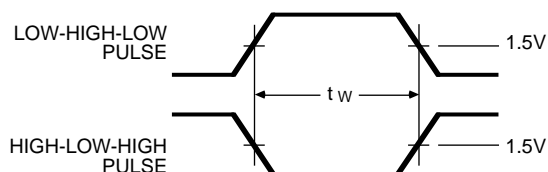
CL = Load capacitance: includes jig and probe capacitance.  
RT = Termination resistance: should be equal to ZOUT of the Pulse Generator.

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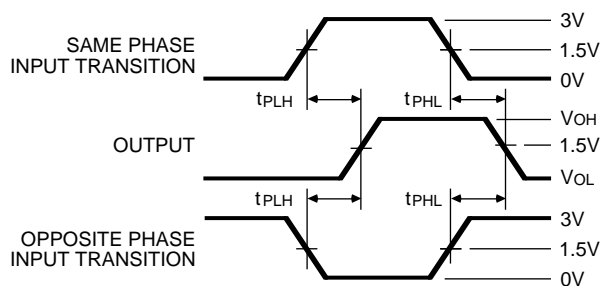
### SET-UP, HOLD AND RELEASE TIMES



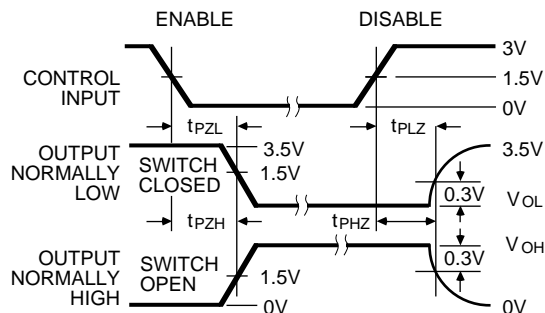
### PULSE WIDTH



### PROPAGATION DELAY



### ENABLE AND DISABLE TIMES

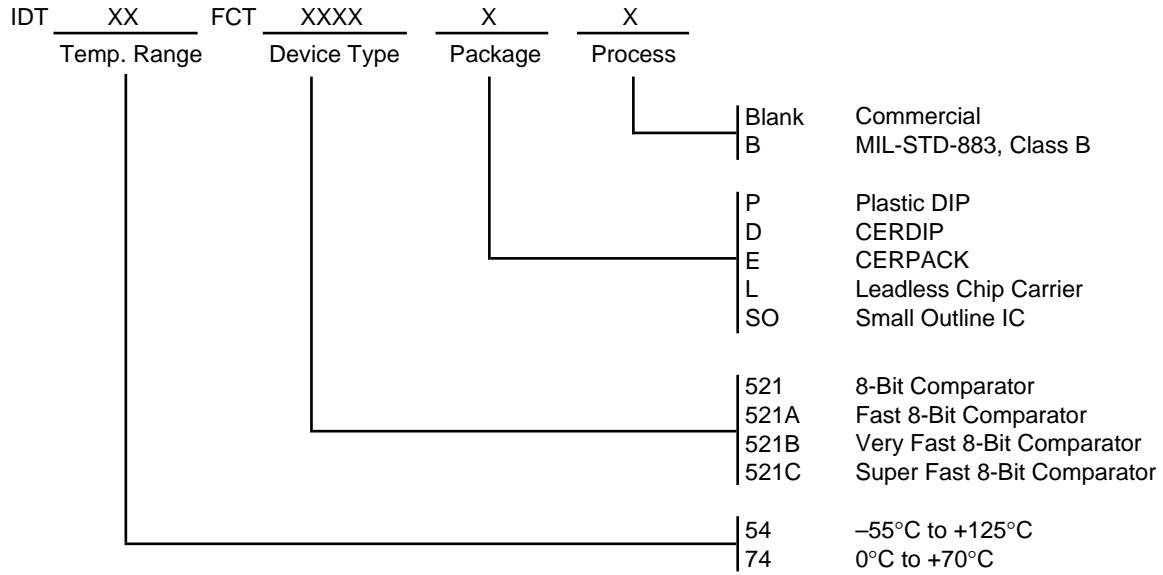


#### NOTES

- Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.
- Pulse Generator for All Pulses: Rate  $\leq 1.0$  MHz; Zo  $\leq 50\Omega$ ; tr  $\leq 2.5$ ns;  $t_r \leq 2.5$ ns.

2604 drw 04

**ORDERING INFORMATION**



2604 cnv\* 09

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