

DM74AS286

9-Bit Parity Generator/Checker with Bus-Driver Parity I/O Port

General Description

These universal, 9-bit parity generators/checkers utilize advanced Schottky high performance circuitry and feature odd/even outputs to facilitate operation of either odd or even parity applications. The word length capability is easily expanded by cascading.

The DM74AS286 can be used to upgrade the performance of most systems utilizing the DM74AS280 parity generator/checker. Although the DM74AS286 is implemented without expander inputs, the corresponding function is provided by the availability of an input pin $\overline{\text{XMIT}}$. $\overline{\text{XMIT}}$ is a control line which makes parity error output active and parity an input port when HIGH; when LOW, parity error output is inactive and parity becomes an output port. In addition, parity I/O control circuitry contains a feature to keep the I/O port in the 3-STATE during power UP or DOWN to prevent bus glitches.

Features

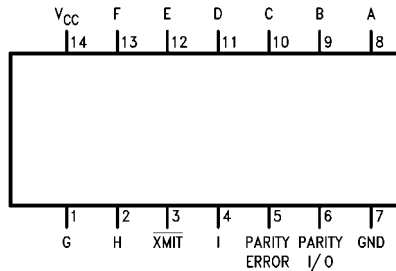
- PNP inputs to reduce bus loading
- Generates either odd or even parity for nine data lines
- Inputs are buffered to lower the drive requirements
- Can be used to upgrade existing systems using MSI parity circuits
- Cascadable for n-bits
- Switching specifications at 50 pF
- Switching specifications guaranteed over full temperature and V_{CC} range
- A parity I/O portable to drive bus

Ordering Code:

| Order Number | Package Number | Package Description |
|--------------|----------------|---|
| DM74AS286M | M14A | 14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150 Narrow |
| DM74AS286N | N14A | 14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide |

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Connection Diagram



Function Table

| Number of Inputs (A thru I) that are HIGH | Parity I/O | | $\overline{\text{XMIT}}$ | Parity Error | Mode of Operation |
|---|------------|--------|--------------------------|-----------------|-------------------------|
| | Input | Output | | | |
| 0, 2, 4, 6, 8 | N/A | H | L | H | Parity Generator |
| 1, 3, 5, 7, 9 | N/A | L | L | H | Parity Checker |
| 0, 2, 4, 6, 8 | H | N/A | H | H | Parity Generator |
| 0, 2, 4, 6, 8 | L | N/A | H | L | Parity Checker |
| 1, 3, 5, 7, 9 | H | N/A | H | L | Parity Generator |
| 1, 3, 5, 7, 9 | L | N/A | H | H | Parity Checker |

L = LOW Logic Level
H = HIGH Logic Level
N/A = Not Applicable

Absolute Maximum Ratings(Note 1)

| | |
|--------------------------------------|-----------------|
| Supply Voltage | 7V |
| Input Voltage | 7V |
| Operating Free Air Temperature Range | 0°C to +70°C |
| Storage Temperature Range | -65°C to +150°C |
| Typical θ_{JA} | |
| N Package | 77.0°C/W |
| M Package | 108.0°C/W |

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Recommended Operating Conditions

| Symbol | Parameter | Min | Typ | Max | Units |
|----------|--------------------------------|--------------|-----|-----|-------|
| V_{CC} | Supply Voltage | 4.5 | 5 | 5.5 | V |
| V_{IH} | HIGH Level Input Voltage | 2 | | | V |
| V_{IL} | LOW Level Input Voltage | | | 0.8 | V |
| I_{OH} | HIGH Level Output Current | Parity I/O | | -15 | mA |
| | | Parity Error | | -2 | mA |
| I_{OL} | LOW Level Output Current | Parity I/O | | 48 | mA |
| | | Parity Error | | 20 | mA |
| T_A | Operating Free-Air Temperature | 0 | | 70 | °C |

Electrical Characteristics

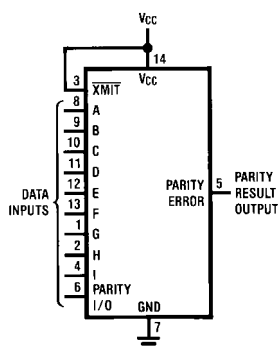
over recommended free-air temperature range. All typical values are measured at $V_{CC} = 5V$, $T_A = 25^\circ C$.

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|----------|--|---|--------------|------|------|---------|
| V_{IK} | Input Clamp Voltage | $V_{CC} = 4.5V$, $I_{IN} = -18\text{ mA}$ | | | -1.2 | V |
| V_{OH} | HIGH Level | $I_{OH} = \text{Max}$, $V_{CC} = 4.5V$ | 2.4 | 3.2 | | V |
| | Output Voltage | $V_{CC} = 4.5V$ to $5.5V$, $I_{OH} = -2\text{ mA}$ | $V_{CC} - 2$ | | | V |
| V_{OL} | LOW Level Output Voltage | $V_{CC} = 4.5V$, $I_{OL} = \text{Max}$ | | 0.35 | 0.5 | V |
| I_I | Input Current at Maximum Input Voltage | $V_{CC} = 5.5V$, $V_{IH} = 7V$ ($V_I = 5.5V$ for Parity I/O) | | | 0.1 | mA |
| I_{IH} | HIGH Level Input Current | $V_{CC} = 5.5V$ | Others | | 20 | μA |
| | | $V_{IH} = 2.7V$ (Note 2) | Parity I/O | | 50 | |
| I_{IL} | LOW Level Input Current | $V_{CC} = 5.5V$, $V_{IL} = 0.4V$ (Note 2) | | | -0.5 | mA |
| I_O | Output Drive Current | $V_{CC} = 5.5V$, $V_{OUT} = 2.25V$ | -30 | | -112 | mA |
| I_{CC} | Supply Current | $V_{CC} = 5.5V$, Transmit Mode XMIT = LOW | | | 43 | mA |
| | | Receive Mode XMIT = HIGH | | | 50 | mA |

Note 2: For I/O ports, the parameters I_{IH} and I_{IL} include the OFF-state current, I_{OZH} and I_{OZL} .

| Switching Characteristics | | | | | | |
|---|--|----------------|--------------|-----|------|-------|
| over recommended supply and temperature range | | | | | | |
| Symbol | Parameter | From | To | Min | Max | Units |
| t _{PLH} | Propagation Delay Time from LOW-to-HIGH Level Output | Any Data Input | Parity I/O | 3 | 15 | ns |
| t _{PHL} | Propagation Delay Time from HIGH-to-LOW Level Output | Any Data Input | Parity I/O | 3 | 14 | ns |
| t _{PLH} | Propagation Delay Time from LOW-to-HIGH Level Output | Any Data Input | Parity Error | 3 | 16.5 | ns |
| t _{PHL} | Propagation Delay Time from HIGH-to-LOW Level Output | Any Data Input | Parity Error | 3 | 16.5 | ns |
| t _{PLH} | Propagation Delay Time from LOW-to-HIGH Level Output | Parity I/O | Parity Error | 3 | 9 | ns |
| t _{PHL} | Propagation Delay Time from HIGH-to-LOW Level Output | Parity I/O | Parity Error | 3 | 9 | ns |
| t _{PZL} | Output Enable Time to LOW Level | XMIT | Parity I/O | 3 | 16 | ns |
| t _{PLZ} | Output Disable Time from LOW Level | XMIT | Parity I/O | 3 | 10 | ns |
| t _{PZH} | Output Disable Time from HIGH Level | XMIT | Parity I/O | 3 | 13 | ns |
| t _{PHZ} | Output Enable Time to HIGH Level | XMIT | Parity I/O | 3 | 11.5 | ns |

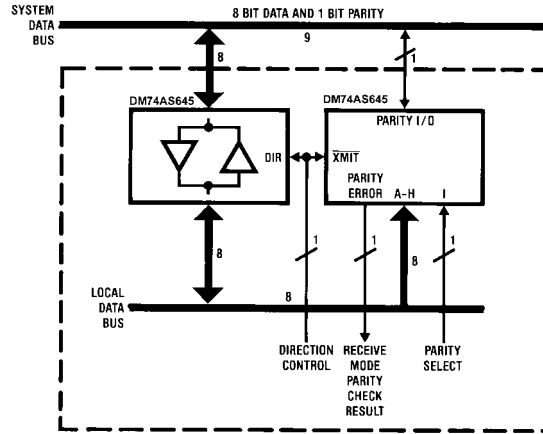
Typical Applications



| Number of Inputs that are Logic "1" | Parity Result Output |
|-------------------------------------|----------------------|
| 0, 2, 4, 6, 8, 10 | Even L |
| 1, 3, 5, 7, 9 | Odd H |

FIGURE 1. Dedicated 10-Bit Parity Sensing Configuration

Typical Applications (Continued)



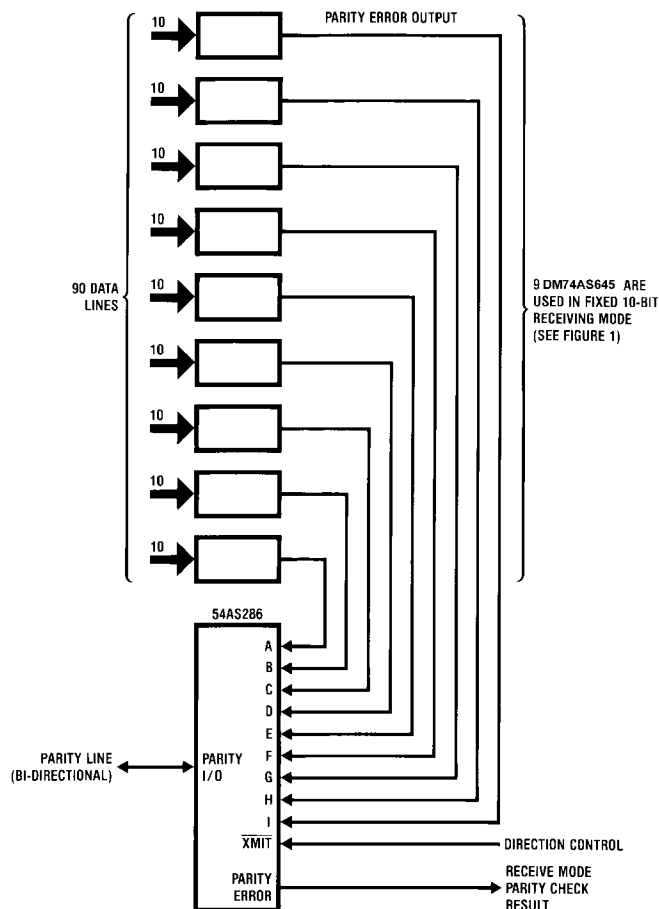
| Direction Control (XMIT) | I/O Direction (Parity I/O) | Parity Check Result (Parity Error) | |
|--------------------------|----------------------------|------------------------------------|-----------------|
| | | Level | Σ Result |
| H | Input (Receive) | H | True |
| | | L | False |
| L | Output (Transmit) | H | N/A |

| Parity Select (Input I) | |
|-------------------------|--------|
| Level | Format |
| H | Even |
| L | Odd |

L = LOW Logic Level
H = HIGH Logic Level
N/A = Not Applicable

FIGURE 2. Bus I/O Parity Implementation

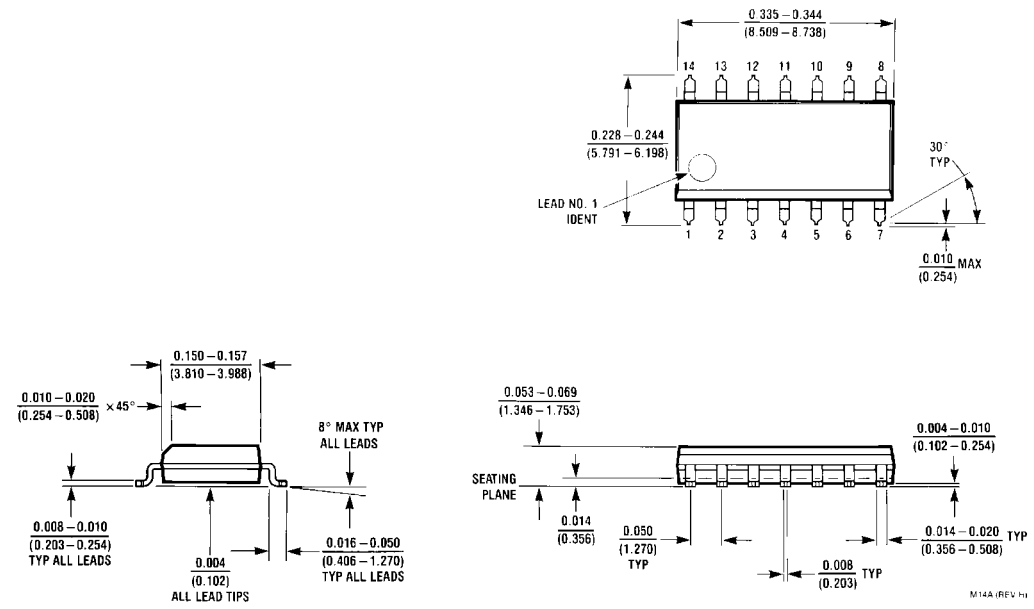
Typical Applications (Continued)



Note: Parity format in this configuration is "odd parity"

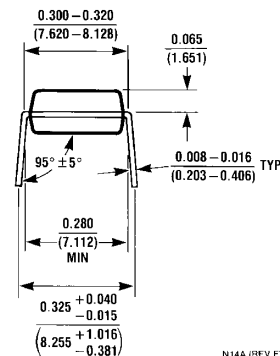
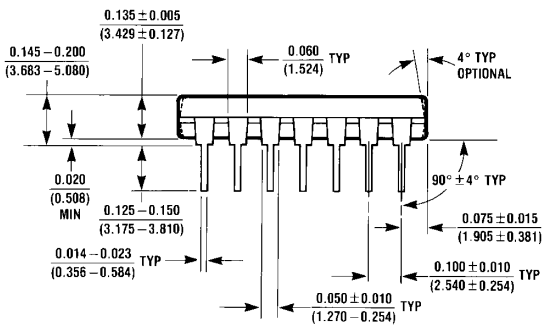
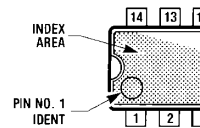
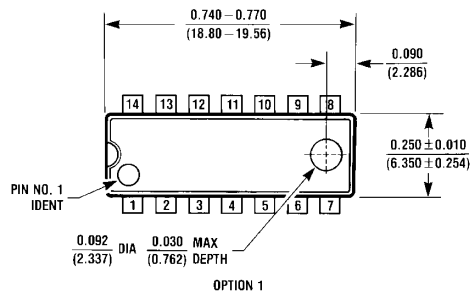
FIGURE 3. 90-Bit Parity Generator/Checker Implementation Using Device Expansion Techniques

Physical Dimensions inches (millimeters) unless otherwise noted



14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150 Narrow Package Number M14A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



N14A (REV F)

14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide Package Number N14A

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