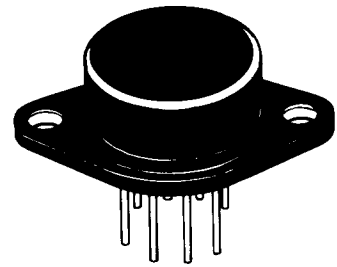


1460

High Power VMOS Output Operational Amplifier



The 1460 heralds a new era in high power, wideband operational amplifiers. Originally designed for ATE signal amplification and pin driving, the 1460 surpasses its competition in speed and output capabilities with a 1GHz gain-bandwidth product, a 300V/ μ sec slew rate, and a full ± 30 V, ± 150 mA output. The 1460 is a full differential input, single-ended output device with internal current limiting. External compensation with a single capacitor allows users to tailor 1460 performance for different applications.

The 1460 is ideally suited for high speed, high gain configurations that require a ± 30 V, high current output. It has been optimized for gains greater than five, making it a superb choice for either analog or digital signal amplification at video frequencies. Secondary breakdown problems associated with most power op amps are eliminated in the 1460 through the use of a unique VMOS output stage. The output voltages and currents are limited only by power dissipation and not by safe operating area curves.

The 1460 is a 0°C to +70°C device that comes in an 8 pin, TO-3 package. For any condition in which the amplifier will be dissipating more than one watt of power, an external heat sink must be used. The thermal resistance of the output transistors is 20°C/watt θ_{JC} and 50°C/watt θ_{JA} . Junction temperatures should not exceed 150°C for normal operation or 200°C for a short-circuit condition.

The 1460-83 is specified over the -55°C to +125°C temperature range and meets the high reliability requirements of MIL-STD-883C, Class "B". This device may also be ordered screened to Class "S".

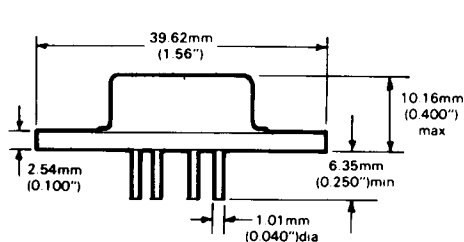
FEATURES

- ± 30 Volt, ± 150 mA Output
- VMOS Output Stage
- No SOA Restrictions
- 1GHz GBW Product
- 300V/ μ sec Slew Rate
- Fully Differential Input

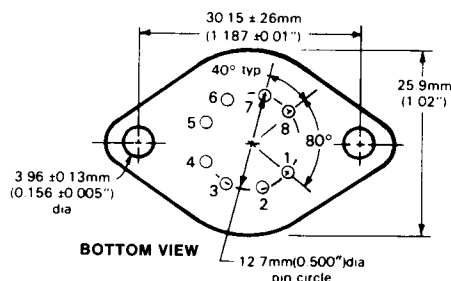
APPLICATIONS

- Video Amplifiers
- Video Yoke Drivers
- ATE Pin Drivers
- Driving Inductive and Capacitive Loads

PACKAGE DIMENSIONS



TO-3 METAL CAN



PIN DESIGNATION

1. OUTPUT
2. OFFSET ADJUST
3. +V_{CC}
4. +IN
5. -IN
6. -V_{CC}
7. COMP
8. COMP./OFFSET

SPECIFICATIONS: ($T_c=+25^\circ\text{C}$, $V_{cc}=\pm 36\text{V}$, unless otherwise indicated).

	TYPICAL	GUARANTEED
OUTPUT RANGE Voltage ($R_L = 200\Omega$) Current	$\pm 31\text{V}$ $\pm 200\text{mA}$	$\pm 30\text{V}$ $\pm 150\text{mA}$
DYNAMIC RESPONSE Gain Bandwidth Product $C_c = 0\text{pF}$ $C_c = 40\text{pF}$ Rise Time 0 to $\pm 5\text{V}$ Step 0 to $\pm 30\text{V}$ Step Settling Time 10V Step to 0.1% 30V Step to 0.1% Slew Rate $C_c = 0$ $C_c = 40\text{pF}$	1.0GHz 150MHz 70ns 400ns 800ns 1 μs 300V/ μs 65V/ μs	— — — — — — 50V/ μs
VOLTAGE GAIN (DC Open Loop) Rated Load	92dB	80dB
INPUT VOLTAGE RANGE(1) Common Mode (Fault Condition) Differential Input Voltage, max. CMRR PSRR	— — 85dB 100dB	$+V_{cc} - 1.5\text{V}$ to $+V_{cc} - 55\text{V}$ $\pm 6\text{V}$ 70dB 75dB
INPUT OFFSET VOLTAGE Initial Vs. Temp.	$\pm 1\text{mV}$ $\pm 10 \mu\text{V}^\circ\text{C}$	$\pm 5\text{mV}$ $\pm 50 \mu\text{V}^\circ\text{C}$
INPUT BIAS CURRENT Initial Input Offset Current Input Bias Current T.C.	$\pm 5 \mu\text{A}$ $\pm 0.3 \mu\text{A}$ 0.8%/ $^\circ\text{C}$	$\pm 10 \mu\text{A}$ — —
POWER REQUIREMENTS Nominal Voltage Quiescent Current Short Circuit Current Supply Voltage Range	$\pm 36\text{V}$ $\pm 20\text{mA}$ 250mA —	— $\pm 25\text{mA}$ 300mA max. $\pm 15\text{V}$ to $\pm 40\text{V}$
TEMPERATURE RANGE Operating Temperature (Case): 1460 1460-83 Storage Range	— — —	0°C to $+70^\circ$ -55°C to $+125^\circ\text{C}$ -65°C to $+150^\circ\text{C}$

NOTES

1. May be nulled with a 500 Ω potentiometer between pins 2 and 8, with the wiper going to $+V_{cc}$.

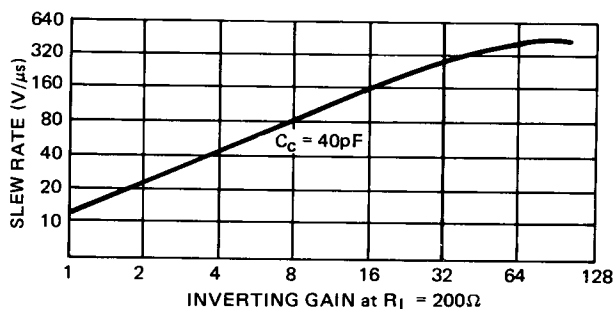


Figure 1. Slew Rate vs. Inverting Gain

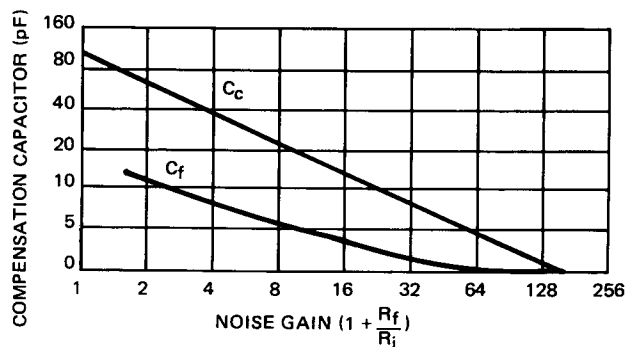


Figure 2. Recommended Compensation

C _{comp} "pF"	Frequency at Unity Gain	Phase at Unity Gain	Frequency at 180°	Slew
0	74MHz	275°	5MHz	250V/μs
10	74MHz	267°	25MHz	125V/μs
20	55MHz	277°	32MHz	84V/μs
40	50MHz	216°	36MHz	50V/μs
80	32MHz	165°	37MHz	28V/μs
180	17MHz	132°	45MHz	25V/μs
330	10MHz	118°	50MHz	7V/μs

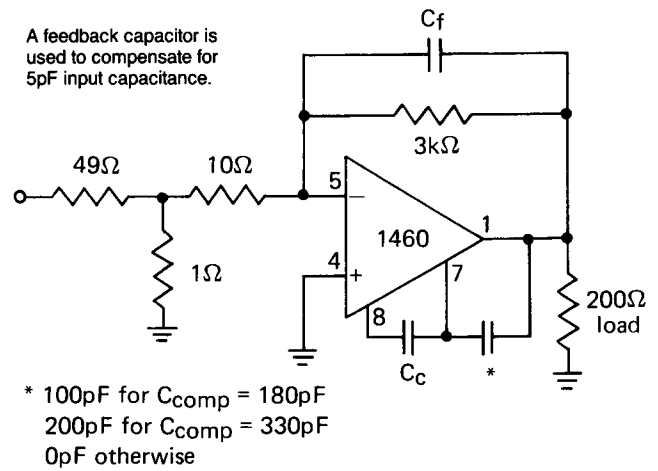
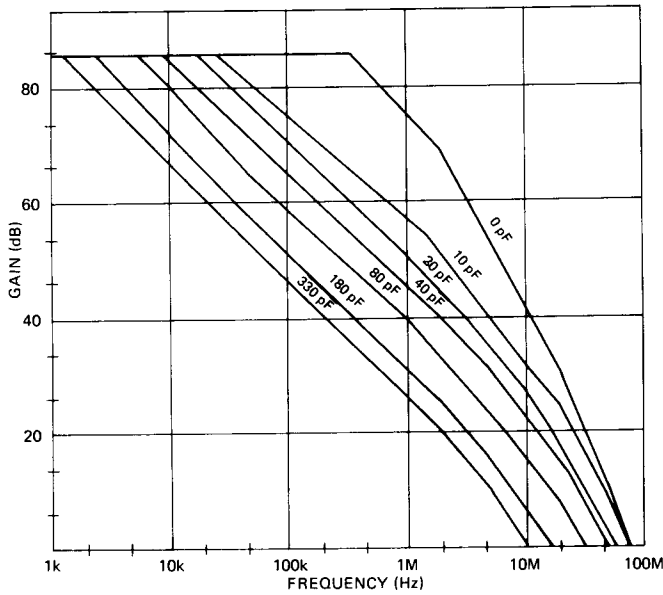


Figure 3. 1460 Bode Plot and Test Circuit

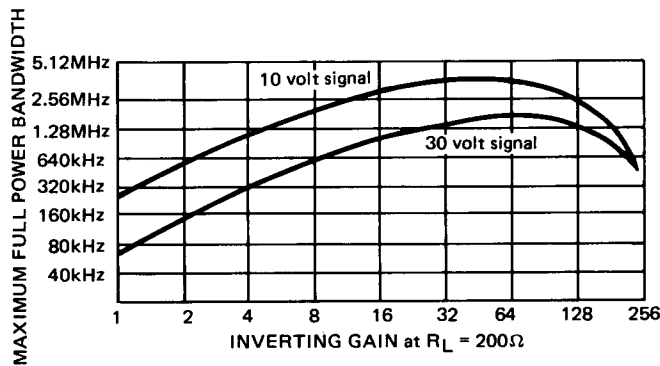


Figure 4. Full Power Bandwidth vs. Inverting Gain

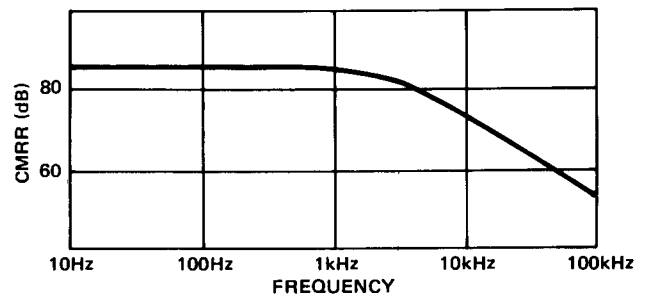


Figure 5. CMRR vs. Frequency

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