

DATA SHEET

74F256

Dual addressable latch

Product specification

1988 Nov 29

IC15 Data Handbook

Dual addressable latch

74F256

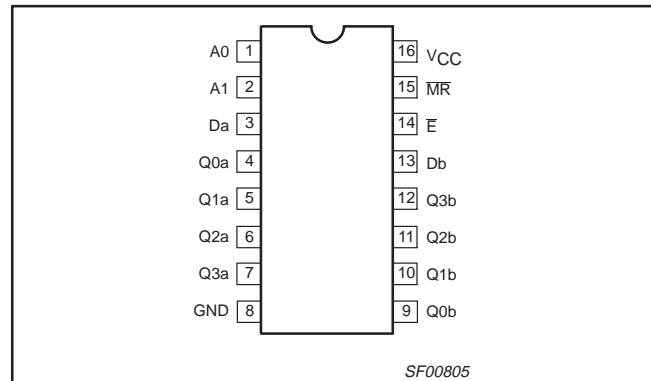
FEATURES

- Combines dual demultiplexer and 8-bit latch
- Serial-to-parallel capability
- Output from each storage bit available
- Random (addressable) data entry
- Easily expandable
- Common reset input
- Useful as dual 1-of-4 active High decoder

DESCRIPTION

The 74F256 dual addressable latch has four distinct modes of operation which are selectable by controlling the Master Reset (\overline{MR}) and Enable (\overline{E}) inputs (see Function Table). In the addressable latch mode, data at the Data inputs is written into the addressed latches. The addressed latches will follow the Data input with all unaddressed latches remaining in their previous states. In the memory mode, all latches remain in their previous states and are unaffected by the Data or Address inputs. To eliminate the possibility of entering erroneous data in the latches, the enable should be held High (inactive) while the address lines are changing. In the dual 1-of-4 decoding or demultiplexing mode ($\overline{MR}=\overline{E}=\text{Low}$), addressed outputs will follow the level of the Data inputs, with all other outputs Low. In the Master Reset mode, all outputs are Low and unaffected by the Address and Data inputs.

PIN CONFIGURATION



TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F256	7.0ns	28mA

ORDERING INFORMATION

DESCRIPTION	ORDER CODE	PKG DWG #
	COMMERCIAL RANGE $V_{CC} = 5V \pm 10\%$, $T_{amb} = 0^{\circ}\text{C to } +70^{\circ}\text{C}$	
16-pin plastic DIP	N74F256N	SOT38-4
16-pin plastic SO	N74F256D	SOT109-1

INPUT AND OUTPUT LOADING AND FAN OUT TABLE

PINS	DESCRIPTION	74F (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
Da, Db	Port A, port B inputs	1.0/1.0	20 μ A/0.6mA
A0, A1	Address inputs	1.0/1.0	20 μ A/0.6mA
\overline{E}	Enable (active Low)	1.0/1.0	20 μ A/0.6mA
\overline{MR}	Master Reset inputs (active Low)	1.0/1.0	20 μ A/0.6mA
Q0a – Q3a	Port A outputs	50/33	1.0mA/20mA
Q0b – Q3b	Port B outputs	50/33	1.0mA/20mA

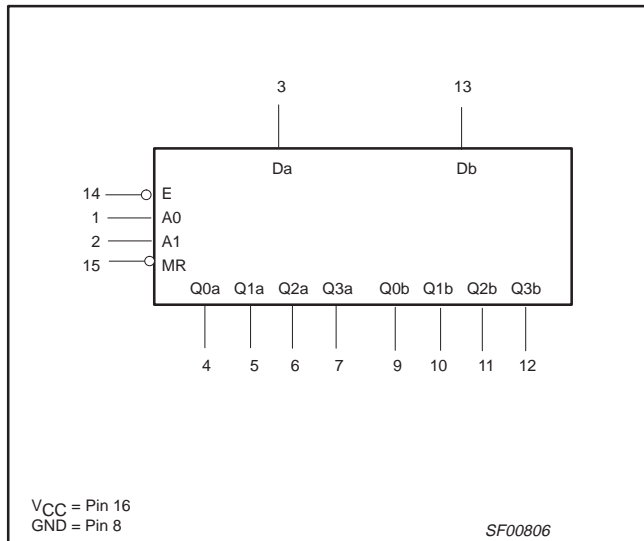
NOTE:

One (1.0) FAST unit load is defined as: 20 μ A in the High state and 0.6mA in the Low state.

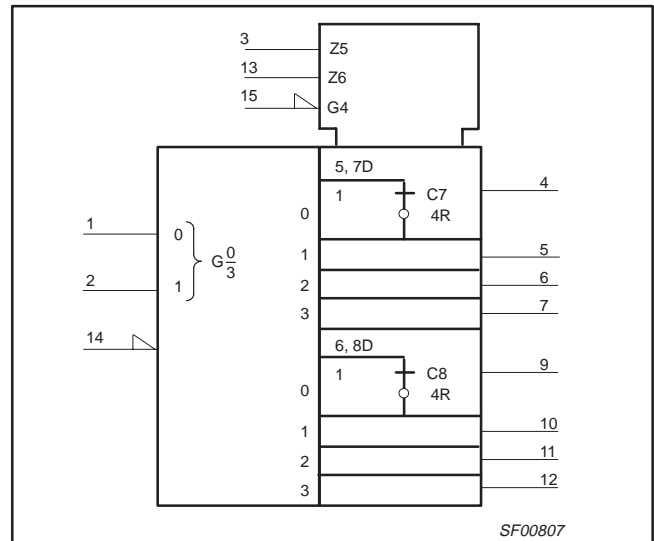
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LOGIC SYMBOL



IEC/IEEE SYMBOL



FUNCTION TABLE

INPUTS					OUTPUTS				OPERATING MODE
MR	\bar{E}	D	A0	A1	Q0	Q1	Q2	Q3	
L	H	X	X	X	L	L	L	L	Master Reset
L	L	d	H	L	Q=d	L	L	L	Demultiplex (active-High decoder when D=H)
L	L	d	L	H	L	L	Q=d	L	
L	L	d	H	H	L	L	L	Q=d	
L	L	d	H	H	L	L	L	Q=d	
H	H	X	X	X	q0	q1	q2	q3	Store (do nothing)
H	L	d	H	L	Q=d	q1	q2	q3	Addressable Latch
H	L	d	L	H	q0	q1	Q=d	q3	
H	L	d	L	H	q0	q1	Q=d	q3	
H	L	d	H	H	q0	q1	q2	Q=d	

H = High voltage level

L = Low voltage level

X = Don't care

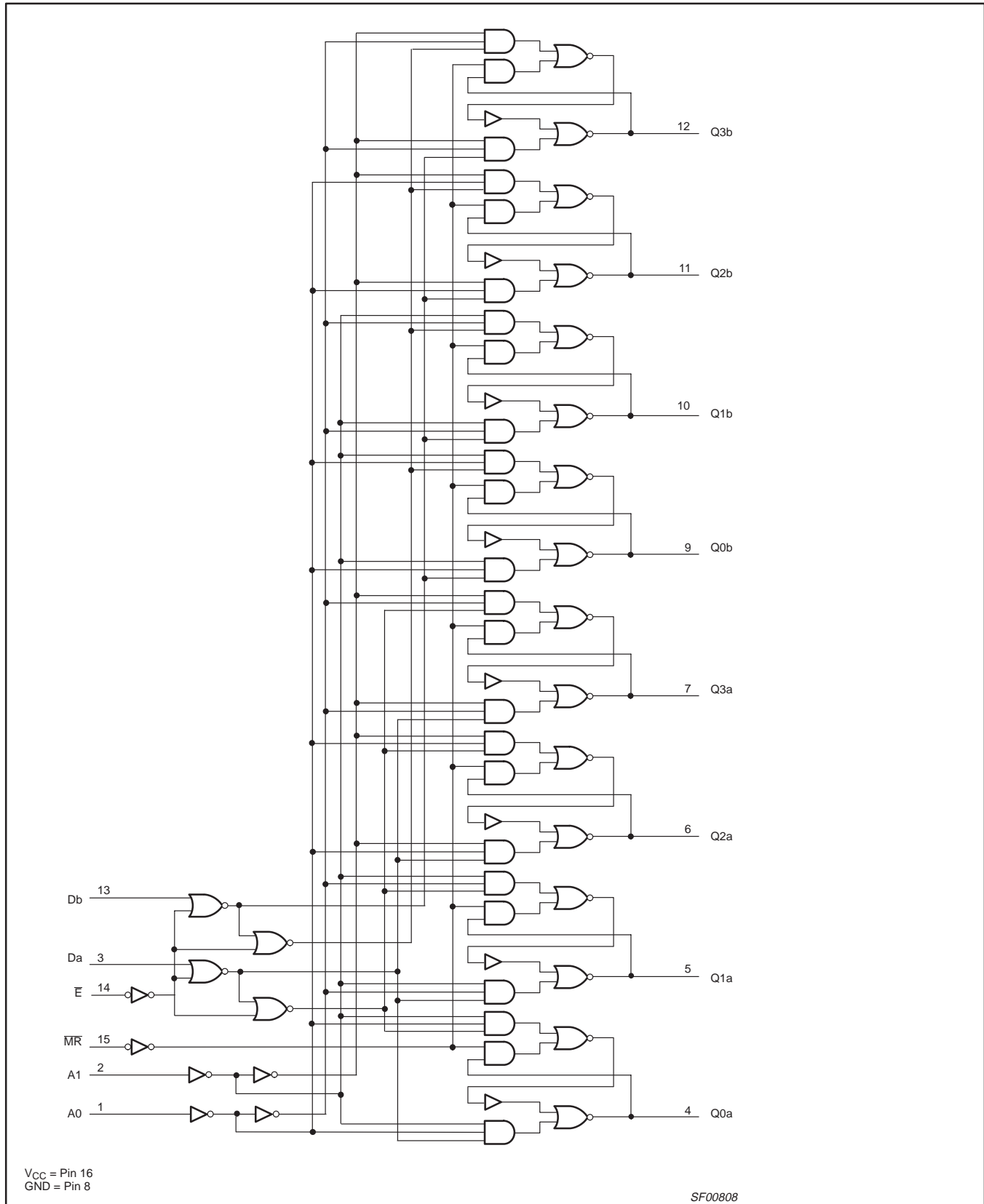
d = High or Low data one setup time prior to the Low-to-High Enable transition

q = Lower case letters indicate the state of the referenced output established during the last cycle in which it was addressed or cleared.

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LOGIC DIAGRAM



Dual addressable latch

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ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limit set forth in this table may impair the useful life of the device.
Unless otherwise noted these limits are over the operating free air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to V_{CC}	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_{amb}	Operating free-air temperature range	0 to +70	°C
T_{stg}	Storage temperature range	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-1	mA
I_{OL}	Low-level output current			20	mA
T_{amb}	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS ¹	LIMITS			UNIT	
			MIN	TYP ²	MAX		
V_{OH}	High-level output voltage	$V_{CC} = \text{MIN}, V_{IL} = \text{MAX},$ $V_{IH} = \text{MIN}, I_{OL} = \text{MAX}$	$\pm 10\%V_{CC}$	2.5		V	
			$\pm 5\%V_{CC}$	2.7	3.4	V	
V_{OL}	Low-level output voltage	$V_{CC} = \text{MIN}, V_{IL} = \text{MAX},$ $V_{IH} = \text{MIN}, I_{OL} = \text{MAX}$	$\pm 10\%V_{CC}$		0.35	0.50	V
			$\pm 5\%V_{CC}$		0.35	0.50	V
V_{IK}	Input clamp voltage	$V_{CC} = \text{MIN}, I_I = I_{IK}$		-0.73	-1.2	V	
I_I	Input current at maximum input voltage	$V_{CC} = \text{MAX}, V_I = 7.0V$			100	μA	
I_{IH}	High-level input current	$V_{CC} = \text{MAX}, V_I = 2.7V$			20	μA	
I_{IL}	Low-level input current	$V_{CC} = \text{MAX}, V_I = 0.5V$			-0.6	mA	
I_{OS}	Short-circuit output current ³	$V_{CC} = \text{MAX}$	-60		-150	mA	
I_{CC}	Supply current (total)	$V_{CC} = \text{MAX}$	I_{CCH}		21	42	mA
			I_{CCL}		33	60	mA

NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at $V_{CC} = 5V, T_{amb} = 25^\circ C$.
- To reduce the effect of external noise during test.
- Not more than one output should be shorted at a time. For testing I_{OS} , the use of High-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

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AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T _{amb} = +25°C V _{CC} = +5V C _L = 50pF, R _L = 500Ω			T _{amb} = 0°C to +70°C V _{CC} = +5V ± 10% C _L = 50pF, R _L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
t _{PLH} t _{PHL}	Propagation delay Dn to Qn	Waveform 2	4.0 3.0	7.0 5.0	9.5 7.0	4.0 2.5	10.0 7.5	ns
t _{PLH} t _{PHL}	Propagation delay E to Qn	Waveform 1	4.5 3.0	8.0 5.0	10.5 7.0	4.5 3.0	12.0 7.5	ns
t _{PLH} t _{PHL}	Propagation delay An to Qn	Waveform 3	5.0 4.5	10.0 8.5	14.0 9.5	5.0 4.0	14.5 10.0	ns
t _{PHL}	Propagation delay MR to Qn	Waveform 4	5.0	7.0	9.0	4.5	10.0	ns

AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T _{amb} = +25°C V _{CC} = +5.0V C _L = 50pF, R _L = 500Ω			T _{amb} = 0°C to +70°C V _{CC} = +5.0V ± 10% C _L = 50pF, R _L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
t _s (H) t _s (L)	Setup time, High or Low Dn to E ₁	Waveform 5	3.0 6.5			3.0 7.0		ns
t _h (H) t _h (L)	Hold time, High or Low Dn to E ₁	Waveform 5	0 0			0 0		ns
t _s (H) t _s (L)	Setup time, High or Low An to E ₁	Waveform 6	2.0 2.0			2.0 2.0		ns
t _h (H) t _h (L)	Hold time, High or Low An to E ₂	Waveform 6	0 0			0 0		ns
t _w (L)	E ₁ Pulse width, Low	Waveform 1	7.5			8.0		ns
t _w (L)	MR Pulse width, Low	Waveform 4	3.0			3.0		ns

NOTES:

1. The Address to Enable setup time is the time before the High-to-Low Enable transition that the Address must be stable so that the correct latch is addressed and the other latches are not affected.
2. The Address to Enable hold time is the time before the Low-to-High Enable transition that the Address must be stable so that the correct latch is addressed and the other latches are not affected.

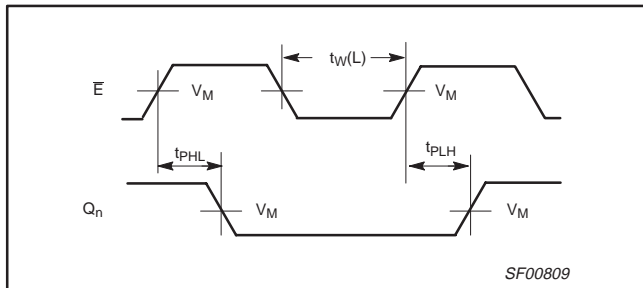
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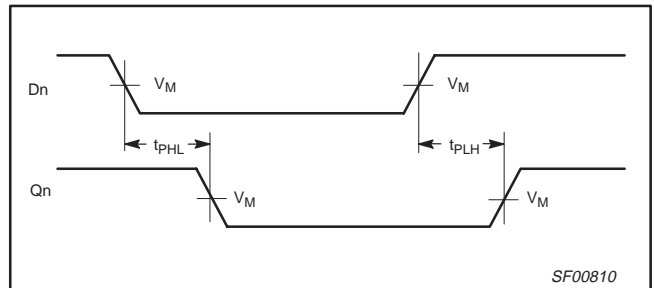
AC WAVEFORMS

For all waveforms, $V_M = 1.5V$.

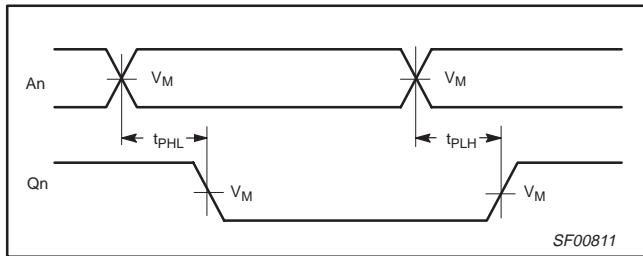
The shaded areas indicate when the input is permitted to change for predictable output performance.



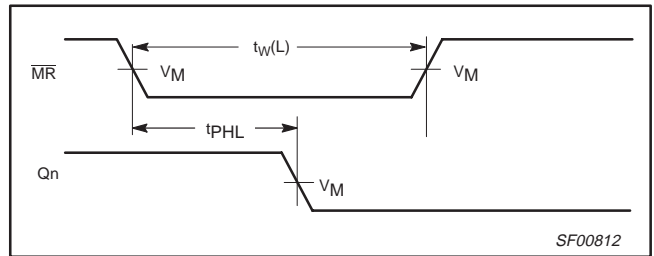
Waveform 1. Propagation Delay, Enable Input to Output, Enable Pulse Width



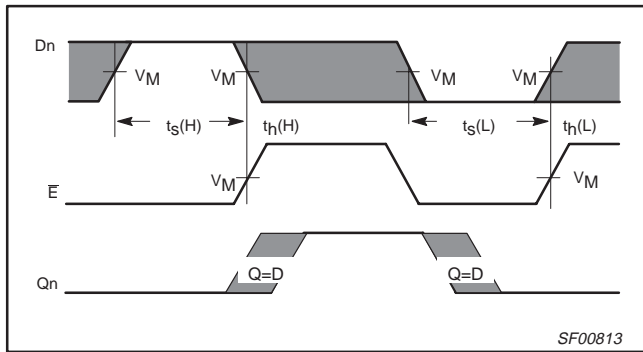
Waveform 2. Propagation Delay, Data to Output



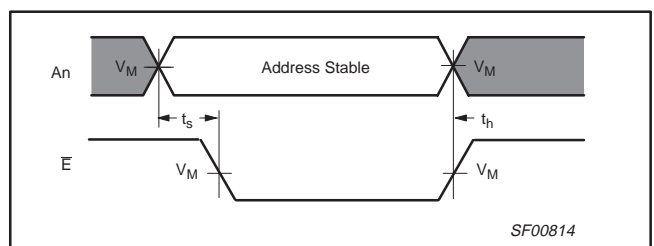
Waveform 3. Propagation Delay Address to Output



Waveform 4. Master Reset Pulse Width and Master Reset to Output Delay



Waveform 5. Data Setup and Hold Times

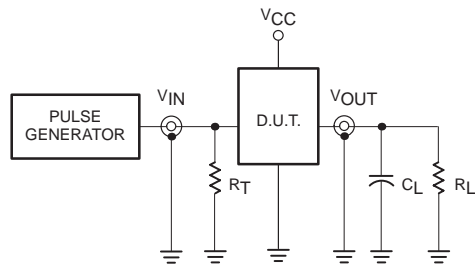


Waveform 6. Address Setup and Hold Times

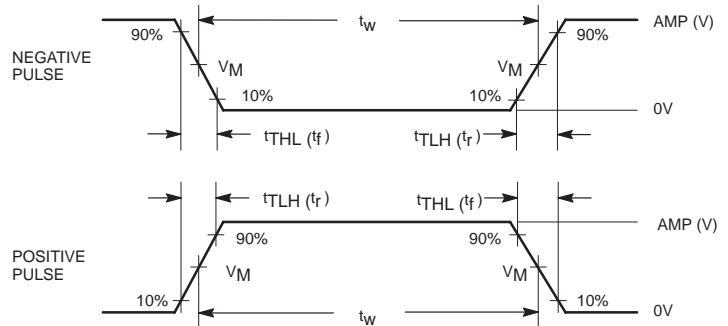
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TEST CIRCUIT AND WAVEFORMS



Test Circuit for Totem-Pole Outputs



Input Pulse Definition

DEFINITIONS:

- R_L = Load resistor; see AC ELECTRICAL CHARACTERISTICS for value.
- C_L = Load capacitance includes jig and probe capacitance; see AC ELECTRICAL CHARACTERISTICS for value.
- R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

family	INPUT PULSE REQUIREMENTS					
	amplitude	V_M	rep. rate	t_w	t_{TLH}	t_{THL}
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns

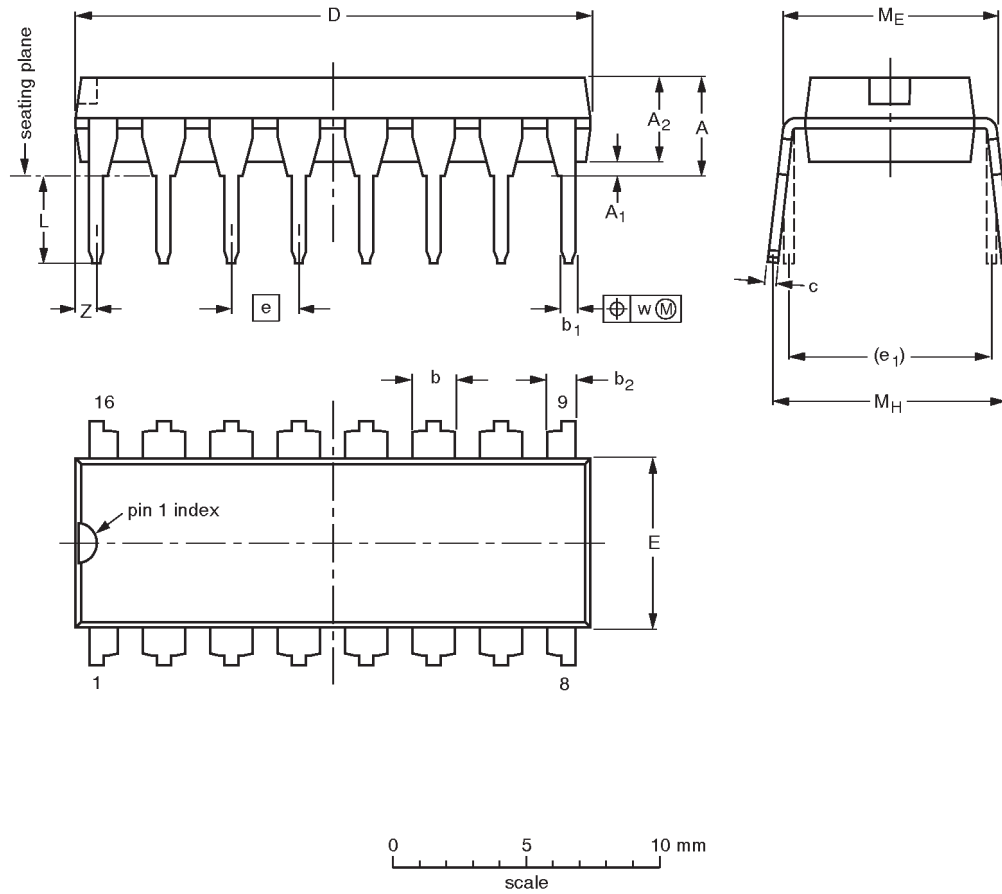
SF00006

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DIP16: plastic dual in-line package; 16 leads (300 mil)

SOT38-4



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A ₁ min.	A ₂ max.	b	b ₁	b ₂	c	D ⁽¹⁾	E ⁽¹⁾	e	e ₁	L	M _E	M _H	w	Z ⁽¹⁾ max.
mm	4.2	0.51	3.2	1.73 1.30	0.53 0.38	1.25 0.85	0.36 0.23	19.50 18.55	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	0.76
inches	0.17	0.020	0.13	0.068 0.051	0.021 0.015	0.049 0.033	0.014 0.009	0.77 0.73	0.26 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.030

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

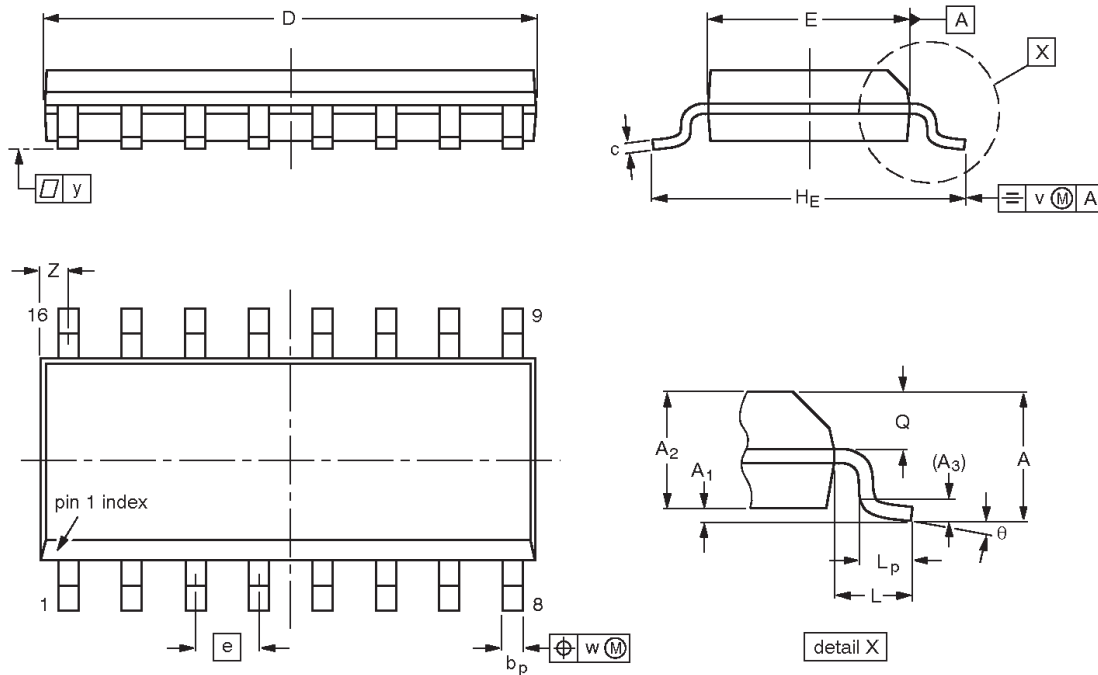
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT38-4						-92-11-17 95-01-14

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SO16: plastic small outline package; 16 leads; body width 3.9 mm

SOT109-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽¹⁾	e	H _E	L	L _p	Q	v	w	y	Z ⁽¹⁾	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	10.0 9.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.39 0.38	0.16 0.15	0.050	0.244 0.228	0.041	0.039 0.016	0.028 0.020	0.01	0.01	0.004	0.028 0.012	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT109-1	076E07S	MS-012AC				95-01-23 97-05-22

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NOTES

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Data sheet status

Data sheet status	Product status	Definition [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
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[1] Please consult the most recently issued datasheet before initiating or completing a design.

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