

# DATA SHEET

## **74F3038**

**Quad 2-input NAND 30  $\Omega$  line driver  
(open collector)**

Product specification  
Supersedes data of 1990 Jan 29  
IC15 Data Handbook

1998 May 21

# Quad 2-input NAND 30Ω line driver (open collector)

# 74F3038

## FEATURES

- 30Ω line driver
- 160mA output drive capability
- High speed
- Facilitates incident wave switching
- 3nh lead inductance each on V<sub>CC</sub> and GND when both side pins are used

## DESCRIPTION

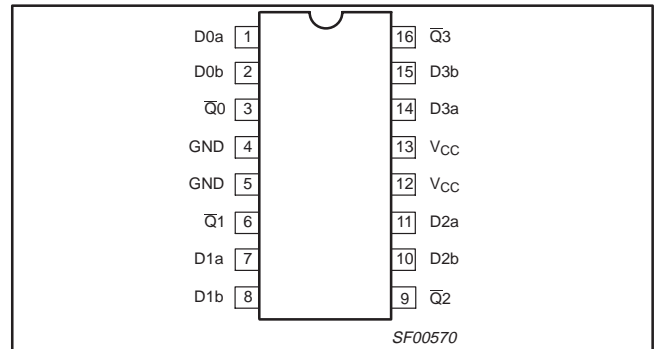
The 74F3038 is a high current Open-Collector Line Driver composed of four 2-input NAND gates. It has been designed to deal with the transmission line effects of PC boards which appear when fast edge rates are used.

The 74F3038 can sink 160mA with a V<sub>CC</sub> as low as 4.5V. This guarantees incident wave switching with V<sub>OL</sub> not more than 0.8V while driving impedances as low as 30Ω. This is applicable with any combination of outputs using continuous duty.

The AC specifications for the 74F3038 were determined using the standard FAST load for open-collector parts of 50pF capacitance, a 500Ω pull-up resistor and a 500Ω pull-down resistor. (See Test Circuit).

Reducing the load resistors to 100Ω will decrease the t<sub>PLH</sub> propagation delay by approximately 50% while increasing t<sub>PHL</sub> only slightly. The graph of typical propagation delay versus load resistor (see AC Characteristics section for Graph) shows a spline fit curve from four measured data points, R<sub>L</sub> = 30Ω, R<sub>L</sub> = 100Ω, R<sub>L</sub> = 300Ω, and R<sub>L</sub> = 500Ω.

## PIN CONFIGURATION



TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F3038	6.0ns	17mA

## ORDERING INFORMATION

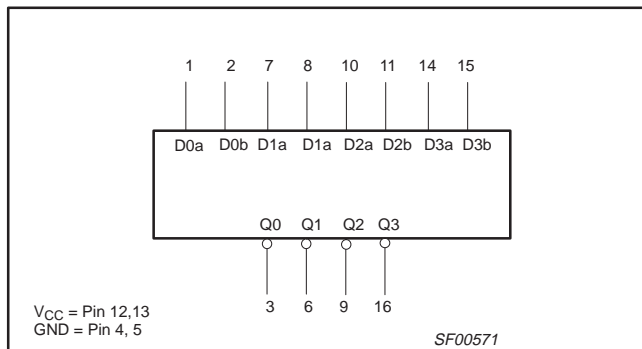
DESCRIPTION	COMMERCIAL RANGE V <sub>CC</sub> = 5V ±10%, T <sub>amb</sub> = 0°C to +70°C	PACKAGE DRAWING NUMBER
16-pin Plastic DIP	N74F3038N	SOT38-4
16-pin Plastic SOL	N74F3038D	SOT162-1

## INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

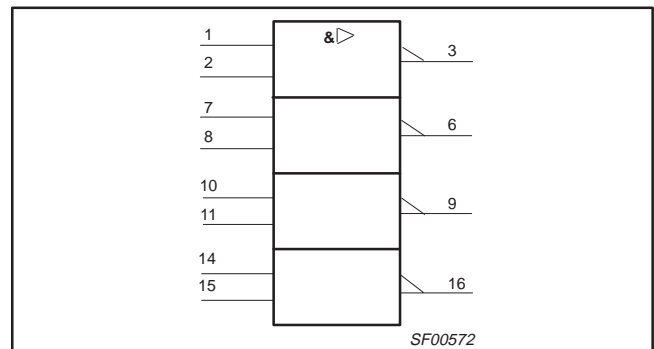
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
Dna, Dnb	Data inputs	1.0/1.0	20μA/0.6mA
Qn	Data outputs	OC/266	OC/160mA

**NOTE:** One (1.0) FAST unit load is defined as: 20μA in the High state and 0.6mA in the Low state. OC = Open Collector.

## LOGIC SYMBOL



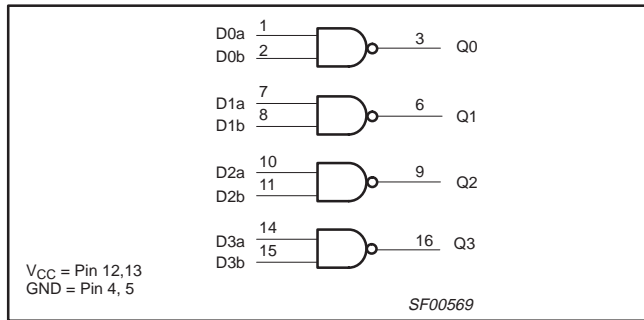
## IEC/IEEE SYMBOL



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## LOGIC DIAGRAM



## FUNCTION TABLE

INPUTS		OUTPUT
Dna	Dnb	$\bar{Q}_n$
L	L	H
L	H	H
H	L	H
H	H	L

H = High voltage level  
 L = Low voltage level

## ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
$V_{CC}$	Supply voltage	-0.5 to +7.0	V
$V_{IN}$	Input voltage	-0.5 to +7.0	V
$I_{IN}$	Input current	-30 to +5	mA
$V_{OUT}$	Voltage applied to output in High output state	-0.5 to $V_{CC}$	V
$I_{OUT}$	Current applied to output in Low output state	320	mA
$T_{amb}$	Operating free-air temperature range	0 to +70	°C
$T_{stg}$	Storage temperature range	-65 to +150	°C

## RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN	NOM	MAX	
$V_{CC}$	Supply voltage	4.5	5.0	5.5	V
$V_{IH}$	High-level input voltage	2.0			V
$V_{IL}$	Low-level input voltage			0.8	V
$I_{IK}$	Input clamp current			-18	mA
$V_{OH}$	High-level output voltage			4.5	V
$I_{OL}$	Low-level output current			160	mA
$T_{amb}$	Operating free-air temperature range	0		+70	°C

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## DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS <sup>1</sup>	LIMITS			UNIT	
			MIN	TYP <sup>2</sup>	MAX		
I <sub>OH</sub>	High-level output current	V <sub>CC</sub> = MIN, V <sub>IL</sub> = MAX, V <sub>IH</sub> = MIN, V <sub>OH</sub> = MAX			250	μA	
V <sub>OL</sub>	Low-level output current	V <sub>CC</sub> = MIN V <sub>IL</sub> = MAX V <sub>IH</sub> = MIN	I <sub>OL</sub> = 100mA	±10% V <sub>CC</sub>	0.42	0.55	V
			I <sub>OL</sub> = 160mA <sup>3</sup>	±5% V <sub>CC</sub>		0.80	V
V <sub>IK</sub>	Input clamp voltage	V <sub>CC</sub> = MIN, I <sub>I</sub> = I <sub>IK</sub>		-0.73	-1.2	V	
I <sub>I</sub>	Input current at maximum input voltage	V <sub>CC</sub> = MAX, V <sub>I</sub> = 7.0V			100	μA	
I <sub>IH</sub>	High-level input current	V <sub>CC</sub> = MAX, V <sub>I</sub> = 2.7V			20	μA	
I <sub>IL</sub>	Low-level input current	V <sub>CC</sub> = MAX, V <sub>I</sub> = 0.5V			-0.6	mA	
I <sub>CC</sub>	Supply current (total)	V <sub>CC</sub> = MAX	V <sub>IN</sub> = GND		3.5	6.0	mA
			V <sub>IN</sub> = 4.5V		30	40	mA

**NOTES:**

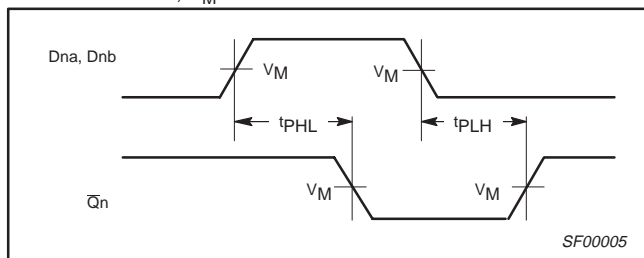
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V<sub>CC</sub> = 5V, T<sub>amb</sub> = 25°C.
3. I<sub>OL1</sub> is the current necessary to guarantee the High to Low transition in a 30Ω transmission line on the incident wave.

## AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T <sub>amb</sub> = +25°C V <sub>CC</sub> = +5.0V C <sub>L</sub> = 50pF, R <sub>L</sub> = 500Ω			T <sub>amb</sub> = 0°C to +70°C V <sub>CC</sub> = +5.0V ± 10% C <sub>L</sub> = 50pF, R <sub>L</sub> = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation delay D <sub>na</sub> , D <sub>nb</sub> to Q <sub>n</sub>	Waveform 1	6.0 1.0	8.5 2.0	11.5 5.0	6.0 1.0	12.0 5.0	ns

## AC WAVEFORMS

For all waveforms, V<sub>M</sub> = 1.5V.

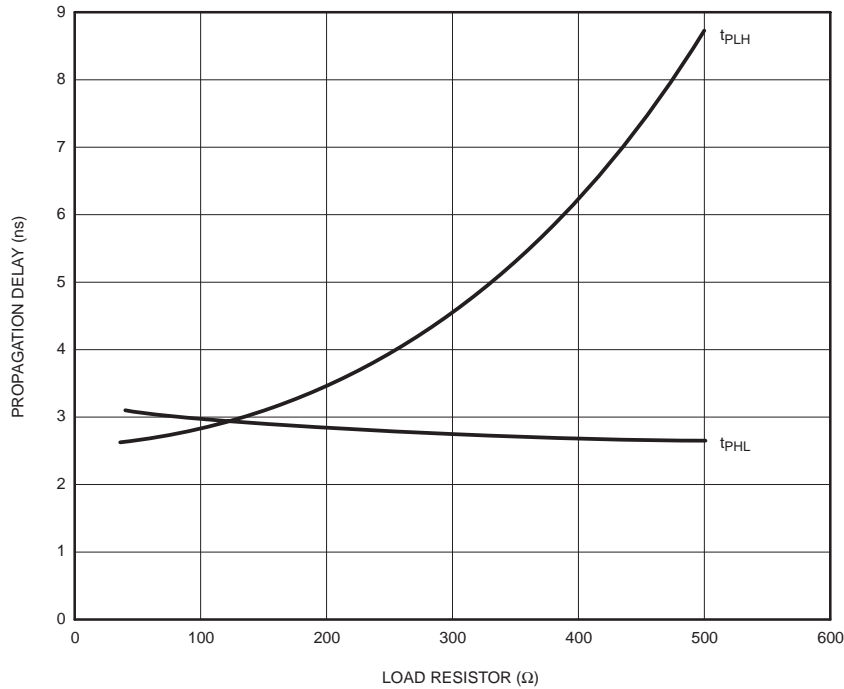


Waveform 1. Propagation Delay for Inputs to Output

# Quad 2-input NAND 30Ω line driver (open collector)

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## TYPICAL PROPAGATION DELAYS VERSUS LOAD FOR OPEN COLLECTOR OUTPUTS

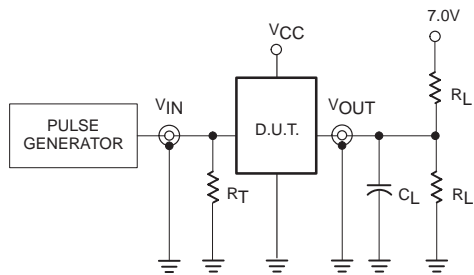


**NOTE:**

When using Open-Collector parts, the value of the pull-up resistor greatly affects the value of the t<sub>PLH</sub>. For example, changing the specified pull-up resistor value from 500Ω to 100Ω will improve the t<sub>PLH</sub> up to 50% with only a slight increase in the t<sub>PHL</sub>. However, if the value of the pull-up resistor is changed, the user must make certain that the total I<sub>OL</sub> current through the resistor and the total I<sub>IL</sub>s of the receivers does not exceed the I<sub>OL</sub> maximum specification.

SF01361

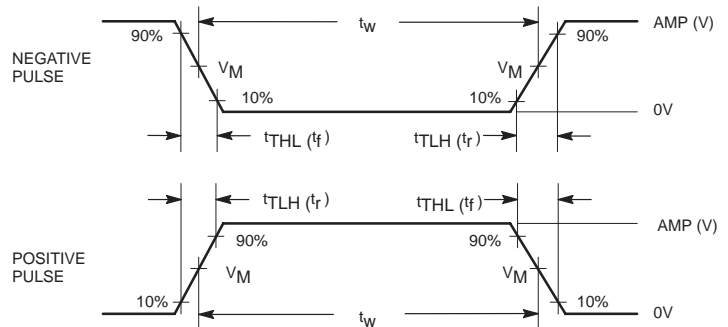
## TEST CIRCUIT AND WAVEFORMS



Test Circuit for Open Collector Outputs

**DEFINITIONS:**

- R<sub>L</sub> = Load resistor; see AC electrical characteristics for value.
- C<sub>L</sub> = Load capacitance includes jig and probe capacitance; see AC electrical characteristics for value.
- R<sub>T</sub> = Termination resistance should be equal to Z<sub>OUT</sub> of pulse generators.



Input Pulse Definition

family	INPUT PULSE REQUIREMENTS					
	amplitude	V <sub>M</sub>	rep. rate	t <sub>w</sub>	t <sub>TLH</sub>	t <sub>THL</sub>
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns

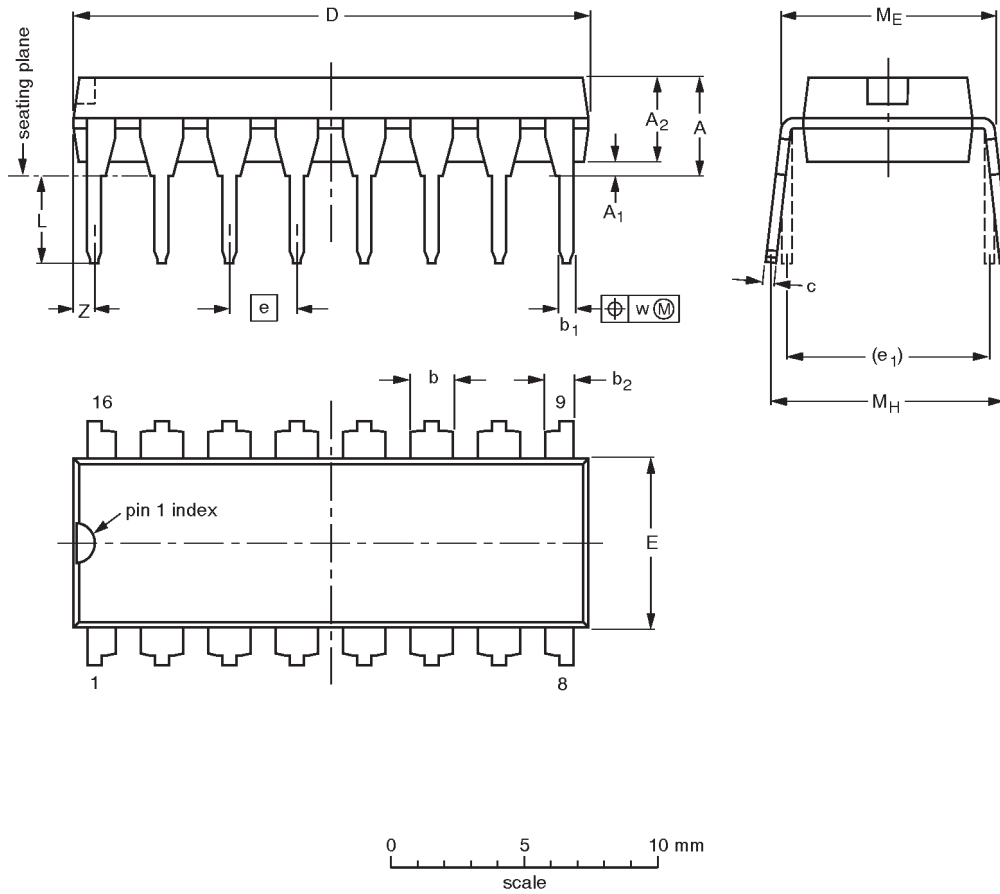
SF00027

Quad 2-input NAND 30 Ω line driver (open collector)

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DIP16: plastic dual in-line package; 16 leads (300 mil)

SOT38-4



**DIMENSIONS** (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A <sub>1</sub> min.	A <sub>2</sub> max.	b	b <sub>1</sub>	b <sub>2</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	e <sub>1</sub>	L	M <sub>E</sub>	M <sub>H</sub>	w	Z <sup>(1)</sup> max.
mm	4.2	0.51	3.2	1.73 1.30	0.53 0.38	1.25 0.85	0.36 0.23	19.50 18.55	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	0.76
inches	0.17	0.020	0.13	0.068 0.051	0.021 0.015	0.049 0.033	0.014 0.009	0.77 0.73	0.26 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.030

**Note**

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

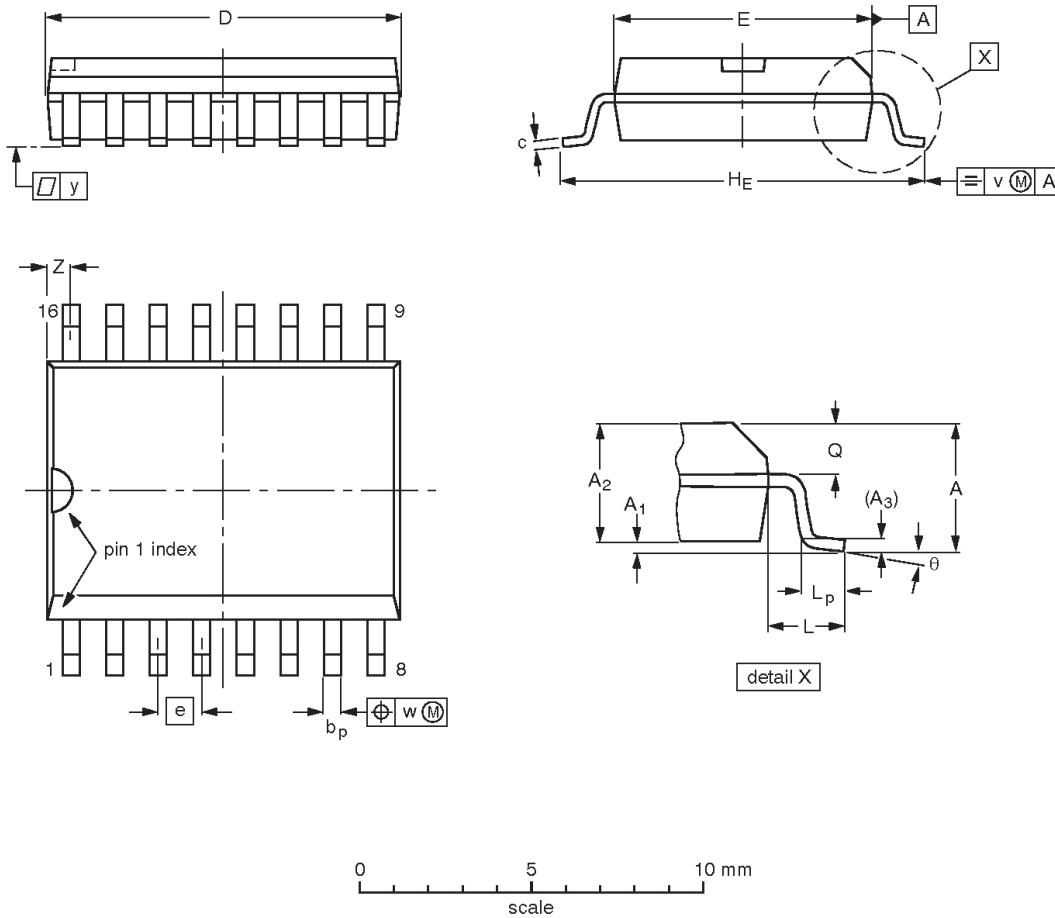
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT38-4						-92-11-17 95-01-14

Quad 2-input NAND 30 Ω line driver (open collector)

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SO16: plastic small outline package; 16 leads; body width 7.5 mm

SOT162-1



**DIMENSIONS (inch dimensions are derived from the original mm dimensions)**

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	z <sup>(1)</sup>	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	10.5 10.1	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8° 0°
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.41 0.40	0.30 0.29	0.050	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

**Note**

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT162-1	075E03	MS-013AA				95-01-24 97-05-22

Quad 2-input NAND 30  $\Omega$  line driver (open collector)

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## Data sheet status

Data sheet status	Product status	Definition [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
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[1] Please consult the most recently issued datasheet before initiating or completing a design.

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