

74F579 8-Bit Bidirectional Binary Counter with 3-STATE Outputs

General Description

The 74F579 is a fully synchronous 8-stage up/down counter with multiplexed 3-STATE I/O ports for bus-oriented applications. It features a preset capability for programmable operation, carry lookahead for easy cascading and a U/D input to control the direction of counting. All state changes, whether in counting or parallel loading, are initiated by the rising edge of the clock.

Features

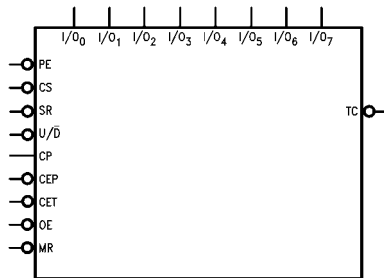
- Multiplexed 3-STATE I/O ports
- Built-in lookahead carry capability
- Count frequency 100 MHz typical
- Supply current 75 mA typical
- Guaranteed 4000V minimum ESD protection

Ordering Code:

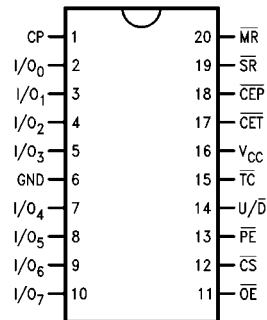
Order Number	Package Number	Package Description
74F579SC	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide
74F579SJ	M20D	20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74F579PC	N20A	20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Logic Symbol



Connection Diagram



Unit Loading/Fan Out

Pin Names	Description	U.L. HIGH/LOW	Input I_{IH}/I_{IL} Output I_{OH}/I_{OL}
I/O_0 – I/O_7	Data Inputs or 3-STATE Outputs	3.5/0.333 75/15	70 μ A/–0.2 mA –3 mA/24 mA
\overline{PE}	Parallel Enable Input (Active LOW)	0.25/0.333	5 μ A/–0.2 mA
U/\overline{D}	Up-Down Count Control Input	0.25/0.333	5 μ A/–0.2 mA
\overline{MR}	Master Reset Input (Active LOW)	0.25/0.333	5 μ A/–0.2 mA
\overline{SR}	Synchronous Reset Input (Active LOW)	0.25/0.333	5 μ A/–0.2 mA
\overline{CEP}	Count Enable Parallel Input (Active LOW)	0.25/0.333	5 μ A/–0.2 mA
\overline{CET}	Count Enable Trickle Input (Active LOW)	0.25/0.333	5 μ A/–0.2 mA
\overline{CS}	Chip Select Input Active (Active LOW)	0.25/0.333	5 μ A/–0.2 mA
\overline{OE}	Output Enable Input (Active LOW)	0.25/0.333	5 μ A/–0.2 mA
CP	Clock Pulse Input (Active Rising Edge)	0.25/0.333	5 μ A/–0.2 mA
\overline{TC}	Terminal Count Output (Active LOW)	25/12.5	–1 mA/5 mA

Function Table

\overline{MR}	\overline{SR}	\overline{CS}	\overline{PE}	\overline{CEP}	\overline{CET}	U/\overline{D}	\overline{OE}	CP	Function
X	X	H	X	X	X	X	X	X	I/O_a to I/O_h in High Z (\overline{PE} Disabled)
X	X	L	H	X	X	X	H	X	I/O_a to I/O_h in High Z
X	X	L	H	X	X	X	L	X	Flip-Flop Outputs Appear on I/O Lines
L	X	X	X	X	X	X	X	X	Asynchronous Reset for all Flip-Flops
H	L	X	X	X	X	X	X	\nearrow	Synchronous Reset for all Flip-Flops
H	H	L	L	X	X	X	X	\nearrow	Parallel Load all Flip-Flops
H	H	(Not LL)	H	X	X	X	X	\nearrow	Hold
H	H	(Not LL)	X	H	X	X	X	\nearrow	Hold (\overline{TC} Held HIGH)
H	H	(Not LL)	L	L	H	X	X	\nearrow	Count Up
H	H	(Not LL)	L	L	L	X	X	\nearrow	Count Down

H = HIGH Voltage Level

L = LOW Voltage Level

X = Immaterial

 \nearrow = LOW to HIGH Clock TransitionNot LL = \overline{CS} and \overline{PE} should never both be LOW voltage level at the same time.

Absolute Maximum Ratings (Note 1)

Storage Temperature	-65°C to +150°C
Ambient Temperature under Bias	-55°C to +125°C
Junction Temperature under Bias	-55°C to +150°C
V _{CC} Pin Potential to Ground Pin	-0.5V to +7.0V
Input Voltage (Note 2)	-0.5V to +7.0V
Input Current (Note 2)	-30 mA to +5.0 mA
Voltage Applied to Output in HIGH State (with V _{CC} = 0V)	
Standard Output	-0.5V to V _{CC}
3-STATE Output	-0.5V to +5.5V
Current Applied to Output in LOW State (Max)	twice the rated I _{OL} (mA)
ESD Last Passing Voltage (Min)	4000V

Recommended Operating Conditions

Free Air Ambient Temperature	0°C to +70°C
Supply Voltage	+4.5V to +5.5V

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

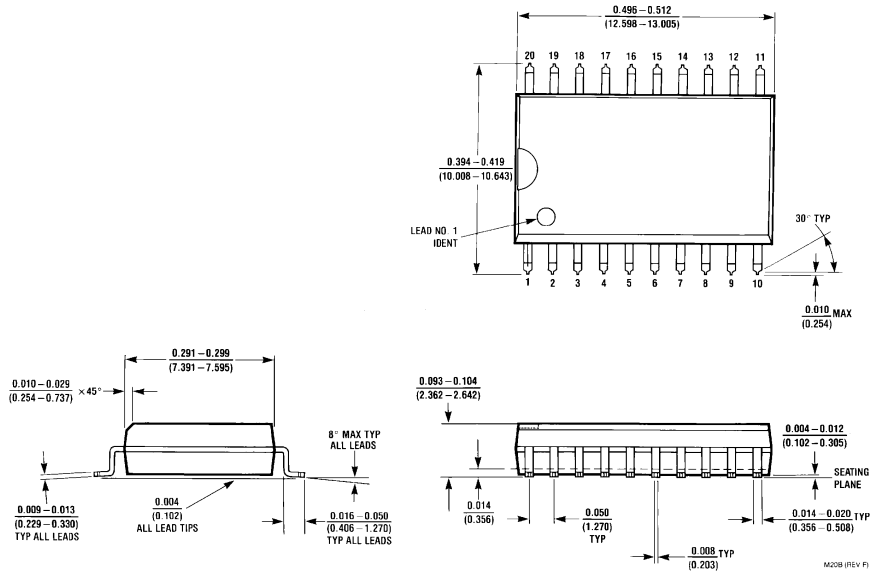
DC Electrical Characteristics

Symbol	Parameter	Min	Typ	Max	Units	V _{CC}	Conditions
V _{IH}	Input HIGH Voltage	2.0			V		Recognized as a HIGH Signal
V _{IL}	Input LOW Voltage			0.8	V		Recognized as a LOW Signal
V _{CD}	Input Clamp Diode Voltage			-1.2	V	Min	I _{IN} = -18 mA
V _{OH}	Output HIGH Voltage	10% V _{CC} 5% V _{CC}	2.4 2.7		V	Min	I _{OH} = -3 mA
V _{OL}	Output LOW Voltage	10% V _{CC} 5% V _{CC}		0.5 0.5	V	Min	I _{OL} = 20 mA ($\overline{\text{TC}}$), I _{OL} = 24 mA (I/O _n) I _{OL} = 20 mA ($\overline{\text{TC}}$), I _{OL} = 24 mA (I/O _n)
I _{IH}	Input HIGH Current			5.0	μA	Max	V _{IN} = 2.7V (Non-I/O Pins)
I _{BVI}	Input HIGH Current Breakdown Test			7.0	μA	Max	V _{IN} = 7.0V (Non-I/O Pins)
I _{BVIT}	Input HIGH Current Breakdown (I/O)			0.5	mA	Max	V _{IN} = 5.5V (I/O _n)
I _{CEX}	Output HIGH Leakage Current			50	μA	Max	V _{OUT} = V _{CC}
V _{ID}	Input Leakage Test	4.75			V	0.0	I _{ID} = 1.9 μA All Other Pins Grounded
I _{OD}	Output Leakage Circuit Control			3.75	μA	0.0	V _{IOD} = 150 mV All Other Pins Grounded
I _{ZZ}	Bus Drainage Test			500	μA	0.0	V _{OUT} = 5.25V
I _{IL}	Input LOW Current			-0.2	mA	Max	V _{IN} = 0.5V (Non-I/O Pins)
I _{IH} & I _{OZH}	Output Leakage Current			70	μA	Max	V _{OUT} = 2.7V (I/O _n)
I _{IL} & I _{OZL}	Output Leakage Current			-200	μA	Max	V _{OUT} = 0.5V (I/O _n)
I _{OS}	Output Short-Circuit Current	-60		-150	mA	Max	V _{OUT} = 0V
I _{CCH}	Power Supply Current		70	110	mA	Max	V _O = HIGH
I _{CCL}	Power Supply Current		85	120	mA	Max	V _O = LOW
I _{CCZ}	Power Supply Current		85	125	mA	Max	V _O = HIGH Z

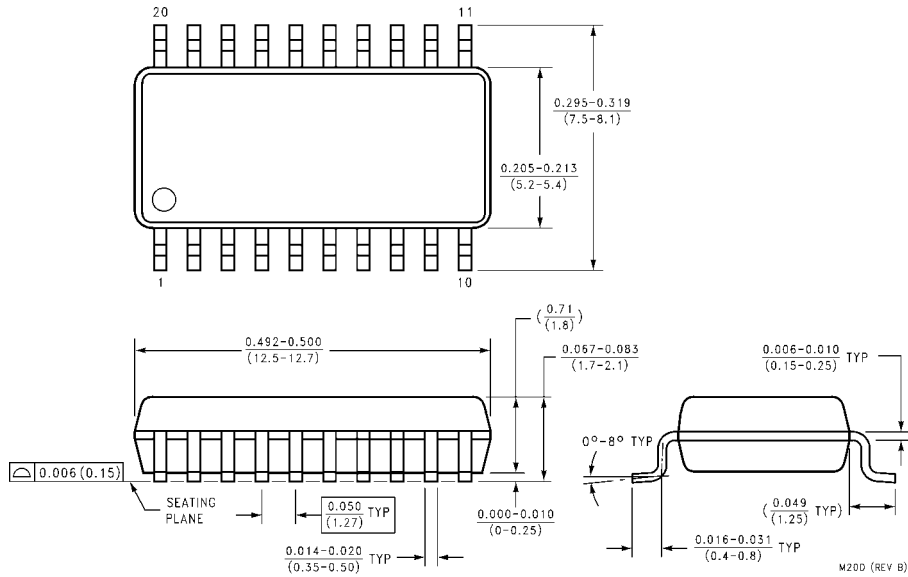
AC Electrical Characteristics							
Symbol	Parameter	T _A = +25°C V _{CC} = +5.0V C _L = 50 pF			T _A = 0°C to +70°C V _{CC} = +5.0V C _L = 50 pF		Units
		Min	Typ	Max	Min	Max	
t _{MAX}	Maximum Clock Frequency	70	85		80		
t _{PLH}	Propagation Delay	3.0	5.0	7.5	3.0	8.0	ns
t _{PHL}	CP to I/O _n	5.0	8.0	11.5	5.0	11.5	
t _{PLH}	Propagation Delay	5.0	7.5	11.5	5.0	12.0	ns
t _{PHL}	CP to \overline{TC}	5.0	7.0	11.5	5.0	12.0	
t _{PLH}	Propagation Delay	4.5	7.0	9.0	4.5	10.0	ns
t _{PHL}	U/ \overline{D} to \overline{TC}	4.5	8.0	9.5	4.5	10.0	
t _{PLH}	Propagation Delay	2.5	3.8	6.0	2.5	6.5	ns
t _{PHL}	\overline{CEP} or \overline{CET} to \overline{TC}	3.5	6.0	8.0	3.5	8.5	
t _{PHL}	Propagation Delay	5.0	7.5	10.0	5.0	10.0	ns
t _{PHL}	Propagation Delay	6.5	10.0	13.0	6.5	13.5	ns
t _{PZH}	Output Enable Time	3.0	5.0	8.5	3.0	9.0	ns
t _{PZL}	\overline{CS} or \overline{PE} to I/O	5.5	8.0	10.5	5.5	11.5	
t _{PHZ}	Output Disable Time	2.0	5.0	8.5	2.0	9.0	ns
t _{PLZ}	\overline{CS} or \overline{PE} to I/O	2.0	4.5	8.0	2.0	8.5	
t _{PZH}	Output Enable Time	3.0	5.0	8.0	3.0	8.5	ns
t _{PZL}	\overline{OE} to I/O _n	5.0	8.0	11.0	5.0	12.0	
t _{PHZ}	Output Disable Time	2.0	4.0	6.5	2.0	6.5	ns
t _{PLZ}	\overline{OE} to I/O _n	2.0	4.0	6.0	2.0	6.5	

AC Operating Requirements							
Symbol	Parameter	T _A = +25°C V _{CC} = +5.0V			T _A = 0°C to +70°C V _{CC} = +5.0V		Units
		Min	Typ	Max	Min	Max	
t _S (H)	Setup Time	4.0			4.0		ns
t _S (L)	I/O _n to CP	4.0			4.0		
t _H (H)	Hold Time	0.0			0.0		ns
t _H (L)	I/O _n to CP	0.0			0.0		
t _S (H)	Setup Time	9.5			9.5		ns
t _S (L)	\overline{PE} , \overline{CS} or \overline{SR} to CP	9.5			9.5		
t _H (H)	Hold Time	0.0			0.0		ns
t _H (L)	\overline{PE} , \overline{CS} or \overline{SR} to CP	0.0			0.0		
t _S (H)	Setup Time	6.5			6.5		ns
t _S (L)	\overline{CET} or \overline{CEP} to CP	9.5			9.5		
t _H (H)	Hold Time	0.0			0.0		ns
t _H (L)	\overline{CET} or \overline{CEP} to CP	0.0			0.0		
t _S (H)	Setup Time	9.0			9.5		ns
t _S (L)	U/ \overline{D} to CP	9.0			9.5		
t _H (H)	Hold Time	0.0			0.0		ns
t _H (L)	U/ \overline{D} to CP	0.0			0.0		
t _W (H)	Clock Pulse Width	4.5			4.5		ns
t _W (L)	HIGH or LOW	4.5			4.5		
t _W (L)	\overline{MR} Pulse Width	3.0			3.0		ns
t _{REC}	Recovery Time	4.0			4.0		ns
	\overline{MR} to CP						

Physical Dimensions inches (millimeters) unless otherwise noted

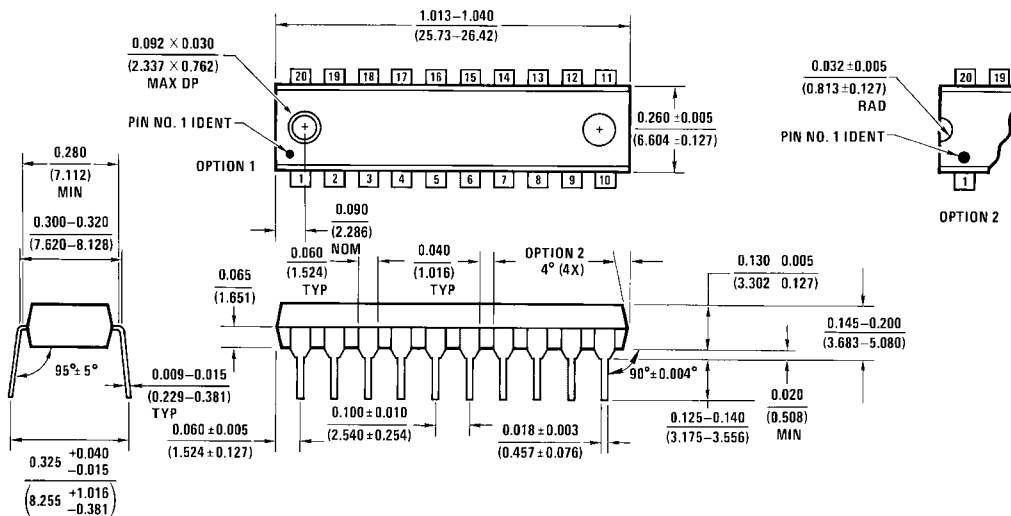


20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide Package Number M20B



20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide Package Number M20D

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



**20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide
Package Number N20A**

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