

BIPOLAR ANALOG INTEGRATED CIRCUIT

μ PC4072

J-FET INPUT LOW-NOISE DUAL OPERATIONAL AMPLIFIER

DESCRIPTION

The μ PC4072 is a J-FET input operational amplifier. This product is designed as low noise version of the μ PC4082. The features of the μ PC4072 are more improved input equivalent noise voltage, input offset voltage and input bias current than those of μ PC4082. By these features, the μ PC4072 is excellent choice for wide variety of applications including audio preamplifier and active filter.

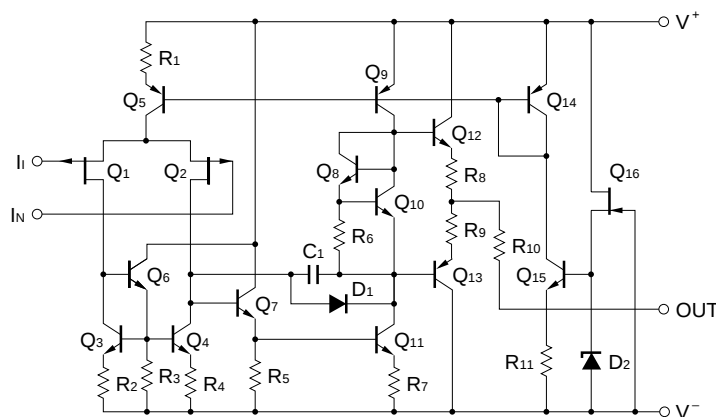
FEATURES

- Low noise: $e_n = 17 \text{ nV}/\sqrt{\text{Hz}}$ (TYP.)
- Very low input bias and offset currents
- Output short circuit protection
- High input impedance...J-FET Input stage
- Internal frequency compensation
- High slew rate...13 V/ μ s (TYP.)

ORDERING INFORMATION

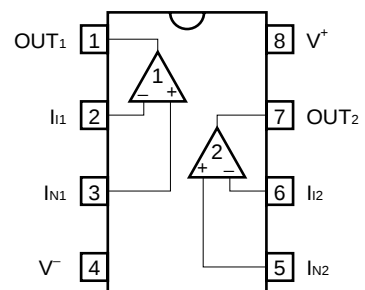
Part Number	Package
μ PC4072C	8-pin plastic DIP (7.62 mm (300))
μ PC4072G2	8-pin plastic SOP (5.72 mm (225))
μ PC4072HA	9-pin plastic slim SIP

EQUIVALENT CIRCUIT (1/2 Circuit)

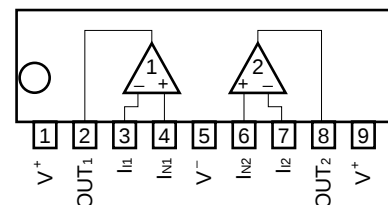


PIN CONFIGURATION (Top View)

μ PC4072C, 4072G2



μ PC4072HA



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Not all devices/types available in every country. Please check with local NEC representative for availability and additional information.

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C)

Parameter		Symbol	Ratings	Unit
Voltage between V ⁺ and V ⁻ ^{Note 1}		V ⁺ – V ⁻	–0.3 to +36	V
Differential Input Voltage		V _{ID}	±30	V
Input Voltage ^{Note 2}		V _I	V ⁻ –0.3 to V ⁺ +0.3	V
Output Voltage ^{Note 3}		V _O	V ⁻ –0.3 to V ⁺ +0.3	V
Power Dissipation	C Package ^{Note 4}	P _T	350	mW
	G2 Package ^{Note 5}		440	mW
	HA Package ^{Note 4}		350	mW
Output Short Circuit Duration ^{Note 6}			Indefinite	sec
Operating Ambient Temperature		T _A	–20 to +80	°C
Storage Temperature		T _{stg}	–55 to +125	°C

Notes 1. Reverse connection of supply voltage can cause destruction.

2. The input voltage should be allowed to input without damage or destruction. Even during the transition period of supply voltage, power on/off etc., this specification should be kept. The normal operation will establish when the both inputs are within the Common Mode Input Voltage Range of electrical characteristics.
3. This specification is the voltage which should be allowed to supply to the output terminal from external without damage or destructive. Even during the transition period of supply voltage, power on/off etc., this specification should be kept. The output voltage of normal operation will be the Output Voltage Swing of electrical characteristics.
4. Thermal derating factor is –5.0 mW/°C when operating ambient temperature is higher than 55°C.
5. Thermal derating factor is –4.4 mW/°C when operating ambient temperature is higher than 25°C.
6. Pay careful attention to the total power dissipation not to exceed the absolute maximum ratings, Note 4 and Note 5.

RECOMMENDED OPERATING CONDITIONS

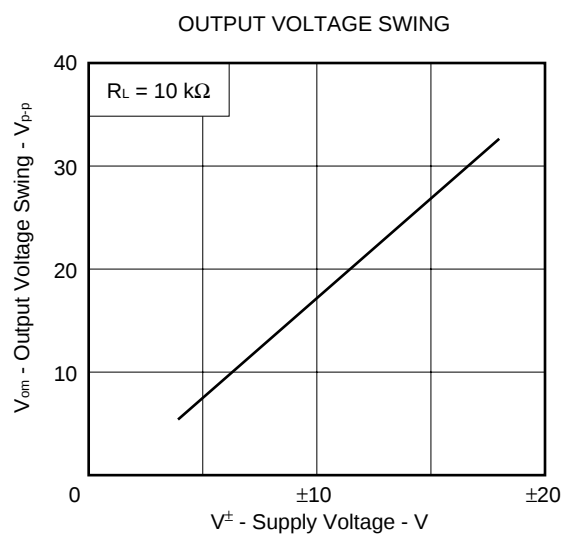
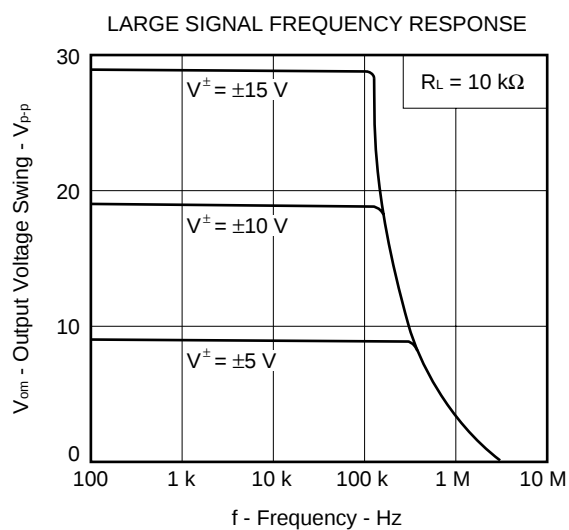
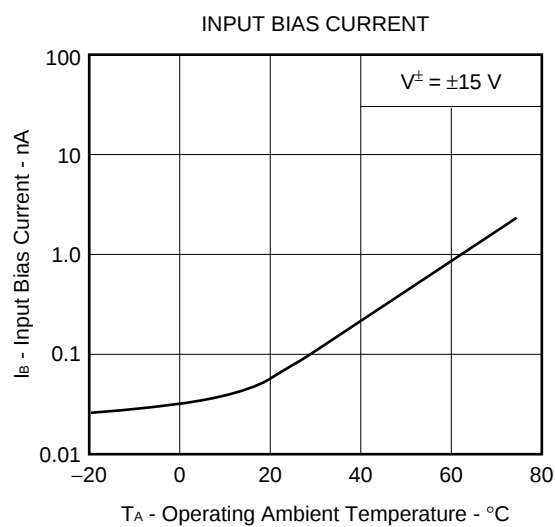
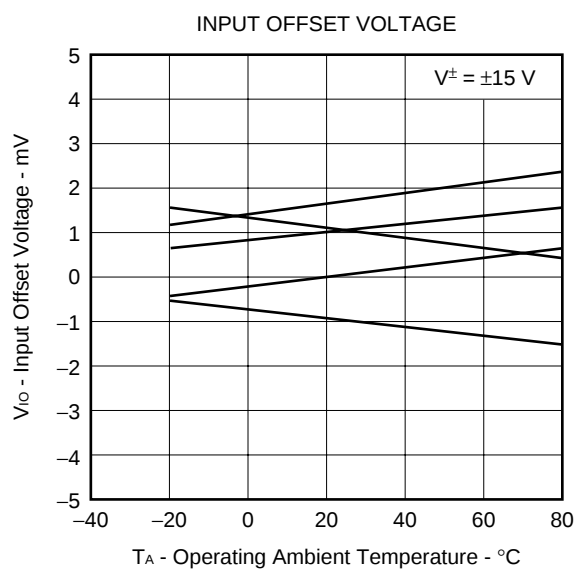
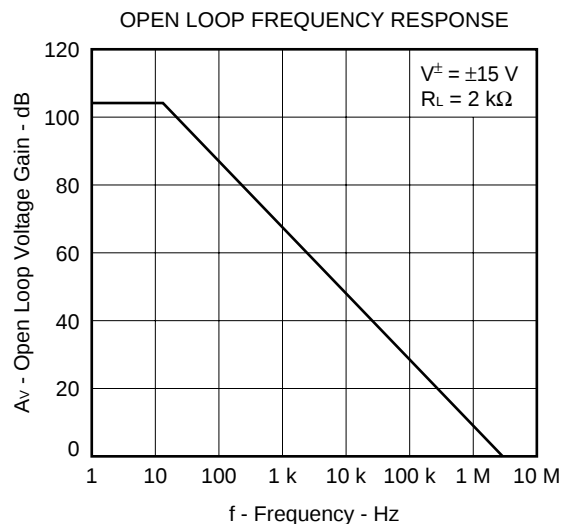
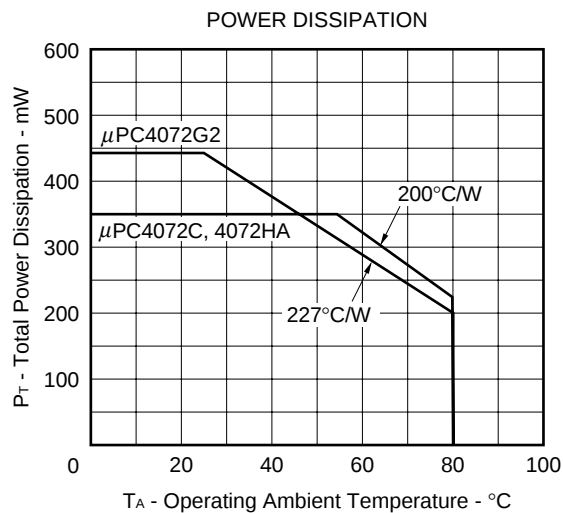
Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Supply Voltage	V [±]	±5		±16	V
Output Current	I _O			±10	mA
Capacitive Load (A _v = +1, R _f = 0 Ω)	C _L			100	pF

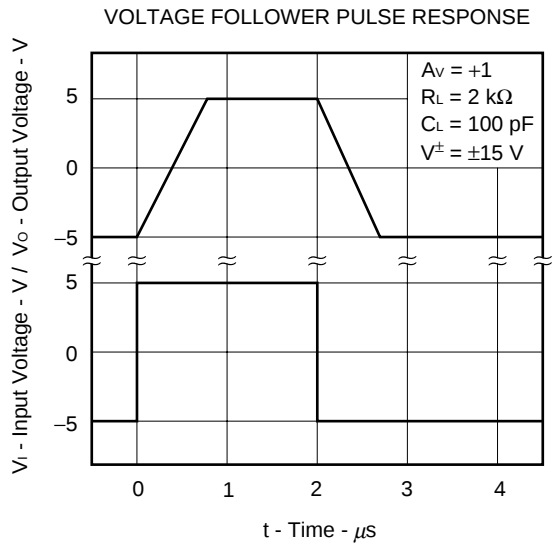
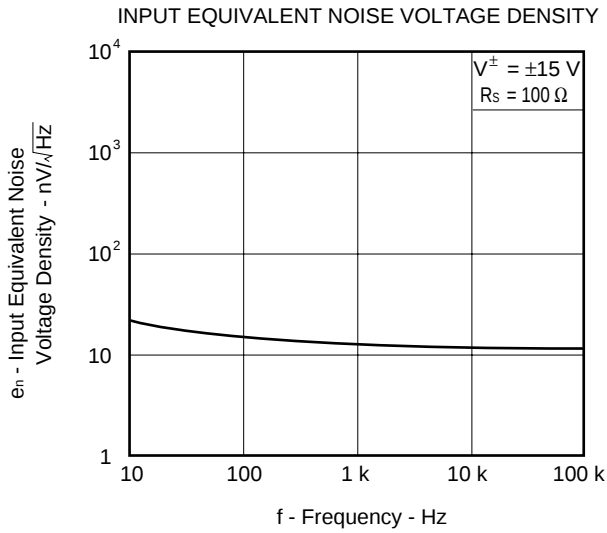
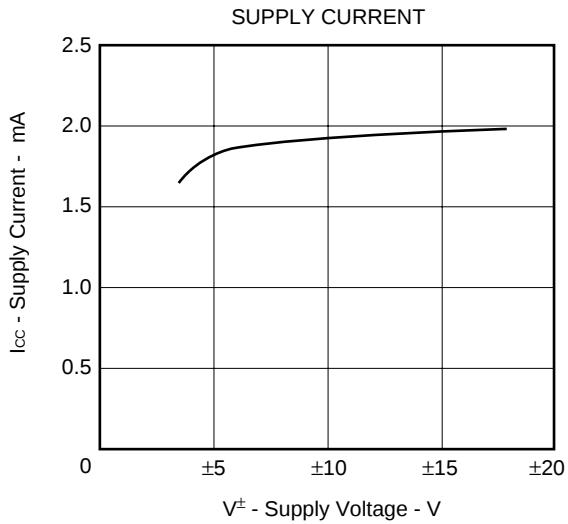
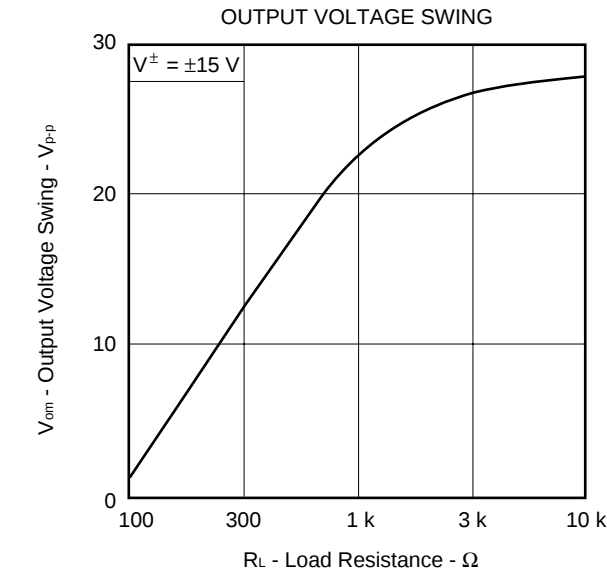
ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$, $V^\pm = \pm 15\text{ V}$)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input Offset Voltage	V_{IO}	$R_S \leq 50\ \Omega$		± 3	± 10	mV
Input Offset Current ^{Note 7}	I_{IO}			± 5	± 50	pA
Input Bias Current ^{Note 7}	I_B			30	200	pA
Large Signal Voltage Gain	A_v	$R_L \geq 2\ \text{k}\Omega$, $V_O = \pm 10\text{ V}$	25000	200000		
Supply Current	I_{CC}	$I_O = 0\text{ A}$, Both Amplifiers		4	5	mA
Common Mode Rejection Ratio	CMR		70	86		dB
Supply Voltage Rejection Ratio	SVR		70	86		dB
Output Voltage Swing	V_{om}	$R_L \geq 10\ \text{k}\Omega$	± 12	± 13.5		V
		$R_L \geq 2\ \text{k}\Omega$	± 10	± 12		V
Common Model Input Voltage Range	V_{ICM}		± 10			V
Slew Rate	SR	$A_v = 1$		13		V/ μs
Unity Gain Frequency	f_{unity}			3		MHz
Input Equivalent Noise Voltage	V_n	$R_S = 100\ \Omega$, $f = 10\text{ Hz to }10\text{ kHz}$		4		$\mu\text{V}_{r.m.s.}$
Input Equivalent Noise Voltage Density	e_n	$R_S = 100\ \Omega$, $f = 1\text{ kHz}$		17		nV/ $\sqrt{\text{Hz}}$
Channel Separation				120		dB
Input Offset Voltage	V_{IO}	$R_S \leq 50\ \Omega$, $T_A = -20\text{ to }+70^\circ\text{C}$			± 13	mV
Average V_{IO} Temperature Drift	$\Delta V_{IO}/\Delta T$	$T_A = -20\text{ to }+70^\circ\text{C}$		± 10		$\mu\text{V}/^\circ\text{C}$
Input Offset Current ^{Note 7}	I_{IO}	$T_A = -20\text{ to }+70^\circ\text{C}$			± 2	nA
Input Bias Current ^{Note 7}	I_B	$T_A = -20\text{ to }+70^\circ\text{C}$			7	nA

Notes 7. Input bias currents flow into IC. Because each currents are gate leak current of P-channel J-FET on input stage. And that are temperature sensitive. Short time measuring method is recommendable to maintain the junction temperature close to the operating ambient temperature.

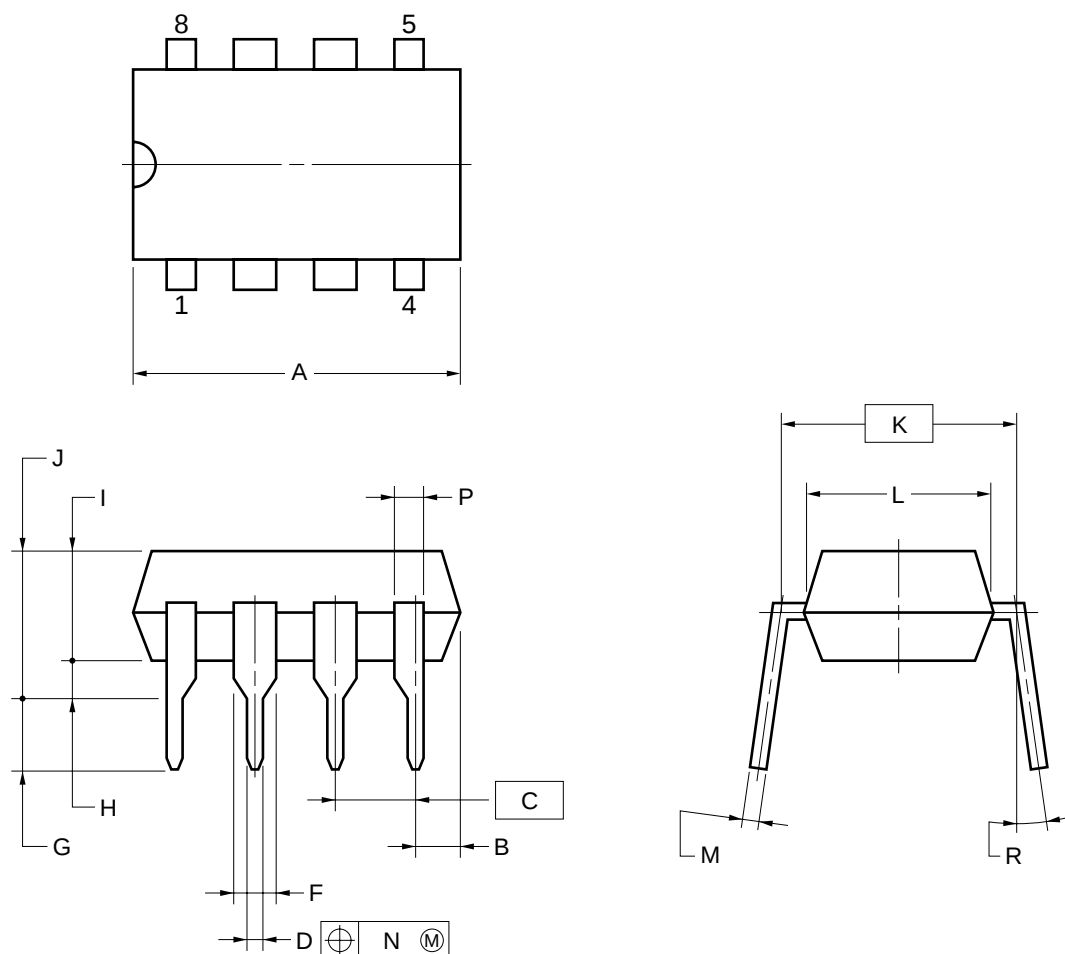
TYPICAL PERFORMANCE CHARACTERISTICS ($T_A = 25^\circ\text{C}$, TYP.)





★ PACKAGE DRAWINGS (Unit : mm)

8-PIN PLASTIC DIP (7.62mm(300))



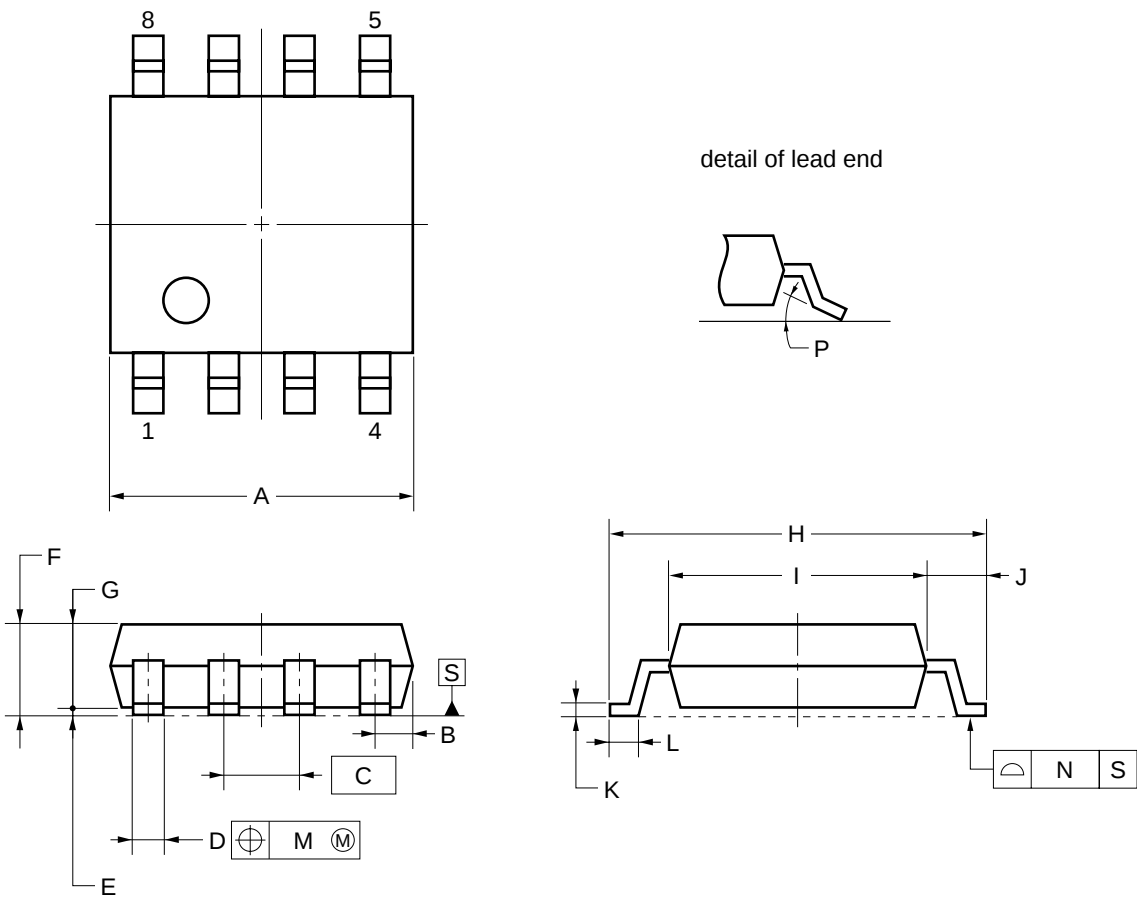
NOTES

1. Each lead centerline is located within 0.25 mm of its true position (T.P.) at maximum material condition.
2. Item "K" to center of leads when formed parallel.

ITEM	MILLIMETERS
A	10.16 MAX.
B	1.27 MAX.
C	2.54 (T.P.)
D	0.50±0.10
F	1.4 MIN.
G	3.2±0.3
H	0.51 MIN.
I	4.31 MAX.
J	5.08 MAX.
K	7.62 (T.P.)
L	6.4
M	0.25 ^{+0.10} _{-0.05}
N	0.25
P	0.9 MIN.
R	0~15°

P8C-100-300B,C-2

8-PIN PLASTIC SOP (5.72 mm (225))

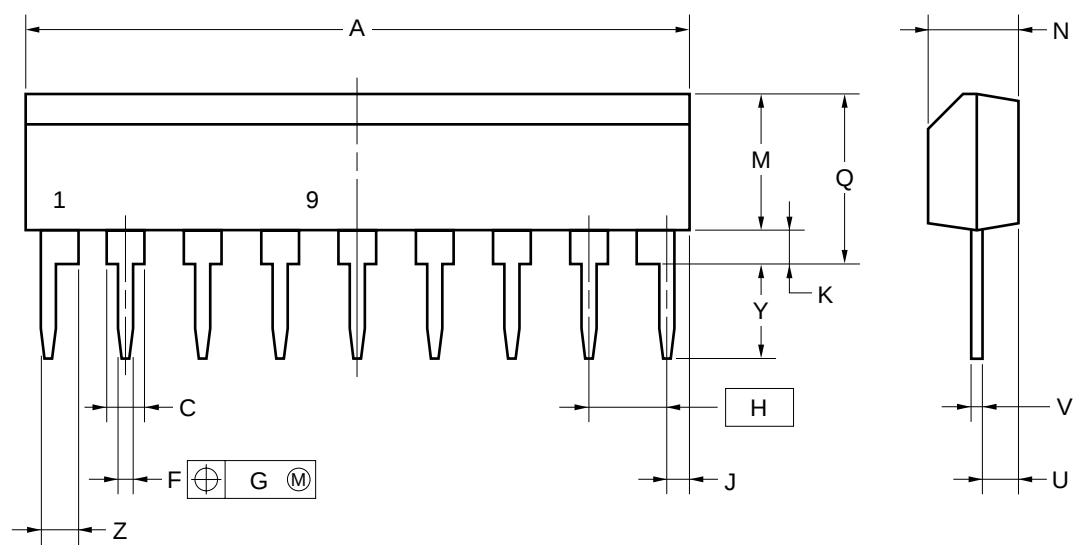


NOTE
Each lead centerline is located within 0.12 mm of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS
A	5.2 ^{+0.17} _{-0.20}
B	0.78 MAX.
C	1.27 (T.P.)
D	0.42 ^{+0.08} _{-0.07}
E	0.1±0.1
F	1.59±0.21
G	1.49
H	6.5±0.3
I	4.4±0.15
J	1.1±0.2
K	0.17 ^{+0.08} _{-0.07}
L	0.6±0.2
M	0.12
N	0.10
P	3° ^{+7°} _{-3°}

S8GM-50-225B-6

9-PIN PLASTIC SLIM SIP



NOTE
Each lead centerline is located within 0.25 mm of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS
A	22.86 MAX.
C	1.1 MIN.
F	0.5±0.1
G	0.25
H	2.54
J	1.27 MAX.
K	0.51 MIN.
M	5.08 MAX.
N	2.8±0.2
Q	5.75 MAX.
U	1.5 MAX.
V	0.25 ^{+0.10} _{-0.05}
Y	3.2±0.5
Z	1.1 MIN.

P9HA-254B-2

★ RECOMMENDED SOLDERING CONDITIONS

When soldering this product, it is highly recommended to observe the conditions as shown below. If other soldering processes are used, or if the soldering is performed under different conditions, please make sure to consult with our sales offices.

For more details, refer to our document "SEMICONDUCTOR DEVICE MOUNTING TECHNOLOGY MANUAL"(C10535E).

Type of Surface Mount Device

μPC4072G2: 8-pin plastic SOP (5.72 mm (225))

Process	Conditions	Symbol
Infrared Ray Reflow	Peak temperature: 230°C or below (Package surface temperature), Reflow time: 30 seconds or less (at 210°C or higher), Maximum number of reflow processes: 1 time.	IR30-00-1
Vapor Phase Soldering	Peak temperature: 215°C or below (Package surface temperature), Reflow time: 40 seconds or less (at 200°C or higher), Maximum number of reflow processes: 1 time.	VP15-00-1
Wave Soldering	Solder temperature: 260°C or below, Flow time: 10 seconds or less, Maximum number of flow processes: 1 time, Pre-heating temperature: 120°C or below (Package surface temperature).	WS60-00-1
Partial Heating Method	Pin temperature: 300°C or below, Heat time: 3 seconds or less (Per each side of the device).	—

Caution Apply only one kind of soldering condition to a device, except for "partial heating method", or the device will be damaged by heat stress.

Type of Through-hole Device

μPC4072C: 8-pin plastic DIP (7.62 mm (300))

μPC4072HA: 9-pin plastic slim SIP

Process	Conditions
Wave Soldering (only to leads)	Solder temperature: 260°C or below, Flow time: 10 seconds or less.
Partial Heating Method	Pin temperature: 300°C or below, Heat time: 3 seconds or less (per each lead).

Caution For through-hole device, the wave soldering process must be applied only to leads, and make sure that the package body does not get jet soldered.

[MEMO]

[MEMO]

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