

54FCT574

Octal D-Type Flip-Flop with TRI-STATE® Outputs

General Description

The 'FCT574 is an octal flip-flop with a buffered common Clock (CP) and a buffered common Output Enable (\overline{OE}). The information presented to the D inputs is stored in the flip-flops on the LOW-to-HIGH Clock (CP) transition.

The device is functionally identical to the 'FCT374 except for the pinouts.

Features

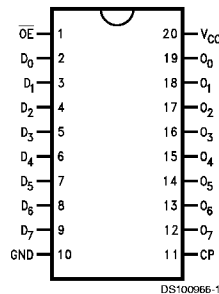
- Inputs and outputs on opposite sides of package allowing easy interface with microprocessors
- Useful as input or output port for microprocessors
- Functionally identical to 'FCT374
- TRI-STATE outputs for bus-oriented applications
- Output sink capability of 32 mA, source capability of 12 mA
- TTL input and output level compatible
- CMOS power consumption
- Standard Microcircuit Drawing (SMD) 5962-8951301

Ordering Code

Military	Package Number	Package Description
54FCT574DMQB	J20A	20-Lead Ceramic Dual-In-Line
54FCT574FMQB	W20A	20-Lead Cerpack
54FCT574LMQB	E20A	20-Lead Ceramic Leadless Chip Carrier, Type C

Connection Diagrams

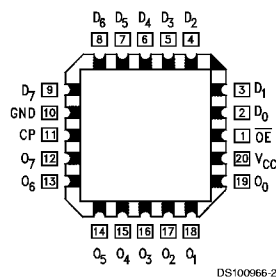
Pin Assignment for DIP and Flatpak



Pin Descriptions

Pin Names	Description
D ₀ –D ₇	Data Inputs
CP	Clock Pulse Input (Active Rising Edge)
\overline{OE}	TRI-STATE Output Enable Input (Active LOW)
O ₀ –O ₇	TRI-STATE Outputs

Pin Assignment for LCC



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Functional Description

The 74FCT574 consists of eight edge-triggered flip-flops with individual D-type inputs and TRI-STATE true outputs. The buffered clock and buffered Output Enable are common to all flip-flops. The eight flip-flops will store the state of their individual D inputs that meet the setup and hold times requirements on the LOW-to-HIGH Clock (CP) transition. With the Output Enable (\overline{OE}) LOW, the contents of the eight flip-flops are available at the outputs. When \overline{OE} is HIGH, the outputs are in a high impedance state. Operation of the \overline{OE} input does not affect the state of the flip-flops.

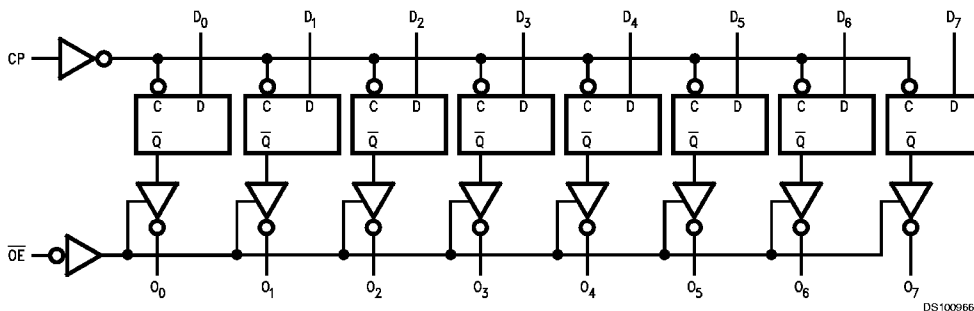
Inputs			Internal	Outputs	Function
\overline{OE}	CP	D	Q	O	
H	H or L	H	NC	Z	Hold
H	N	L	L	Z	Load
H	N	H	H	Z	Load
L	N	L	L	L	Data Available
L	N	H	H	H	Data Available
L	H or L	L	NC	NC	No Change in Data
L	H or L	H	NC	NC	No Change in Data

H = HIGH Voltage Level
 L = LOW Voltage Level
 X = Immaterial
 Z = High Impedance
 N = LOW-to-HIGH Transition
 NC = No Change

Function Table

Inputs			Internal	Outputs	Function
\overline{OE}	CP	D	Q	O	
H	H or L	L	NC	Z	Hold

Logic Diagram



DS100966-3

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	-65°C to +150°C
Ambient Temperature under Bias	-55°C to +125°C
Junction Temperature under Bias	
Ceramic	-55°C to +175°C
V _{CC} Pin Potential to Ground Pin	-0.5V to +7.0V
Input Voltage (Note 2)	-0.5V to +7.0V
Input Current (Note 2)	-30 mA to +5.0 mA
Voltage Applied to Any Output in the Disabled or Power-Off State	-0.5V to 5.5V
in the HIGH State	-0.5V to V _{CC}

Current Applied to Output in LOW State (Max)	twice the rated I _{OL} (mA)
DC Latchup Source Current	-500 mA

Recommended Operating Conditions

Free Air Ambient Temperature	
Military	-55°C to +125°C
Supply Voltage	
Military	+4.5V to +5.5V

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

DC Electrical Characteristics

Symbol	Parameter	FCT574		Units	V _{CC}	Conditions
		Min	Max			
V _{IH}	Input HIGH Voltage	2.0		V		Recognized HIGH Signal
V _{IL}	Input LOW Voltage		0.8	V		Recognized LOW Signal
V _{CD}	Input Clamp Diode Voltage		-1.2	V	Min	I _{IN} = -18 mA
V _{OH}	Output HIGH Voltage	54FCT	4.3	V	Min	I _{OH} = -300 μA
		54FCT	2.4	V	Min	I _{OH} = -12 mA
V _{OL}	Output LOW Voltage	54FCT	0.2	V	Min	I _{OL} = 300 μA
		54FCT	0.5	V	Min	I _{OL} = 32mA
I _{IH}	Input HIGH Current		5	μA	Max	V _{IN} = 2.7V (Note 3)
			5	μA	Max	V _{IN} = V _{CC}
I _{IL}	Input LOW Current		-5	μA	Max	V _{IN} = 0.5V (Note 3)
			-5	μA	Max	V _{IN} = 0.0V
I _{OZH}	Output Leakage Current		10	μA	0 - 5.5V	V _{OUT} = 2.7V; \overline{OE} = 2.0V
I _{OZL}	Output Leakage Current		-10	μA	0 - 5.5V	V _{OUT} = 0.5V; \overline{OE} = 2.0V
I _{OS}	Output Short-Circuit Current		-60	mA	Max	V _{OUT} = 0.0V
I _{CCQ}	Power Supply Current		1.5	mA	Max	V _{IN} = 0.2V or V _{IN} = 5.3V, f _i = 0MHz
ΔI _{CC}	Power Supply Current		2.0	mA	Max	V _{IN} = 3.4V
I _{CCT}	Additional I _{CC} /Input		6.0	mA	Max	V _I = V _{CC} - 2.1V or V _{IN} = GND, f _{CP} = 10MHz, Outputs open, \overline{OE} = GND, one bit toggling at f _i = 5MHz, 50% duty cycle
			5.5	mA	Max	V _I = 5.3V or V _{CC} = 0.2V, f _{CP} = 10MHz, Outputs open, \overline{OE} = GND, one bit toggling at f _i = 5MHz, 50% duty cycle
I _{CCD}	Dynamic I _{CC} No Load		0.40	mA/MHz	Max	Outputs Open, \overline{OE} = GND, One bit toggling, 50% duty cycle, V _{IN} = 5.3V or V _{IN} = 0.2V

Note 3: Guaranteed, but not tested.

AC Electrical Characteristics

Symbol	Parameter	54FCT		Units	Fig. No.
		T _A = -55°C to +125°C V _{CC} = 4.5V to 5.5V C _L = 50 pF			
		Min	Max		
t _{PLH}	Propagation Delay	2.0	11.0	ns	Figure 4
t _{PHL}	CP to O _n	2.0	11.0		
t _{PZH}	Output Enable Time	1.5	14.0	ns	Figure 6
t _{PZL}		1.5	14.0		
t _{PHZ}	Output Disable Time	1.5	8.0	ns	Figure 6
t _{PLZ}		1.5	8.0		

AC Operating Requirements

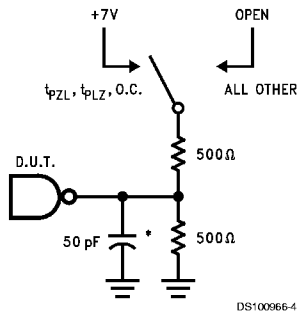
Symbol	Parameter	54FCT		Units	Fig. No.
		T _A = -55°C to +125°C V _{CC} = 4.5V to 5.5V C _L = 50 pF			
		Min	Max		
t _s (H)	Setup Time, HIGH	3.5		ns	Figure 7
t _s (L)	or LOW D _n to CP	3.5			
t _h (H)	Hold Time, HIGH	2.0		ns	Figure 7
t _h (L)	or LOW D _n to CP	2.0			
t _w (H)	Pulse Width, CP,	7.0		ns	Figure 5
t _w (L)	HIGH or LOW	7.0			

Capacitance

Symbol	Parameter	Typ	Units	Conditions T _A = 25°C
C _{IN}	Input Capacitance	5.0	pF	V _{CC} = 0V
C _{OUT} (Note 4)	Output Capacitance	9.0	pF	V _{CC} = 5.0V

Note 4: C_{OUT} is measured at frequency f = 1 MHz, per MIL-STD-883B, Method 3012.

AC Loading



*Includes jig and probe capacitance

FIGURE 1. Standard AC Test Load

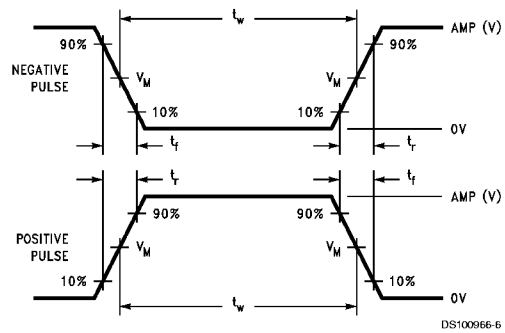


FIGURE 2. $V_M = 1.5V$

Input Pulse Requirements

Amplitude	Rep. Rate	t_w	t_r	t_f
3.0V	1 MHz	500 ns	2.5 ns	2.5 ns

FIGURE 3. Test Input Signal Requirements

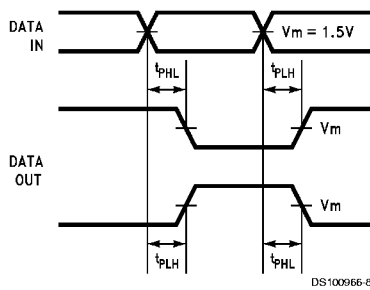


FIGURE 4. Propagation Delay Waveforms for Inverting and Non-Inverting Functions

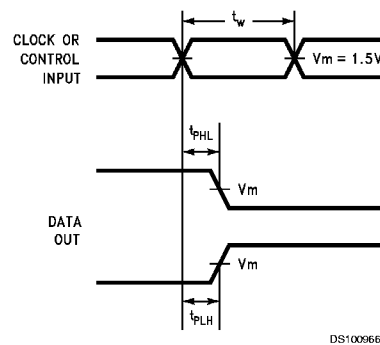


FIGURE 5. Propagation Delay, Pulse Width Waveforms

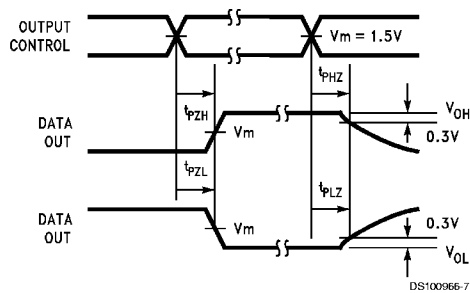


FIGURE 6. TRI-STATE Output HIGH and LOW Enable and Disable Times

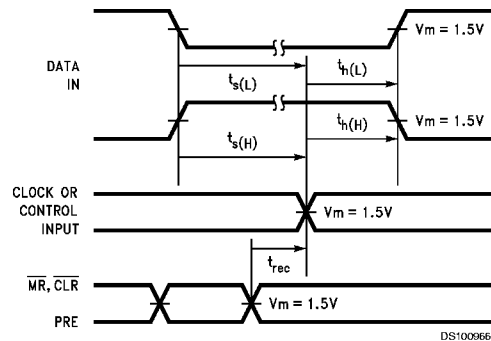
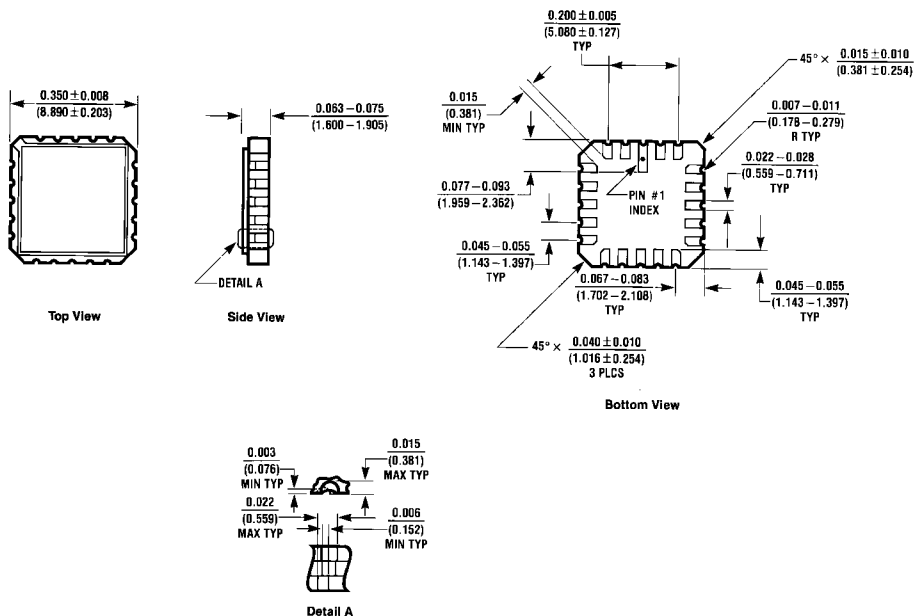


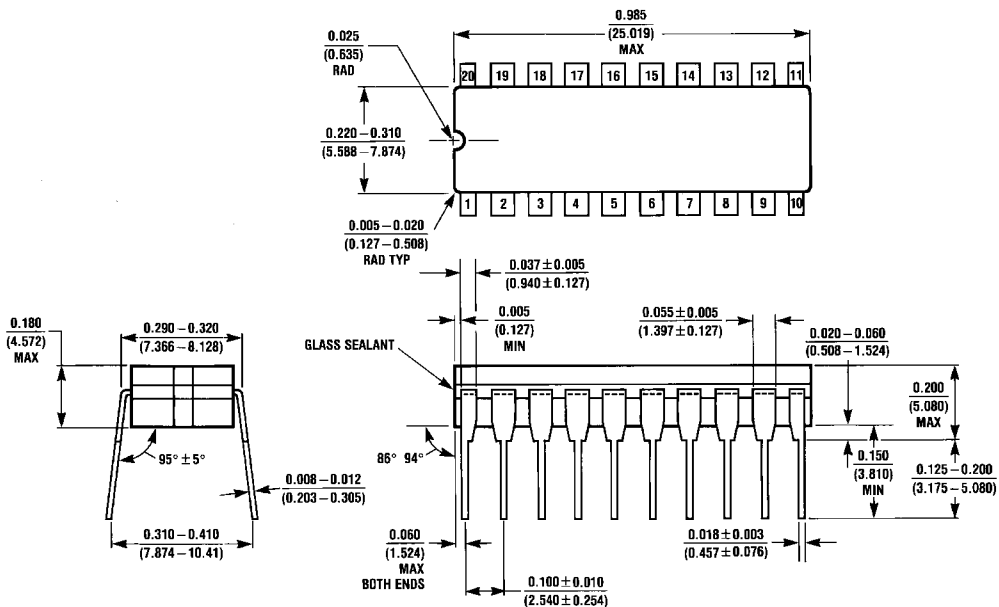
FIGURE 7. Setup Time, Hold Time and Recovery Time Waveforms

Physical Dimensions inches (millimeters) unless otherwise noted



E20A (REV D)

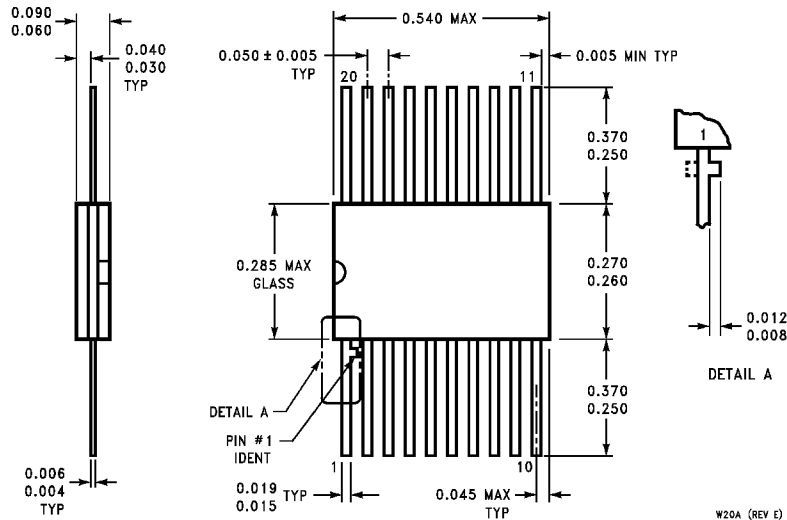
20-Terminal Ceramic Chip Carrier (L)
 NS Package Number E20A



J20A (REV M)

20-Lead Ceramic Dual-In-Line Package (D)
 NS Package Number J20A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)




**20-Lead Ceramic Flatpak (F)
NS Package Number W20A**

W20A (REV E)

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Fax: 1-800-737-7018
Email: support@nsc.com

www.national.com

National Semiconductor Europe
Fax: +49 (0) 1 80-530 85 86
Email: europe.support@nsc.com
Deutsch Tel: +49 (0) 1 80-530 85 85
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