Quad 2-Input AND Gate

MC10104

The MC10104 is a quad 2–input AND gate. One of the gates has both AND/NAND outputs available.

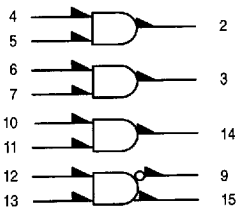
P_D = 35 mW typ/gate (No Load)
t_{pd} = 2.7 ns typ
t_r, t_f = 2.0 ns typ (20%–80%)

L SUFFIX
CERAMIC PACKAGE
CASE 620–10

P SUFFIX
PLASTIC PACKAGE
CASE 648–08

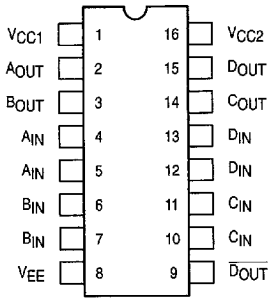
FN SUFFIX
PLCC
CASE 775–02

LOGIC DIAGRAM



V_{CC1} = PIN 1
V_{CC2} = PIN 16
V_{EE} = PIN 8

DIP
PIN ASSIGNMENT



Pin assignment is for Dual–in–Line Package.
For PLCC pin assignment, see the Pin Conversion Tables on page 6–11.

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MOTOROLA

ELECTRICAL CHARACTERISTICS

Characteristic		Symbol	Pin Under Test	Test Limits							Unit
				−30°C		+25°C			+85°C		
				Min	Max	Min	Typ	Max	Min	Max	
Power Supply Drain Current		I_E	8		39			35		39	mAdc
Input Current		I_{inH}*	12 13		425 350			265 220		265 220	µAdc
		I_{inL}	12	0.5		0.5			0.3		µAdc
Output Voltage	Logic 1	V_{OH}	15 9	−1.060 −1.060	−0.890 −0.890	−0.960 −0.960		−0.810 −0.810	−0.890 −0.890	−0.700 −0.700	Vdc
Output Voltage	Logic 0	V_{OL}	15 9	−1.890 −1.890	−1.675 −1.675	−1.850 −1.850		−1.650 −1.650	−1.825 −1.825	−1.615 −1.615	Vdc
Threshold Voltage	Logic 1	V_{OHA}	9 9 15 15	−1.090 −1.090 −1.090 −1.090		−0.980 −0.980 −0.980 −0.980			−0.910 −0.910 −0.910 −0.910		Vdc
Threshold Voltage	Logic 0	V_{OLA}	9 9 15 15		−1.655 −1.655 −1.655 −1.655			−1.630 −1.630 −1.630 −1.630		−1.595 −1.595 −1.595 −1.595	Vdc
Switching Times	(50Ω Load)										ns
Propagation Delay		t_{12+15+} t_{12-15-} t_{12+9-} t_{12-9+}	15 15 9 9	1.0 1.0 1.0 1.0	4.3 4.3 4.3 4.3	1.0 1.0 1.0 1.0	2.2 2.2 2.2 2.2	4.0 4.0 4.0 4.0	1.0 1.0 1.0 1.0	4.2 4.2 4.2 4.2	
		t_{13+15+} t_{13+9-}	15 9	1.0 1.0	4.3 4.3	1.0 1.0	2.7 2.7	4.0 4.0	1.0 1.0	4.2 4.2	
Rise Time	(20 to 80%)	t_{15+} t_{9+}	15 9	1.5 1.5	3.7 3.7	1.5 1.5	2.0 2.0	3.5 3.5	1.5 1.5	3.6 3.6	
Fall Time	(20 to 80%)	t_{15-} t_{9-}	15 9	1.5 1.5	3.7 3.7	1.5 1.5	2.0 2.0	3.5 3.5	1.5 1.5	3.6 3.6	

* Inputs 4, 7, 10 and 13 will behave similarly for ac and I_{inH} values.
Inputs 5, 6, 11 and 12 will behave similarly for ac and I_{inH} values.

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ELECTRICAL CHARACTERISTICS (continued)

@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}	(V_{CC}) Gnd
−30°C	−0.890	−1.890	−1.205	−1.500	−5.2	
+25°C	−0.810	−1.850	−1.105	−1.475	−5.2	
+85°C	−0.700	−1.825	−1.035	−1.440	−5.2	

Characteristic		Symbol	Pin Under Test	TEST VOLTAGE APPLIED TO PINS LISTED BELOW V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current		I_E	8					8	1, 16
Input Current		I_{inH}*	12	12, 13				8	1, 16
			13	13				8	1, 16
		I_{inL}	12		12			8	1, 16
Output Voltage	Logic 1	V_{OH}	15	12, 13				8	1, 16
			9					8	1, 16
Output Voltage	Logic 0	V_{OL}	15					8	1, 16
			9	12, 13				8	1, 16
Threshold Voltage	Logic 1	V_{OHA}	9				12	8	1, 16
			9				13	8	1, 16
			15	12		13		8	1, 16
			15	13		12		8	1, 16
Threshold Voltage	Logic 0	V_{OLA}	9	12		13		8	1, 16
			9	13		12		8	1, 16
			15				12	8	1, 16
			15				13	8	1, 16
Switching Times	(50Ω Load)			+1.11V		Pulse In	Pulse Out	−3.2 V	+2.0 V
Propagation Delay		t_{12+15+}	15	13		12	15	8	1, 16
		t_{12-15-}	15	13		12	15	8	1, 16
		t_{12+9-}	9	13		12	9	8	1, 16
		t_{12-9+}	9	13		12	9	8	1, 16
		t_{13+15+}	15	12		13	15	8	1, 16
		t_{13+9-}	9	12		13	9	8	1, 16
Rise Time	(20 to 80%)	t_{15+}	15	12		13	15	8	1, 16
		t_{9+}	9	12		13	9	8	1, 16
Fall Time	(20 to 80%)	t_{15-}	15	12		13	15	8	1, 16
		t_{9-}	9	12		13	9	8	1, 16

* Inputs 4, 7, 10 and 13 will behave similarly for ac and I_{inH} values.
Inputs 5, 6, 11 and 12 will behave similarly for ac and I_{inH} values.

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to −2.0 volts. Test procedures are shown for only one gate. The other gates are tested in the same manner.