

74F823

9-Bit D-Type Flip-Flop

General Description

The 74F823 is a 9-bit buffered register. It features Clock Enable and Clear which are ideal for parity bus interfacing in high performance microprogramming systems.

Features

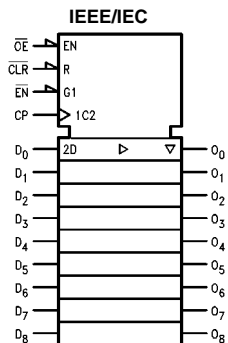
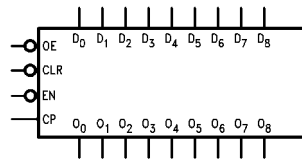
- 3-STATE outputs
- Clock Enable and Clear

Ordering Code:

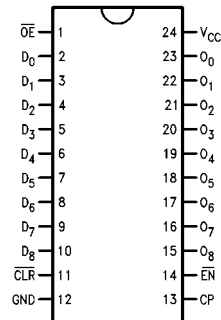
Order Number	Package Number	Package Description
74F823SC	M24B	24-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide
74F823SPC	N24C	24-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-100, 0.300 Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Logic Symbols



Connection Diagram



Unit Loading/Fan Out

Pin Names	Description	U.L. HIGH/LOW	Input I_{IH}/I_{IL} Output I_{OH}/I_{OL}
D ₀ -D ₈	Data Inputs	1.0/1.0	20 μ A/-0.6 mA
\overline{OE}	Output Enable Input	1.0/1.0	20 μ A/-0.6 mA
\overline{CLR}	Clear	1.0/1.0	20 μ A/-0.6 mA
CP	Clock Input	1.0/2.0	20 μ A/-1.2 mA
\overline{EN}	Clock Enable	1.0/1.0	20 μ A/-0.6 mA
O ₀ -O ₈	3-STATE Outputs	150/40 (33.3)	-3 mA/24 mA (20 mA)

Functional Description

The 74F823 device consists of nine D-type edge-triggered flip-flops. It has 3-STATE true outputs and is organized in broadside pinning. The buffered Clock (CP) and buffered Output Enable (\overline{OE}) are common to all flip-flops. The flip-flops will store the state of their individual D inputs that meet the setup and hold times requirements on the LOW-to-HIGH CP transition. With the \overline{OE} LOW the contents of the flip-flops are available at the outputs. When the \overline{OE} is HIGH, the outputs go to the high impedance state. Operation of the \overline{OE} input does not affect the state of the flip-flops. In addition to the Clock and Output Enable pins, the 74F823 has Clear (\overline{CLR}) and Clock Enable (\overline{EN}) pins.

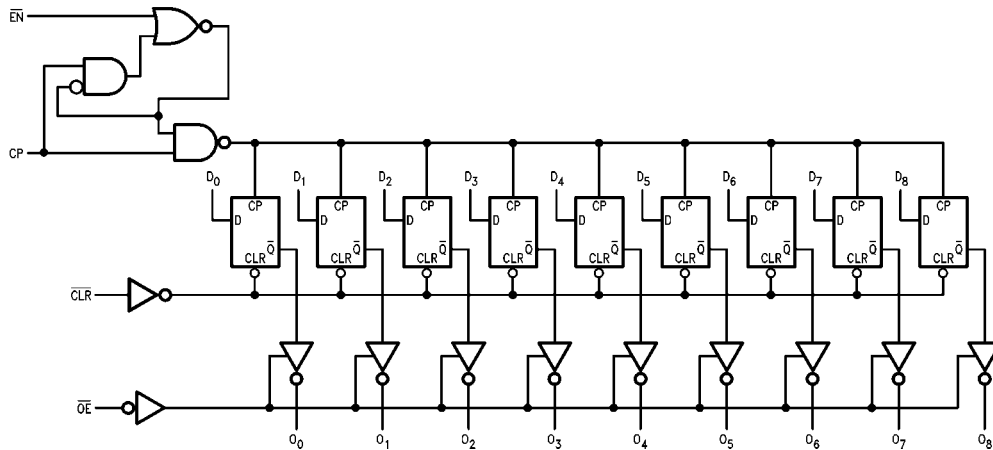
When the \overline{CLR} is LOW and the \overline{OE} is LOW, the outputs are LOW. When \overline{CLR} is HIGH, data can be entered into the flip-flops. When \overline{EN} is LOW, data on the inputs is transferred to the outputs on the LOW-to-HIGH clock transition. When the \overline{EN} is HIGH, the outputs do not change state regardless of the data or clock inputs transitions. This device is ideal for parity bus interfacing in high performance systems.

Function Table

Inputs					Internal	Output	Function
\overline{OE}	\overline{CLR}	\overline{EN}	CP	D	\overline{Q}	O	
H	H	L	H	X	NC	Z	Hold
H	H	L	L	X	NC	Z	Hold
H	H	H	X	X	NC	Z	Hold
L	H	H	X	X	NC	NC	Hold
H	L	X	X	X	H	Z	Clear
L	L	X	X	X	H	L	Clear
H	H	L	\nearrow	H	H	Z	Load
H	H	L	\nearrow	H	L	Z	Load
L	H	L	\nearrow	L	H	L	Data Available
L	H	L	\nearrow	H	L	H	Data Available
L	H	L	H	X	NC	NC	No Change in Data
L	H	L	L	X	NC	NC	No Change in Data

L = LOW Voltage Level
H = HIGH Voltage Level
X = Immaterial
Z = High Impedance
 \nearrow = LOW-to-HIGH Transition
NC = No Change

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings(Note 1)

Storage Temperature	-65°C to +150°C
Ambient Temperature under Bias	-55°C to +125°C
Junction Temperature under Bias	-55°C to +150°C
V _{CC} Pin Potential to Ground Pin	-0.5V to +7.0V
Input Voltage (Note 2)	-0.5V to +7.0V
Input Current (Note 2)	-30 mA to +5.0 mA
Voltage Applied to Output in HIGH State (with V _{CC} = 0V)	
Standard Output	-0.5V to V _{CC}
3-STATE Output	-0.5V to +5.5V
Current Applied to Output in LOW State (Max)	twice the rated I _{OL} (mA)

Recommended Operating Conditions

Free Air Ambient Temperature	0°C to +70°C
Supply Voltage	+4.5V to +5.5V

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

DC Electrical Characteristics

Symbol	Parameter	Min	Typ	Max	Units	V _{CC}	Conditions
V _{IH}	Input HIGH Voltage	2.0			V		Recognized as a HIGH Signal
V _{IL}	Input LOW Voltage			0.8	V		Recognized as a LOW Signal
V _{CD}	Input Clamp Diode Voltage			-1.2	V	Min	I _{IN} = -18 mA
V _{OH}	Output HIGH Voltage	10% V _{CC} 10% V _{CC} 5% V _{CC} 5% V _{CC}	2.5 2.4 2.7 2.7		V	Min	I _{OH} = -1 mA I _{OH} = -3 mA I _{OH} = -1 mA I _{OH} = -3 mA
V _{OL}	Output LOW Voltage	10% V _{CC}		0.5	V	Min	I _{OL} = 24 mA
I _{IH}	Input HIGH Current			5.0	μA	Max	V _{IN} = 2.7V
I _{BVI}	Input HIGH Current Breakdown Test			7.0	μA	Max	V _{IN} = 7.0V
I _{CEX}	Output HIGH Leakage Current			50	μA	Max	V _{OUT} = V _{CC}
V _{ID}	Input Leakage Test	4.75			V	0.0	I _{ID} = 1.9 μA All Other Pins Grounded
I _{OD}	Output Leakage Circuit Current			3.75	μA	0.0	V _{IDP} = 150 mV All Other Pins Grounded
I _{IL}	Input LOW Current			-0.6 -1.2	mA mA	Max Max	V _{IN} = 0.5V (OE, CLR, EN) V _{IN} = 0.5V (CP)
I _{OZH}	Output Leakage Current			50	μA	Max	V _{OUT} = 2.7V
I _{OZL}	Output Leakage Current			-50	μA	Max	V _{OUT} = 0.5V
I _{OS}	Output Short-Circuit Current	-60		-150	mA	Max	V _{OUT} = 0V
I _{ZZ}	Buss Drainage Test			500	μA	0.0V	V _{OUT} = 5.25V
I _{CCZ}	Power Supply Current		75	100	mA	Max	V _O = HIGH Z

AC Electrical Characteristics

Symbol	Parameter	T _A = +25°C V _{CC} = +5.0V C _L = 50 pF			T _A = -55°C to +125°C V _{CC} = +5.0V C _L = 50 pF		T _A = 0°C to +70°C V _{CC} = +5.0V C _L = 50 pF		Units
		Min	Typ	Max	Min	Max	Min	Max	
f _{MAX}	Maximum Clock Frequency	100	160		60		70		MHz
t _{PLH}	Propagation Delay	2.0	5.6	9.5	2.0	10.5	2.0	10.5	ns
t _{PHL}	CP to O _n	2.0	5.2	9.5	2.0	10.5	2.0	10.5	
t _{PHL}	Propagation Delay CLR to O _n	4.0	7.1	12.0	4.0	13.0	4.0	13.0	ns
t _{PZH}	Output Enable Time	2.0	5.8	10.5	2.0	13.0	2.0	11.5	ns
t _{PZL}	OE to O _n	2.0	5.5	10.5	2.0	13.0	2.0	11.5	
t _{PHZ}	Output Disable Time	1.5	2.9	7.0	1.0	7.5	1.5	7.5	ns
t _{PLZ}	OE to O _n	1.5	2.7	7.0	1.0	7.5	1.5	7.5	

AC Operating Requirements

Symbol	Parameter	T _A = +25°C V _{CC} = +5.0V		T _A = -55°C to +125°C V _{CC} = +5.0V		T _A = 0°C to +70°C V _{CC} = +5.0V		Units
		Min	Max	Min	Max	Min	Max	
t _S (H)	Setup Time, HIGH or LOW	2.5		4.0		3.0		ns
t _S (L)	D _n to CP	2.5		4.0		3.0		
t _H (H)	Hold Time, HIGH or LOW	2.5		2.5		2.5		ns
t _H (L)	D _n to CP	2.5		2.5		2.5		
t _S (H)	Setup Time, HIGH or LOW	4.5		5.0		5.0		ns
t _S (L)	EN to CP	2.5		3.0		3.0		
t _H (H)	Hold Time, HIGH or LOW	2.0		3.0		2.0		ns
t _H (L)	EN to CP	0		1.0		0		
t _W (H)	CP Pulse Width	5.0		6.0		6.0		ns
t _W (L)	HIGH or LOW	5.0		6.0		6.0		ns
t _W (L)	CLR Pulse Width, LOW	5.0		5.0		5.0		ns
t _{REC}	CLR Recovery Time	5.0		5.0		5.0		ns

