



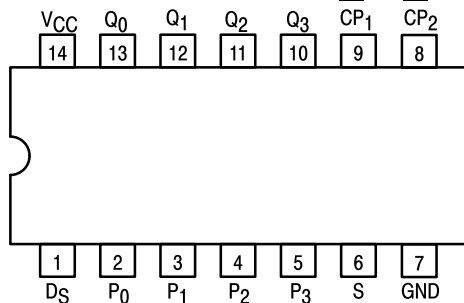
4-BIT SHIFT REGISTER

The SN54/74LS95B is a 4-Bit Shift Register with serial and parallel synchronous operating modes. The serial shift right and parallel load are activated by separate clock inputs which are selected by a mode control input. The data is transferred from the serial or parallel D inputs to the Q outputs synchronous with the HIGH to LOW transition of the appropriate clock input.

The LS95B is fabricated with the Schottky barrier diode process for high speed and is completely compatible with all Motorola TTL families.

- Synchronous, Expandable Shift Right
- Synchronous Shift Left Capability
- Synchronous Parallel Load
- Separate Shift and Load Clock Inputs
- Input Clamp Diodes Limit High Speed Termination Effects

CONNECTION DIAGRAM DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

V_{CC} = PIN 14
GND = PIN 7

PIN NAMES

- S Mode Control Input
- D_S Serial Data Input
- P₀-P₃ Parallel Data Inputs
- CP₁ Serial Clock (Active LOW Going Edge) Input
- CP₂ Parallel Clock (Active LOW Going Edge) Input
- Q₀-Q₃ Parallel Outputs (Note b)

LOADING (Note a)

| | HIGH | LOW |
|--------------------------------|----------|--------------|
| S | 0.5 U.L. | 0.25 U.L. |
| D _S | 0.5 U.L. | 0.25 U.L. |
| P ₀ -P ₃ | 0.5 U.L. | 0.25 U.L. |
| CP ₁ | 0.5 U.L. | 0.25 U.L. |
| CP ₂ | 0.5 U.L. | 0.25 U.L. |
| Q ₀ -Q ₃ | 10 U.L. | 5 (2.5) U.L. |

NOTES:

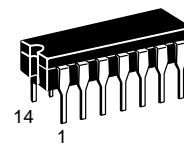
- a. 1 TTL Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW.
- b. The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74) Temperature Ranges.

GUARANTEED OPERATING RANGES

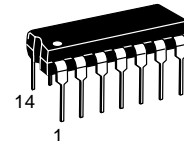
| Symbol | Parameter | | Min | Typ | Max | Unit |
|-----------------|-------------------------------------|----------|-------------|------------|-------------|------|
| V _{CC} | Supply Voltage | 54 74 | 4.5 4.75 | 5.0 5.0 | 5.5 5.25 | V |
| T _A | Operating Ambient Temperature Range | 54 74 | -55 0 | 25 25 | 125 70 | °C |
| I _{OH} | Output Current — High | 54, 74 | | | -0.4 | mA |
| I _{OL} | Output Current — Low | 54 74 | | | 4.0 8.0 | mA |

SN54/74LS95B

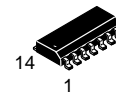
4-BIT SHIFT REGISTER LOW POWER SCHOTTKY



J SUFFIX
CERAMIC
CASE 632-08



N SUFFIX
PLASTIC
CASE 646-06



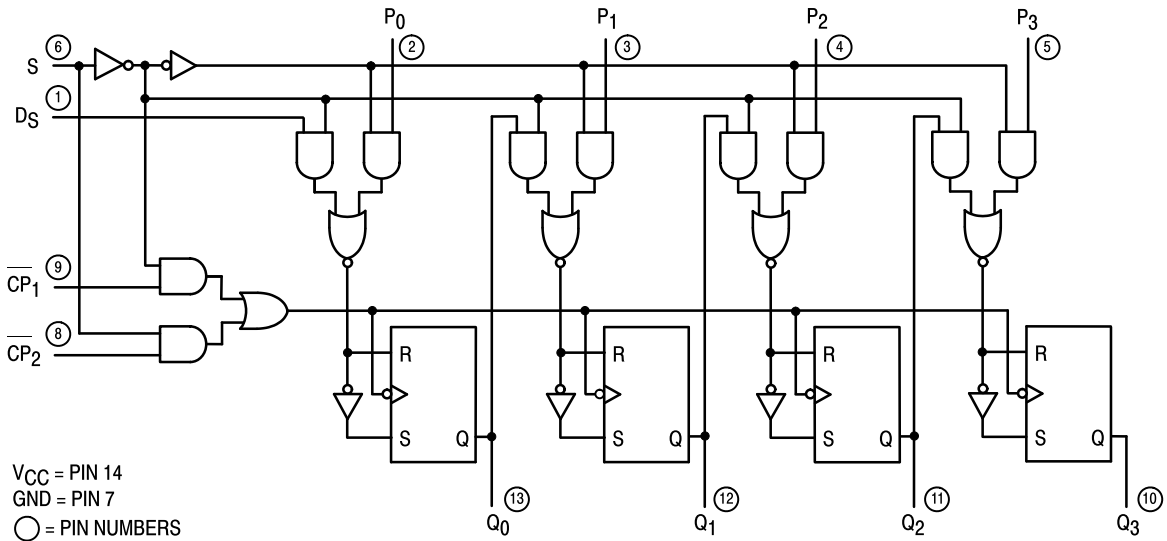
D SUFFIX
SOIC
CASE 751A-02

ORDERING INFORMATION

- SN54LSXXJ Ceramic
- SN74LSXXN Plastic
- SN74LSXXD SOIC

SN54/74LS95B

LOGIC DIAGRAM



FUNCTIONAL DESCRIPTION

The LS95B is a 4-Bit Shift Register with serial and parallel synchronous operating modes. It has a Serial (D_S) and four Parallel (P_0 – P_3) Data inputs and four Parallel Data outputs (Q_0 – Q_3). The serial or parallel mode of operation is controlled by a Mode Control input (S) and two Clock Inputs (CP_1) and (CP_2). The serial (right-shift) or parallel data transfers occur synchronous with the HIGH to LOW transition of the selected clock input.

When the Mode Control input (S) is HIGH, CP_2 is enabled. A HIGH to LOW transition on enabled CP_2 transfers parallel data from the P_0 – P_3 inputs to the Q_0 – Q_3 outputs.

When the Mode Control input (S) is LOW, CP_1 is enabled. A

HIGH to LOW transition on enabled CP_1 transfers the data from Serial input (D_S) to Q_0 and shifts the data in Q_0 to Q_1 , Q_1 to Q_2 , and Q_2 to Q_3 respectively (right-shift). A left-shift is accomplished by externally connecting Q_3 to P_2 , Q_2 to P_1 , and Q_1 to P_0 , and operating the LS95B in the parallel mode (S = HIGH).

For normal operation, S should only change states when both Clock inputs are LOW. However, changing S from LOW to HIGH while CP_2 is HIGH, or changing S from HIGH to LOW while CP_1 is HIGH and CP_2 is LOW will not cause any changes on the register outputs.

MODE SELECT — TRUTH TABLE

| OPERATING MODE | INPUTS | | | | | OUTPUTS | | | |
|----------------|--------|-----------------|-----------------|----------------|----------------|----------------|----------------|----------------|----------------|
| | S | CP ₁ | CP ₂ | D _S | P _n | Q ₀ | Q ₁ | Q ₂ | Q ₃ |
| Shift | L | ⌊ | X | l | X | L | q ₀ | q ₁ | q ₂ |
| | L | ⌊ | X | h | X | H | q ₀ | q ₁ | q ₂ |
| Parallel Load | H | X | ⌊ | X | P _n | P ₀ | P ₁ | P ₂ | P ₃ |
| Mode Change | ⌊ | L | L | X | X | No Change | | | |
| | ⌋ | L | L | X | X | No Change | | | |
| | ⌊ | H | L | X | X | No Change | | | |
| | ⌋ | H | L | X | X | Undetermined | | | |
| | ⌊ | L | H | X | X | Undetermined | | | |
| | ⌋ | L | H | X | X | No Change | | | |
| | ⌊ | H | H | X | X | Undetermined | | | |
| | ⌋ | H | H | X | X | No Change | | | |

L = LOW Voltage Level

H = HIGH Voltage Level

X = Don't Care

l = LOW Voltage Level one set-up time prior to the HIGH to LOW clock transition.

h = HIGH Voltage Level one set-up time prior to the HIGH to LOW clock transition.

P_n = Lower case letters indicate the state of the referenced input (or output) one set-up time prior to the HIGH to LOW clock transition.

SN54/74LS95B

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

| Symbol | Parameter | Limits | | | Unit | Test Conditions | |
|-----------------|--------------------------------|--------|-------|------|------|--|---|
| | | Min | Typ | Max | | | |
| V _{IH} | Input HIGH Voltage | 2.0 | | | V | Guaranteed Input HIGH Voltage for All Inputs | |
| V _{IL} | Input LOW Voltage | 54 | | 0.7 | V | Guaranteed Input LOW Voltage for All Inputs | |
| | | 74 | | 0.8 | | | |
| V _{IK} | Input Clamp Diode Voltage | | -0.65 | -1.5 | V | V _{CC} = MIN, I _{IN} = -18 mA | |
| V _{OH} | Output HIGH Voltage | 54 | 2.5 | 3.5 | V | V _{CC} = MIN, I _{OH} = MAX, V _{IN} = V _{IH} or V _{IL} per Truth Table | |
| | | 74 | 2.7 | 3.5 | V | | |
| V _{OL} | Output LOW Voltage | 54, 74 | | 0.25 | 0.4 | V | I _{OL} = 4.0 mA V _{CC} = V _{CC} MIN, V _{IN} = V _{IL} or V _{IH} per Truth Table |
| | | 74 | | 0.35 | 0.5 | V | |
| I _{IH} | Input HIGH Current | | | 20 | μA | V _{CC} = MAX, V _{IN} = 2.7 V | |
| | | | | 0.1 | mA | V _{CC} = MAX, V _{IN} = 7.0 V | |
| I _{IL} | Input HIGH Current | | | -0.4 | mA | V _{CC} = MAX, V _{IN} = 0.4 V | |
| I _{OS} | Short Circuit Current (Note 1) | -20 | | -100 | mA | V _{CC} = MAX | |
| I _{CC} | Power Supply Current | | | 21 | mA | V _{CC} = MAX | |

Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

AC CHARACTERISTICS (T_A = 25°C, V_{CC} = 5.0 V)

| Symbol | Parameter | Limits | | | Unit | Test Conditions |
|--------------------------------------|-------------------------|--------|-----|-----|------|---|
| | | Min | Typ | Max | | |
| f _{MAX} | Maximum Clock Frequency | 25 | 36 | | MHz | V _{CC} = 5.0 V C _L = 15 pF |
| t _{PLH} t _{PHL} | CP to Output | | 18 | 27 | ns | |
| | | | 21 | 32 | ns | |

AC SETUP REQUIREMENTS (T_A = 25°C, V_{CC} = 5.0 V)

| Symbol | Parameter | Limits | | | Unit | Test Conditions |
|----------------|-------------------------|--------|-----|-----|------|-------------------------|
| | | Min | Typ | Max | | |
| t _W | CP Pulse Width | 20 | | | ns | V _{CC} = 5.0 V |
| t _S | Data Setup Time | 20 | | | ns | |
| t _H | Data Hold Time | 20 | | | ns | |
| t _S | Mode Control Setup Time | 20 | | | ns | |
| t _H | Mode Control Hold Time | 20 | | | ns | |

SN54/74LS95B

DESCRIPTION OF TERMS

SETUP TIME (t_s) — is defined as the minimum time required for the correct logic level to be present at the logic input prior to the clock transition from HIGH to LOW in order to be recognized and transferred to the outputs.

HOLD TIME (t_h) — is defined as the minimum time following

the clock transition from HIGH to LOW that the logic level must be maintained at the input in order to ensure continued recognition. A negative HOLD TIME indicates that the correct logic level may be released prior to the clock transition from HIGH to LOW and still be recognized.

AC WAVEFORMS

The shaded areas indicate when the input is permitted to change for predictable output performance.

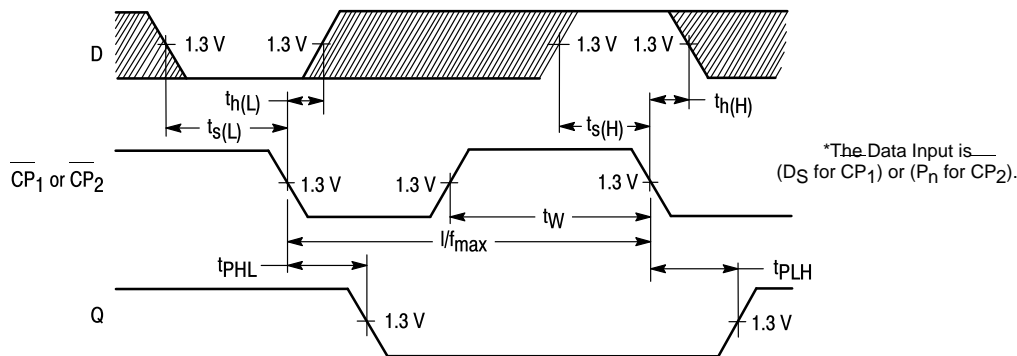


Figure 1

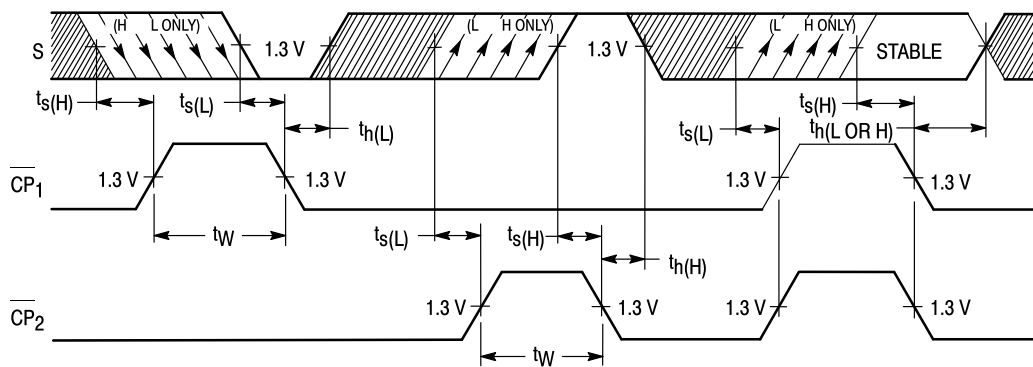
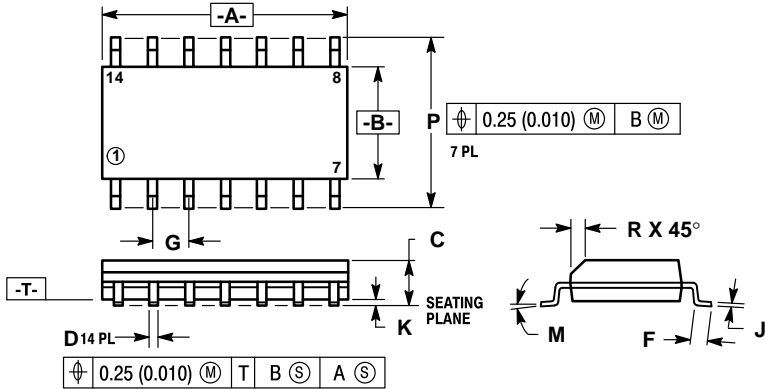


Figure 2

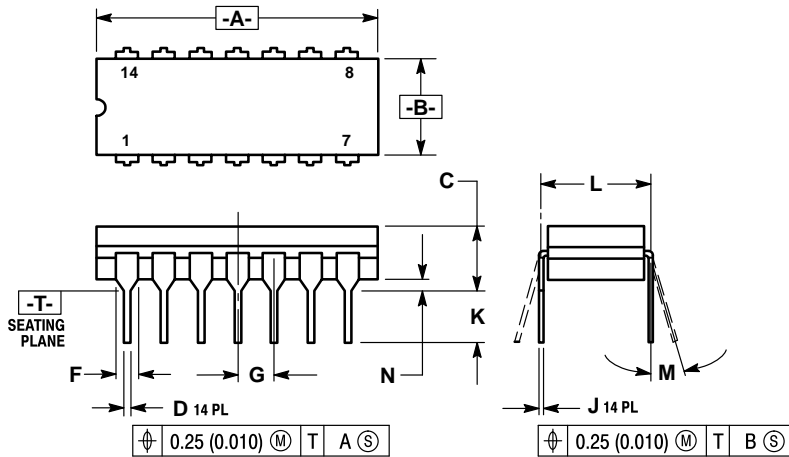
Case 751A-02 D Suffix
14-Pin Plastic
SO-14



- NOTES:
1. DIMENSIONS "A" AND "B" ARE DATUMS AND "T" IS A DATUM SURFACE.
 2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 3. CONTROLLING DIMENSION: MILLIMETER.
 4. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
 5. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
 6. 751A-01 IS OBSOLETE, NEW STANDARD 751A-02.

| DIM | MILLIMETERS | | INCHES | |
|-----|-------------|------|-----------|-------|
| | MIN | MAX | MIN | MAX |
| A | 8.55 | 8.75 | 0.337 | 0.344 |
| B | 3.80 | 4.00 | 0.150 | 0.157 |
| C | 1.35 | 1.75 | 0.054 | 0.068 |
| D | 0.35 | 0.49 | 0.014 | 0.019 |
| F | 0.40 | 1.25 | 0.016 | 0.049 |
| G | 1.27 BSC | | 0.050 BSC | |
| J | 0.19 | 0.25 | 0.008 | 0.009 |
| K | 0.10 | 0.25 | 0.004 | 0.009 |
| M | 0° | 7° | 0° | 7° |
| P | 5.80 | 6.20 | 0.229 | 0.244 |
| R | 0.25 | 0.50 | 0.010 | 0.019 |

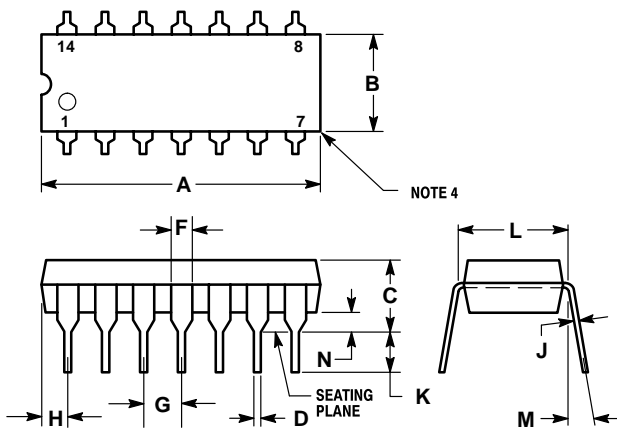
Case 632-08 J Suffix
14-Pin Ceramic Dual In-Line



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: INCH.
 3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
 4. DIM F MAY NARROW TO 0.76 (0.030) WHERE THE LEAD ENTERS THE CERAMIC BODY.
 5. 632-01 THRU -07 OBSOLETE, NEW STANDARD 632-08.


| DIM | MILLIMETERS | | INCHES | |
|-----|-------------|-------|-----------|-------|
| | MIN | MAX | MIN | MAX |
| A | 19.05 | 19.94 | 0.750 | 0.785 |
| B | 6.23 | 7.11 | 0.245 | 0.280 |
| C | 3.94 | 5.08 | 0.155 | 0.200 |
| D | 0.39 | 0.50 | 0.015 | 0.020 |
| F | 1.40 | 1.65 | 0.055 | 0.065 |
| G | 2.54 BSC | | 0.100 BSC | |
| J | 0.21 | 0.38 | 0.008 | 0.015 |
| K | 3.18 | 4.31 | 0.125 | 0.170 |
| L | 7.62 BSC | | 0.300 BSC | |
| M | 0° | 15° | 0° | 15° |
| N | 0.51 | 1.01 | 0.020 | 0.040 |

Case 646-06 N Suffix
14-Pin Plastic



- NOTES:
1. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
 2. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
 3. DIMENSION "B" DOES NOT INCLUDE MOLD FLASH.
 4. ROUNDED CORNERS OPTIONAL.
 5. 646-05 OBSOLETE, NEW STANDARD 646-06.

| DIM | MILLIMETERS | | INCHES | |
|-----|-------------|-------|-----------|-------|
| | MIN | MAX | MIN | MAX |
| A | 18.16 | 19.56 | 0.715 | 0.770 |
| B | 6.10 | 6.60 | 0.240 | 0.260 |
| C | 3.69 | 4.69 | 0.145 | 0.185 |
| D | 0.38 | 0.53 | 0.015 | 0.021 |
| F | 1.02 | 1.78 | 0.040 | 0.070 |
| G | 2.54 BSC | | 0.100 BSC | |
| H | 1.32 | 2.41 | 0.052 | 0.095 |
| J | 0.20 | 0.38 | 0.008 | 0.015 |
| K | 2.92 | 3.43 | 0.115 | 0.135 |
| L | 7.62 BSC | | 0.300 BSC | |
| M | 0° | 10° | 0° | 10° |
| N | 0.39 | 1.01 | 0.015 | 0.039 |

Motorola reserves the right to make changes without further notice to any products herein. Motorola makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does Motorola assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation consequential or incidental damages. "Typical" parameters can and do vary in different applications. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. Motorola does not convey any license under its patent rights nor the rights of others. Motorola products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the Motorola product could create a situation where personal injury or death may occur. Should Buyer purchase or use Motorola products for any such unintended or unauthorized application, Buyer shall indemnify and hold Motorola and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that Motorola was negligent regarding the design or manufacture of the part. Motorola and  are registered trademarks of Motorola, Inc. Motorola, Inc. is an Equal Opportunity/Affirmative Action Employer.

Literature Distribution Centers:

USA: Motorola Literature Distribution; P.O. Box 20912; Phoenix, Arizona 85036.

EUROPE: Motorola Ltd.; European Literature Centre; 88 Tanners Drive, Blakelands, Milton Keynes, MK14 5BP, England.

JAPAN: Nippon Motorola Ltd.; 4-32-1, Nishi-Gotanda, Shinagawa-ku, Tokyo 141, Japan.

ASIA PACIFIC: Motorola Semiconductors H.K. Ltd.; Silicon Harbour Center, No. 2 Dai King Street, Tai Po Industrial Estate, Tai Po, N.T., Hong Kong.





LittleDiode supplies new, hard to find or obsolete electronic components and semiconductors all over the world.

With over two million different components listed you are sure to find the part you need.

Feel free to visit us today at our online store:

LittleDiode.com

Looking forward to providing you with the best possible service.