

# DATA SHEET

For a complete data sheet, please also download:

- The IC06 74HC/HCT/HCU/HCMOS Logic Family Specifications
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Information
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Outlines

## **74HC/HCT137**

**3-to-8 line decoder/demultiplexer  
with address latches; inverting**

Product specification  
File under Integrated Circuits, IC06

December 1990

## 3-to-8 line decoder/demultiplexer with address latches; inverting

## 74HC/HCT137

### FEATURES

- Combines 3-to-8 decoder with 3-bit latch
- Multiple input enable for easy expansion or independent controls
- Active LOW mutually exclusive outputs
- Output capability: standard
- I<sub>CC</sub> category: MSI

### GENERAL DESCRIPTION

The 74HC/HCT137 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT137 are 3-to-8 line decoder/demultiplexers with latches at the three address inputs (A<sub>n</sub>). The "137" essentially combines the 3-to-8 decoder function with a 3-bit storage latch. When the latch is enabled ( $\overline{LE} = \text{LOW}$ ), the "137" acts as a 3-to-8 active LOW decoder. When the latch enable ( $\overline{LE}$ ) goes from LOW-to-HIGH, the last data present at the inputs before this transition, is stored in the latches. Further address changes are ignored as long as  $\overline{LE}$  remains HIGH.

The output enable input ( $\overline{E}_1$  and E<sub>2</sub>) controls the state of the outputs independent of the address inputs or latch operation. All outputs are HIGH unless  $\overline{E}_1$  is LOW and E<sub>2</sub> is HIGH.

The "137" is ideally suited for implementing non-overlapping decoders in 3-state systems and strobed (stored address) applications in bus oriented systems.

### QUICK REFERENCE DATA

GND = 0 V; T<sub>amb</sub> = 25 °C; t<sub>r</sub> = t<sub>f</sub> = 6 ns

| SYMBOL                              | PARAMETER                                 | CONDITIONS                                    | TYPICAL |     | UNIT |
|-------------------------------------|---|---|---------|-----|------|
|                                     |   |   | HC      | HCT |      |
| t <sub>PHL</sub> / t <sub>PLH</sub> | propagation delay                         | C <sub>L</sub> = 15 pF; V <sub>CC</sub> = 5 V |         |     |      |
|                                     | A <sub>n</sub> to $\overline{Y}_n$        |   | 18      | 19  | ns   |
|                                     | $\overline{LE}$ to $\overline{Y}_n$       |   | 17      | 21  | ns   |
|                                     | $\overline{E}_1$ to $\overline{Y}_n$      |   | 15      | 17  | ns   |
|                                     | E <sub>2</sub> to $\overline{Y}_n$        |   | 15      | 15  | ns   |
| C <sub>I</sub>                      | input capacitance                         |   | 3.5     | 3.5 | pF   |
| C <sub>PD</sub>                     | power dissipation capacitance per package | notes 1 and 2                                 | 57      | 59  | pF   |

### Notes

1. C<sub>PD</sub> is used to determine the dynamic power dissipation (P<sub>D</sub> in μW):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f<sub>i</sub> = input frequency in MHz

f<sub>o</sub> = output frequency in MHz

∑ (C<sub>L</sub> × V<sub>CC</sub><sup>2</sup> × f<sub>o</sub>) = sum of outputs

C<sub>L</sub> = output load capacitance in pF

V<sub>CC</sub> = supply voltage in V

2. For HC the condition is V<sub>1</sub> = GND to V<sub>CC</sub>  
For HCT the condition is V<sub>1</sub> = GND to V<sub>CC</sub> – 1.5 V

### ORDERING INFORMATION

See "74HC/HCT/HCU/HCMOS Logic Package Information".

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## PIN DESCRIPTION

| PIN NO.                      | SYMBOL                               | NAME AND FUNCTION               |
|------------------------------|--------------------------------------|---------------------------------|
| 1, 2, 3                      | $A_0$ to $A_2$                       | data inputs                     |
| 4                            | $\overline{LE}$                      | latch enable input (active LOW) |
| 5                            | $\overline{E}_1$                     | data enable input (active LOW)  |
| 6                            | $E_2$                                | data enable input (active HIGH) |
| 8                            | GND                                  | ground (0 V)                    |
| 15, 14, 13, 12, 11, 10, 9, 7 | $\overline{Y}_0$ to $\overline{Y}_7$ | multiplexer outputs             |
| 16                           | $V_{CC}$                             | positive supply voltage         |

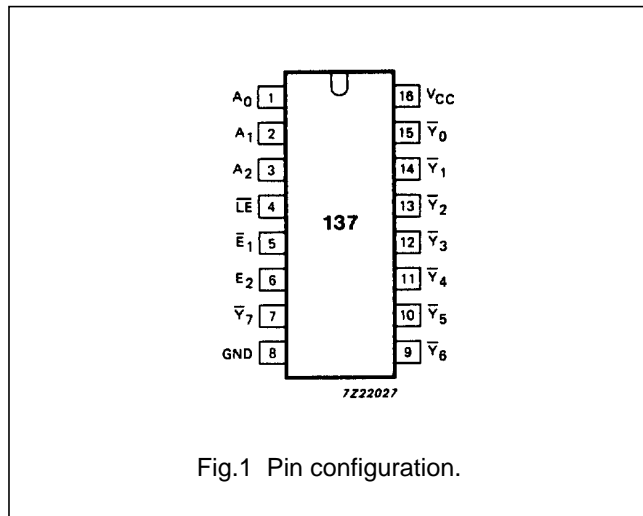


Fig.1 Pin configuration.

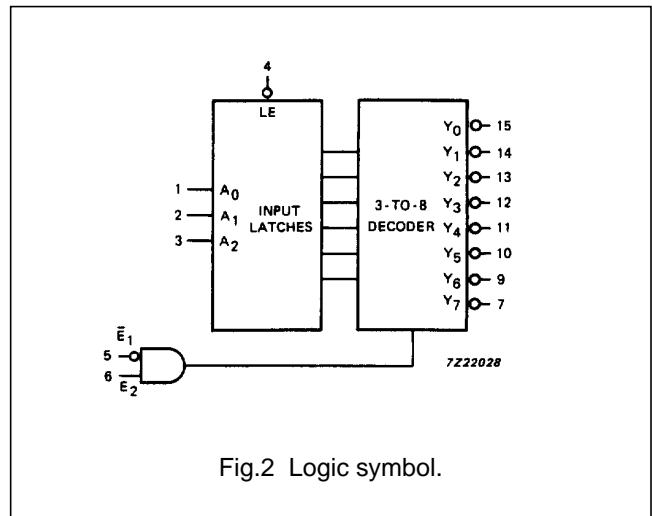


Fig.2 Logic symbol.

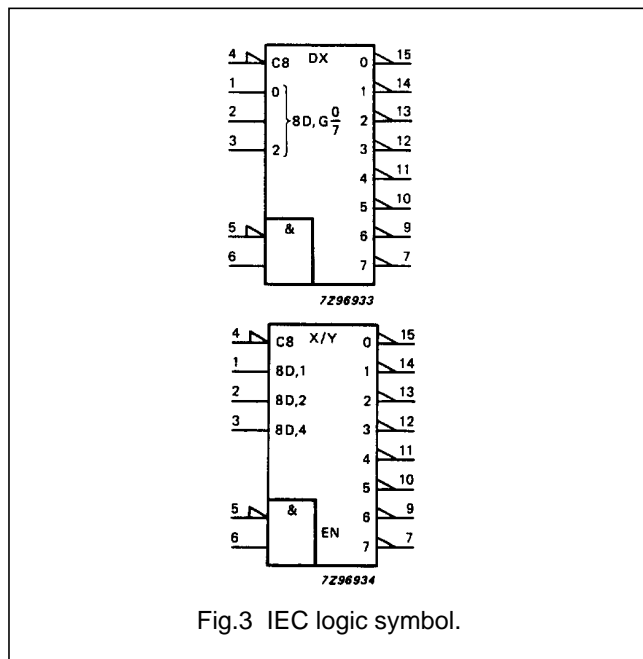


Fig.3 IEC logic symbol.

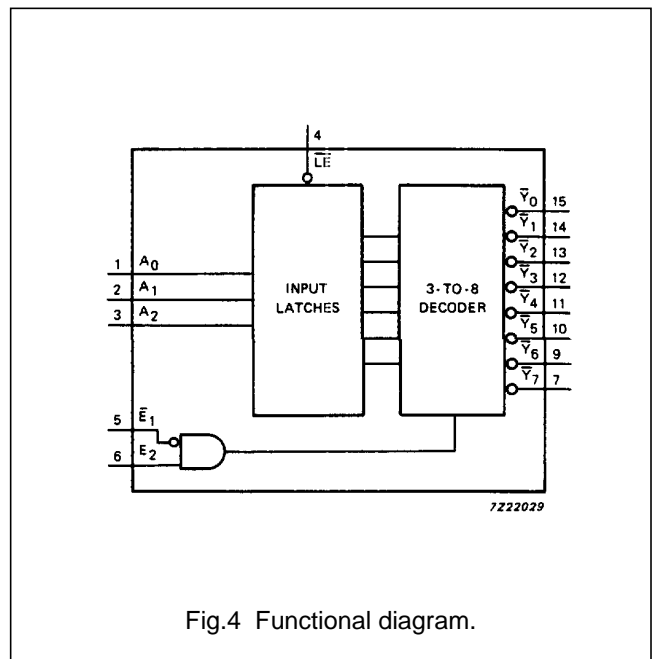


Fig.4 Functional diagram.

# 3-to-8 line decoder/demultiplexer with address latches; inverting

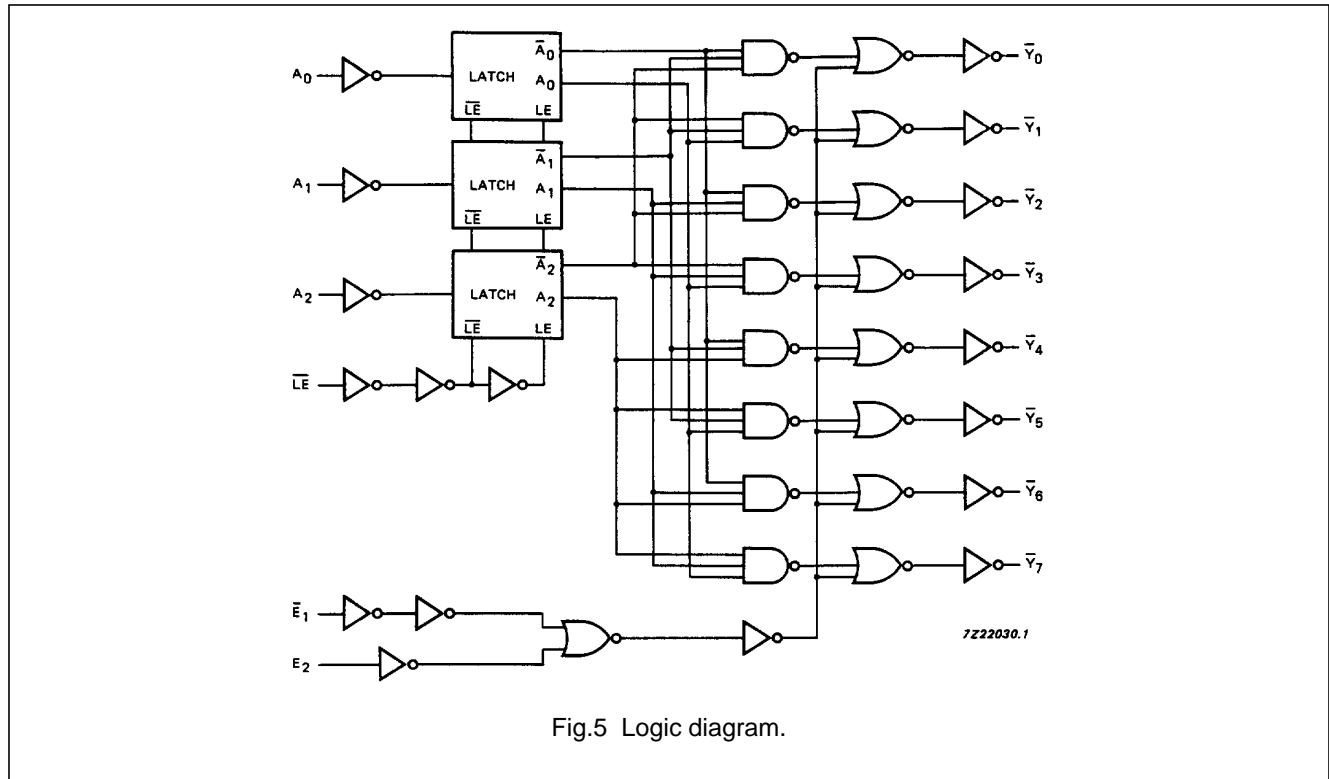
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## FUNCTION TABLE

| INPUTS          |                  |       |       |       |       | OUTPUTS          |                  |                  |                  |                  |                  |                  |                  |
|-----------------|------------------|-------|-------|-------|-------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|
| $\overline{LE}$ | $\overline{E}_1$ | $E_2$ | $A_0$ | $A_1$ | $A_2$ | $\overline{Y}_0$ | $\overline{Y}_1$ | $\overline{Y}_2$ | $\overline{Y}_3$ | $\overline{Y}_4$ | $\overline{Y}_5$ | $\overline{Y}_6$ | $\overline{Y}_7$ |
| H               | L                | H     | X     | X     | X     | stable           |                  |                  |                  |                  |                  |                  |                  |
| X               | H                | X     | X     | X     | X     | H                | H                | H                | H                | H                | H                | H                | H                |
| X               | X                | L     | X     | X     | X     | H                | H                | H                | H                | H                | H                | H                | H                |
| L               | L                | H     | L     | L     | L     | L                | H                | H                | H                | H                | H                | H                | H                |
| L               | L                | H     | H     | L     | L     | H                | L                | H                | H                | H                | H                | H                | H                |
| L               | L                | H     | L     | H     | L     | H                | H                | L                | H                | H                | H                | H                | H                |
| L               | L                | H     | H     | H     | L     | H                | H                | H                | L                | H                | H                | H                | H                |
| L               | L                | H     | L     | L     | H     | H                | H                | H                | H                | L                | H                | H                | H                |
| L               | L                | H     | H     | L     | H     | H                | H                | H                | H                | L                | H                | H                | H                |
| L               | L                | H     | L     | H     | H     | H                | H                | H                | H                | H                | L                | H                | H                |
| L               | L                | H     | H     | H     | H     | H                | H                | H                | H                | H                | H                | L                | H                |

### Notes

- H = HIGH voltage level  
L = LOW voltage level  
X = don't care



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## DC CHARACTERISTICS FOR 74HC

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: standard

I<sub>CC</sub> category: MSI

## AC CHARACTERISTICS FOR 74HC

GND = 0 V; t<sub>r</sub> = t<sub>f</sub> = 6 ns; C<sub>L</sub> = 50 pF

| SYMBOL                              | PARAMETER  | T <sub>amb</sub> (°C) |                |                 |                |                 |                |                 |    | UNIT              | TEST CONDITIONS        |           |
|-------------------------------------|--|-----------------------|----------------|-----------------|----------------|-----------------|----------------|-----------------|----|-------------------|------------------------|-----------|
|                                     |  | 74HC                  |                |                 |                |                 |                |                 |    |                   | V <sub>CC</sub><br>(V) | WAVEFORMS |
|                                     |  | +25                   |                |                 | -40 to +85     |                 | -40 to +125    |                 |    |                   |                        |           |
|                                     |  | min.                  | typ.           | max.            | min.           | max.            | min.           | max.            |    |                   |                        |           |
| t <sub>PHL</sub> / t <sub>PLH</sub> | propagation delay<br>A <sub>n</sub> to $\bar{Y}_n$ |                       | 58<br>21<br>17 | 180<br>36<br>31 |                | 225<br>45<br>38 |                | 270<br>54<br>46 | ns | 2.0<br>4.5<br>6.0 | Fig.6                  |           |
| t <sub>PHL</sub> / t <sub>PLH</sub> | propagation delay<br>$\bar{LE}$ to $\bar{Y}_n$     |                       | 55<br>20<br>16 | 190<br>38<br>32 |                | 240<br>48<br>41 |                | 285<br>57<br>48 | ns | 2.0<br>4.5<br>6.0 | Fig.7                  |           |
| t <sub>PHL</sub> / t <sub>PLH</sub> | propagation delay<br>$\bar{E}_1$ to $\bar{Y}_n$    |                       | 50<br>18<br>14 | 145<br>29<br>25 |                | 180<br>36<br>31 |                | 220<br>44<br>38 | ns | 2.0<br>4.5<br>6.0 | Fig.7                  |           |
| t <sub>PHL</sub> / t <sub>PLH</sub> | propagation delay<br>E <sub>2</sub> to $\bar{Y}_n$ |                       | 50<br>18<br>14 | 145<br>29<br>25 |                | 180<br>36<br>31 |                | 220<br>44<br>38 | ns | 2.0<br>4.5<br>6.0 | Fig.6                  |           |
| t <sub>THL</sub> / t <sub>TLH</sub> | output transition time                             |                       | 19<br>7<br>6   | 75<br>15<br>13  |                | 95<br>19<br>16  |                | 110<br>22<br>19 | ns | 2.0<br>4.5<br>6.0 | Fig.6                  |           |
| t <sub>w</sub>                      | $\bar{LE}$ pulse width<br>HIGH                     | 50<br>10<br>9         | 11<br>4<br>3   |                 | 65<br>13<br>11 |                 | 75<br>15<br>13 |                 | ns | 2.0<br>4.5<br>6.0 | Fig.8                  |           |
| t <sub>su</sub>                     | set-up time<br>A <sub>n</sub> to $\bar{LE}$        | 50<br>10<br>9         | 3<br>1<br>1    |                 | 65<br>13<br>11 |                 | 75<br>15<br>13 |                 | ns | 2.0<br>4.5<br>6.0 | Fig.8                  |           |
| t <sub>h</sub>                      | hold time<br>A <sub>n</sub> to $\bar{LE}$          | 30<br>6<br>5          | 3<br>1<br>1    |                 | 40<br>8<br>7   |                 | 45<br>9<br>8   |                 | ns | 2.0<br>4.5<br>6.0 | Fig.8                  |           |

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## DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: standard

I<sub>CC</sub> category: MSI

### Note to HCT types

The value of additional quiescent supply current ( $\Delta I_{CC}$ ) for a unit load of 1 is given in the family specifications. To determine  $\Delta I_{CC}$  per input, multiply this value by the unit load coefficient shown in the table below.

| INPUT            | UNIT LOAD COEFFICIENT |
|------------------|-----------------------|
| A <sub>n</sub>   | 1.50                  |
| $\overline{E}_1$ | 1.50                  |
| E <sub>2</sub>   | 1.50                  |
| $\overline{LE}$  | 1.50                  |

## AC CHARACTERISTICS FOR 74HCT

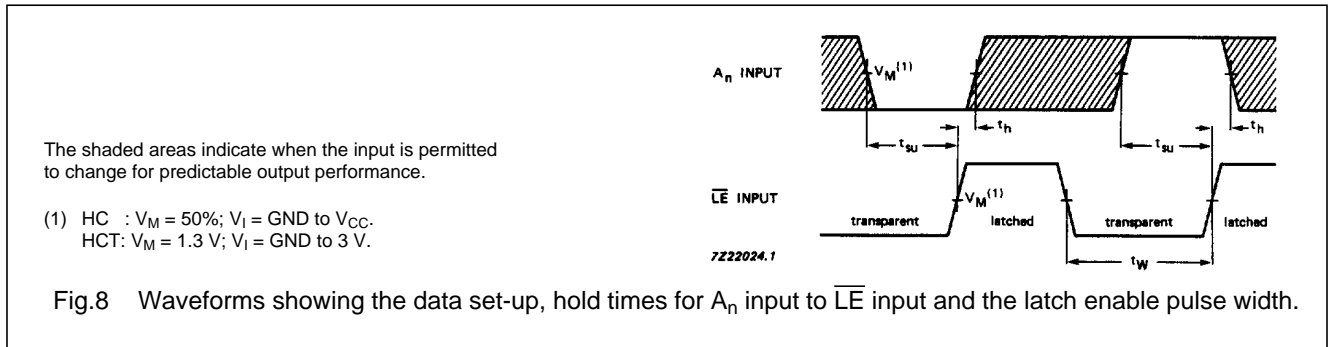
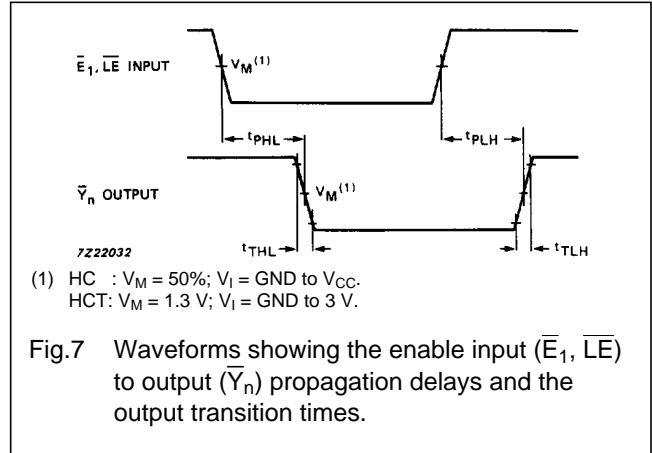
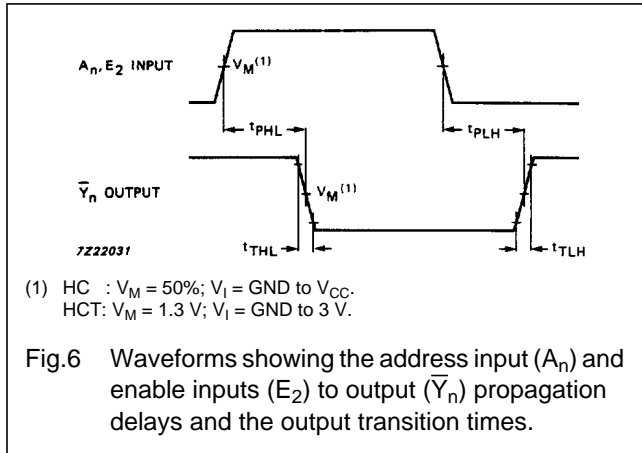
GND = 0 V; t<sub>r</sub> = t<sub>f</sub> = 6 ns; C<sub>L</sub> = 50 pF

| SYMBOL                              | PARAMETER   | T <sub>amb</sub> (°C) |      |      |            |      |             |      | UNIT | TEST CONDITIONS        |           |
|-------------------------------------|---|-----------------------|------|------|------------|------|-------------|------|------|------------------------|-----------|
|                                     |   | 74HCT                 |      |      |            |      |             |      |      | V <sub>CC</sub><br>(V) | WAVEFORMS |
|                                     |   | +25                   |      |      | -40 to +85 |      | -40 to +125 |      |      |                        |           |
|                                     |   | min.                  | typ. | max. | min.       | max. | min.        | max. |      |                        |           |
| t <sub>PHL</sub> / t <sub>PLH</sub> | propagation delay<br>A <sub>n</sub> to $\overline{Y}_n$   |                       | 22   | 38   |            | 48   |             | 57   | ns   | 4.5                    | Fig.6     |
| t <sub>PHL</sub> / t <sub>PLH</sub> | propagation delay<br>$\overline{LE}$ to $\overline{Y}_n$  |                       | 25   | 44   |            | 55   |             | 66   | ns   | 4.5                    | Fig.7     |
| t <sub>PHL</sub> / t <sub>PLH</sub> | propagation delay<br>$\overline{E}_1$ to $\overline{Y}_n$ |                       | 20   | 37   |            | 46   |             | 56   | ns   | 4.5                    | Fig.7     |
| t <sub>PHL</sub> / t <sub>PLH</sub> | propagation delay<br>E <sub>2</sub> to $\overline{Y}_n$   |                       | 18   | 35   |            | 44   |             | 53   | ns   | 4.5                    | Fig.6     |
| t <sub>THL</sub> / t <sub>TLH</sub> | output transition time                                    |                       | 7    | 15   |            | 19   |             | 22   | ns   | 4.5                    | Fig.6     |
| t <sub>w</sub>                      | $\overline{LE}$ pulse width<br>HIGH                       | 10                    | 5    |      | 13         |      | 15          |      | ns   | 4.5                    | Fig.8     |
| t <sub>su</sub>                     | set-up time<br>A <sub>n</sub> to $\overline{LE}$          | 10                    | 2    |      | 13         |      | 15          |      | ns   | 4.5                    | Fig.8     |
| t <sub>h</sub>                      | hold time<br>A <sub>n</sub> to $\overline{LE}$            | 7                     | 2    |      | 9          |      | 11          |      | ns   | 4.5                    | Fig.8     |

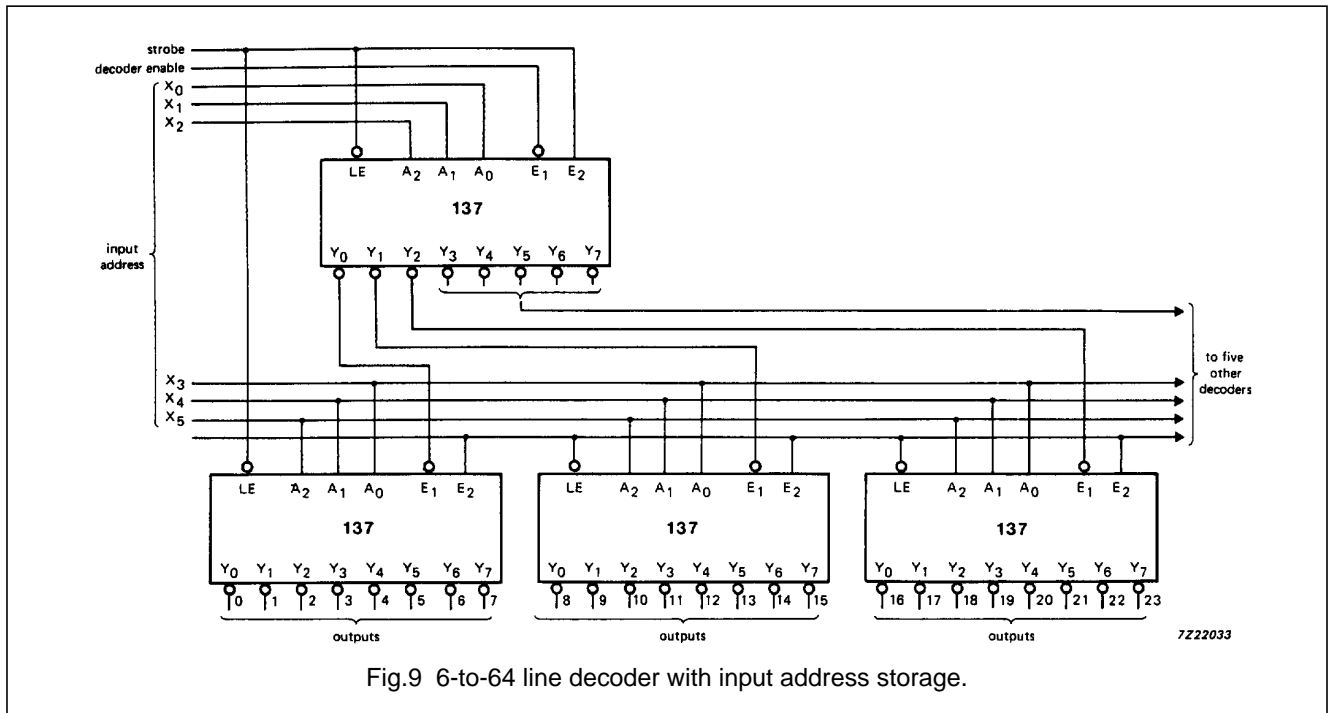
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## AC WAVEFORMS



## APPLICATION INFORMATION



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**PACKAGE OUTLINES**

See *"74HC/HCT/HCU/HCMOS Logic Package Outlines"*.



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