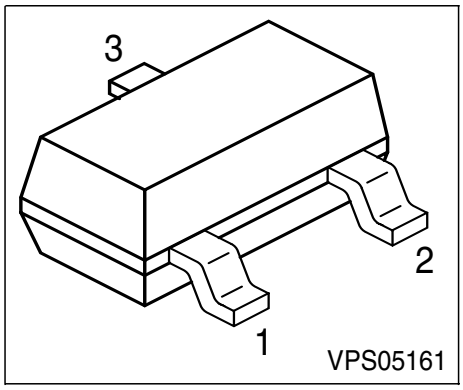
Silicon N-Channel MOSFET Triode

- For high-frequency stages up to 300 MHz preferably in FM applications



ESD: **E**lectro**s**tatic **d**ischarge sensitive device, observe handling precaution!

Type	Marking	Pin Configuration			Package
BF 999	LBs	1 = G	2 = D	3 = S	SOT-23

Maximum Ratings

Parameter	Symbol	Value	Unit
Drain-source voltage	V_{DS}	20	V
Continuos drain current	I_D	30	mA
Gate-source peak current	$\pm I_{GSM}$	10	mA
Total power dissipation, $T_A \leq 60$ °C	P_{tot}	200	mW
Storage temperature	T_{stg}	-55 ... 150	°C
Channel temperature	T_{ch}	150	

Thermal Resistance

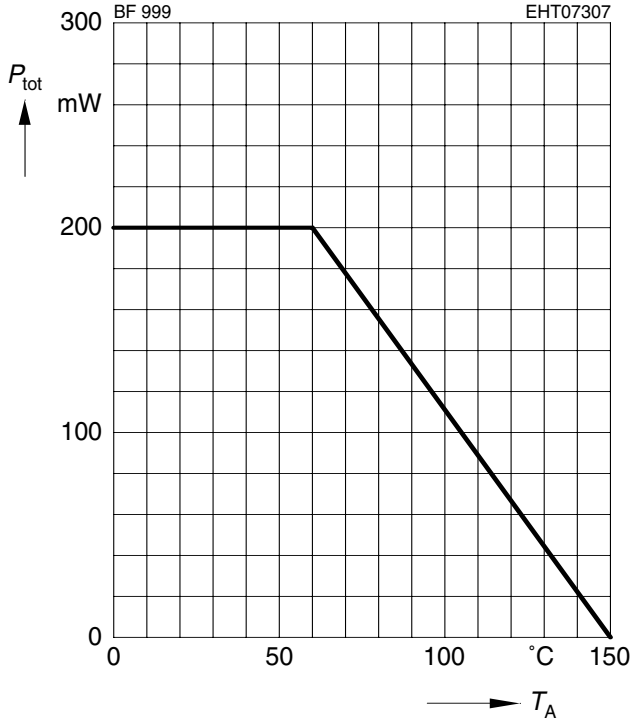
Junction - ambient [1)]	R_{thJA}	≤450	K/W

1) Package mounted on alumina 15mm x 16.7mm x 0.7mm

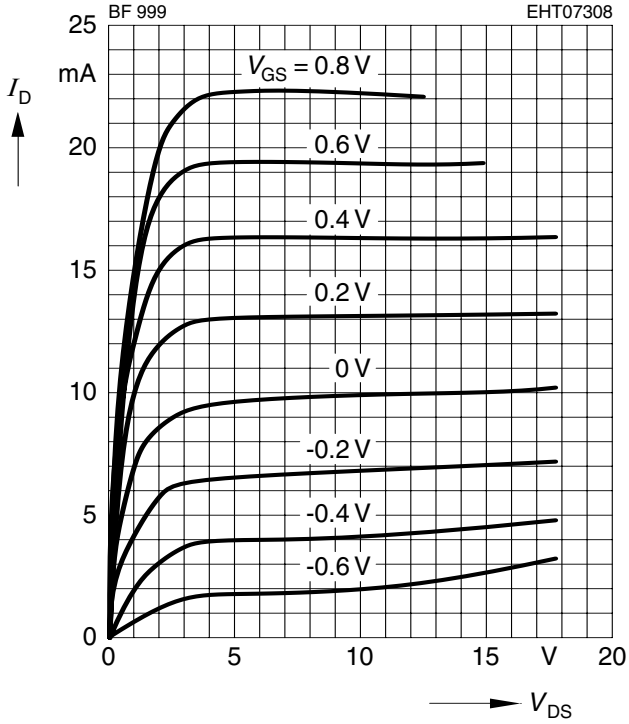
Electrical Characteristics at T_A = 25 °C, unless otherwise specified.

Parameter	Symbol	Values			Unit
		min.	typ.	max.	
DC characteristics					
Drain-source breakdown voltage I_D = 10 µA, - V_{GS} = 4 V	$V_{(BR)DS}$	20	-	-	V
Gate-source breakdown voltage ± I_{GS} = 10 mA, V_{DS} = 0	± $V_{(BR)GSS}$	6.5	-	12	
Gate-source leakage current ± V_{GS} = 5 V, V_{DS} = 0	± I_{GSS}	-	-	50	nA
Drain current V_{DS} = 10 V, V_{GS} = 0	I_{DSS}	5	-	18	mA
Gate-source pinch-off voltage V_{DS} = 10 V, I_D = 20 µA	- $V_{GS\ (p)}$	-	-	2.5	V
AC characteristics					
Forward tranconductance V_{DS} = 10 V, I_D = 10 mA	g_{fs}	14	16	-	mS
Gate input capacitance V_{DS} = 10 V, I_D = 10 mA, f = 1 MHz	C_{gss}	-	2.5	-	pF
Reverse tranfer capacitance V_{DS} = 10 V, I_D = 10 mA, f = 1 MHz	C_{dg}	-	25	-	fF
Output capacitance V_{DS} = 10 V, I_D = 10 mA, f = 1 MHz	C_{dss}	-	1	-	pF
Power gain V_{DS} = 10 V, I_D = 10 mA, f = 200 MHz	G_p	-	25	-	dB
Noise figure V_{DS} = 10 V, I_D = 10 mA, f = 200 MHz	F	-	1	-	

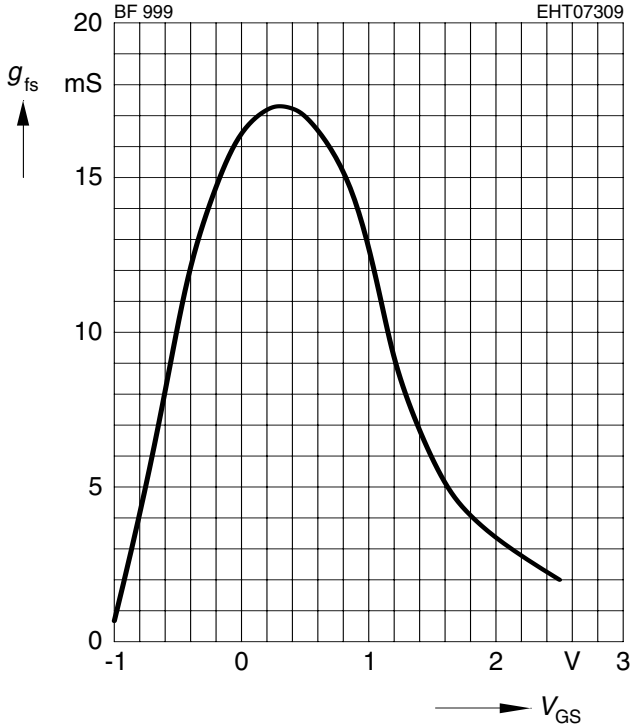
Total power dissipation $P_{tot} = f(T_A)$



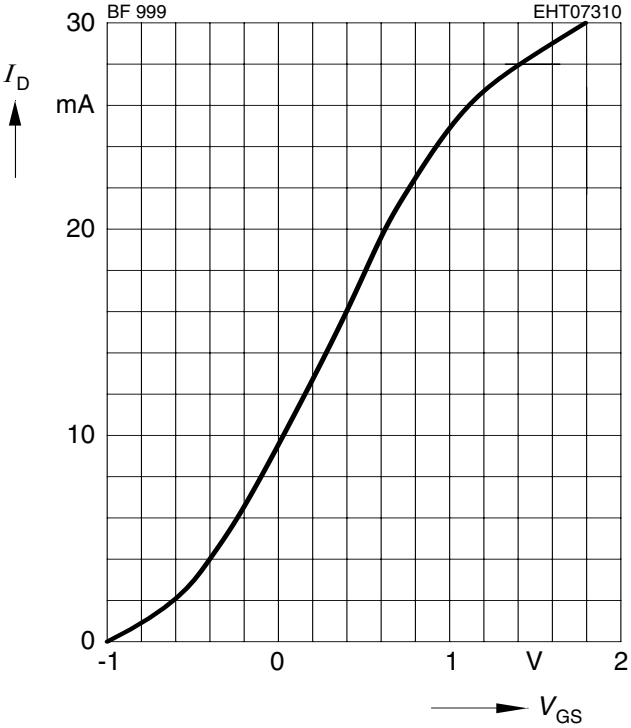
Output characteristics $I_D = f(V_{DS})$



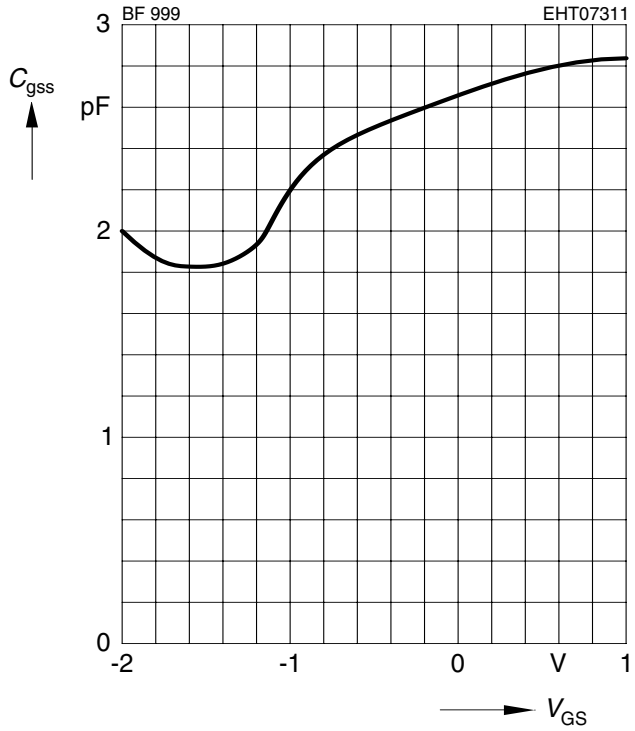
Gate transconductance $g_{fs} = f(V_{GS})$



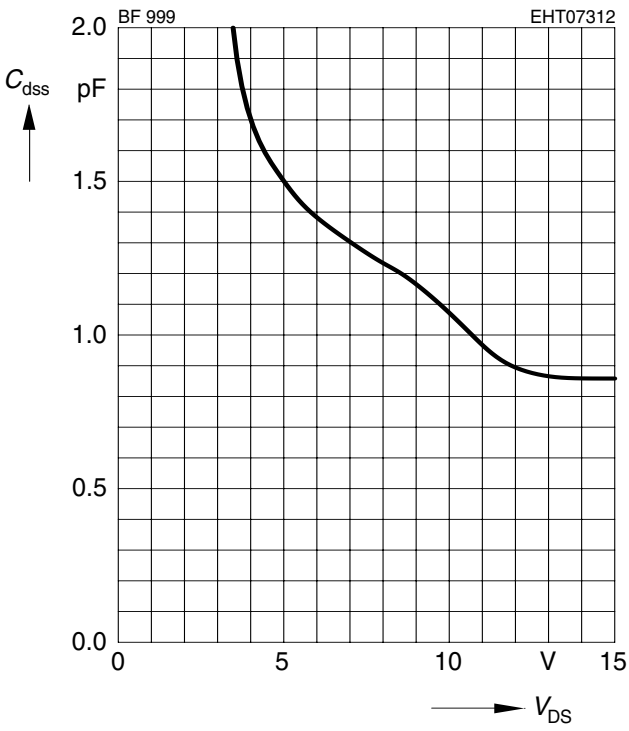
Drain current $I_D = f(V_{GS})$



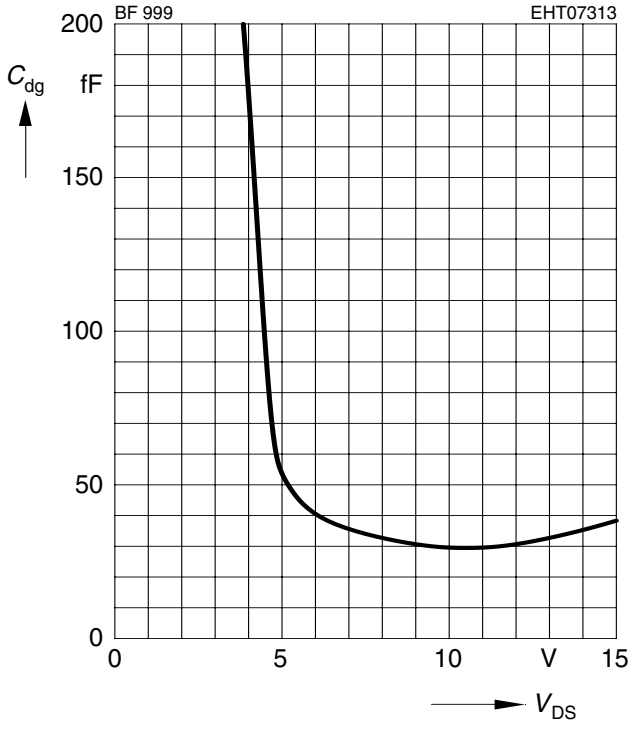
Gate input capacitance $C_{gss} = f(V_{GS})$



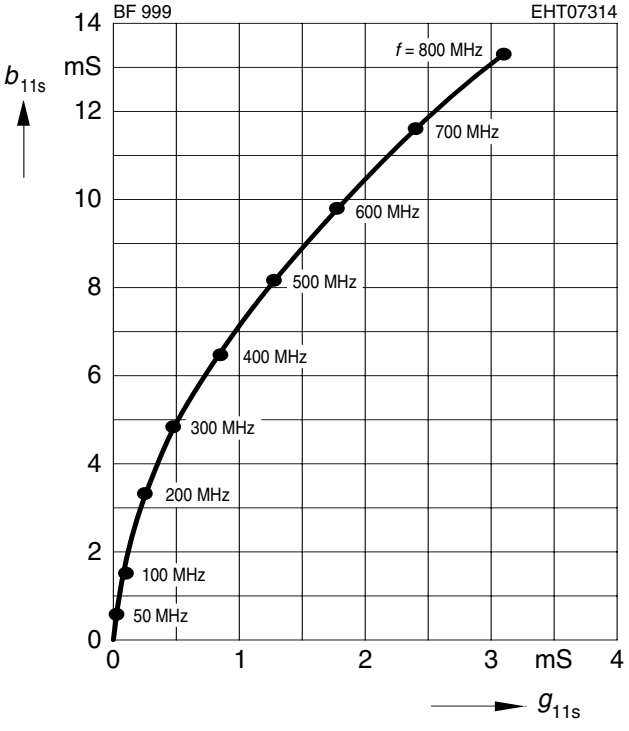
Output capacitance $C_{dss} = f(V_{DS})$



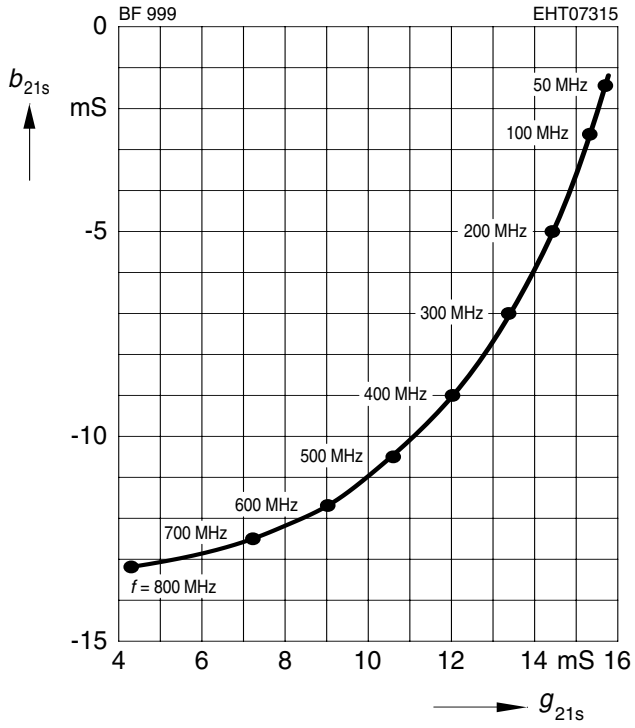
Reverse transfer capacitance
$C_{dg} = f(V_{DS})$



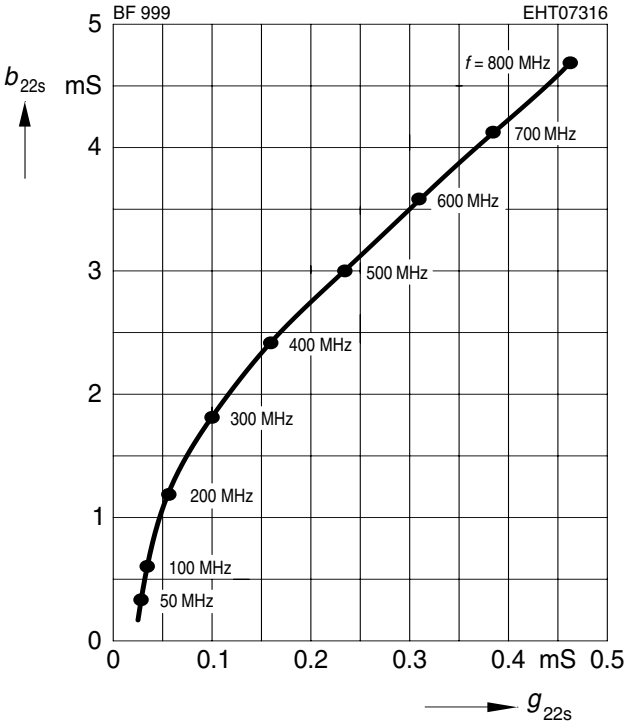
Gate input admittance y_{11s}
(common-source)



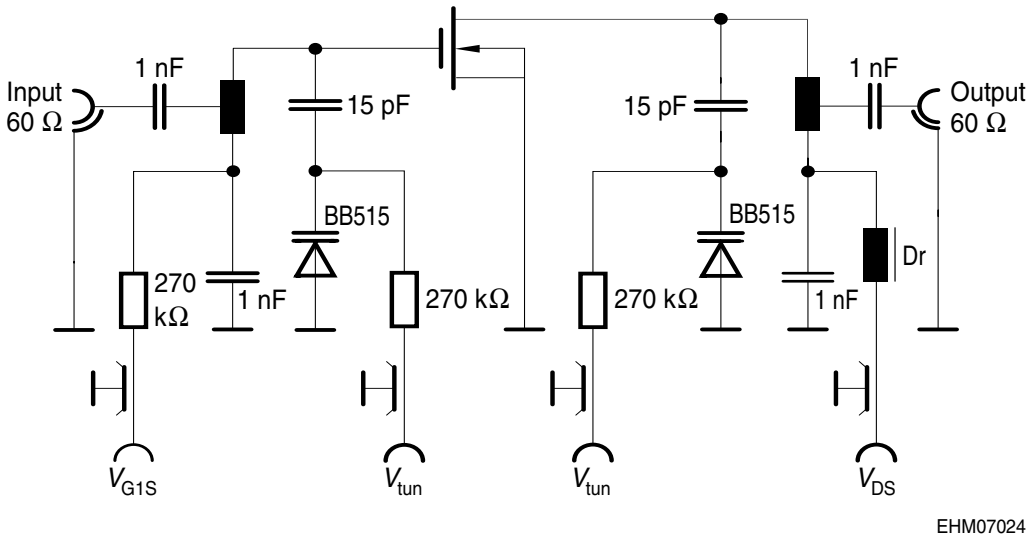
Gate forward transfer admittance y_{21s}
(common-source)



Output admittance y_{22s}
(common-source)



Test circuit for power gain and noise figure
f = 200 MHz



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