

T-39-13

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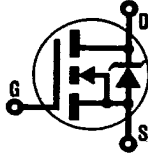
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REPETITIVE AVALANCHE AND dv/dt RATED*
 LOWER ON STATE RESISTANCE, 175°C OPERATING TEMPERATURE

HEXFET® TRANSISTORS

- IRF540**
- IRF541**
- IRF542**
- IRF543**

**N-CHANNEL
 POWER MOSFETs**



**100 Volt, 0.077 Ohm HEXFET
 TO-220AB Plastic Package**

The HEXFET® technology is the key to International Rectifier's advanced line of power MOSFET transistors. The efficient geometry and unique processing of this latest "State of the Art" design achieves: very low on-state resistance combined with high transconductance; superior reverse energy and diode recovery dv/dt capability.

The HEXFET transistors also feature all of the well established advantages of MOSFETs such as voltage control, very fast switching, ease of paralleling and temperature stability of the electrical parameters.

They are well suited for applications such as switching power supplies, motor controls, inverters, choppers, audio amplifiers and high energy pulse circuits.

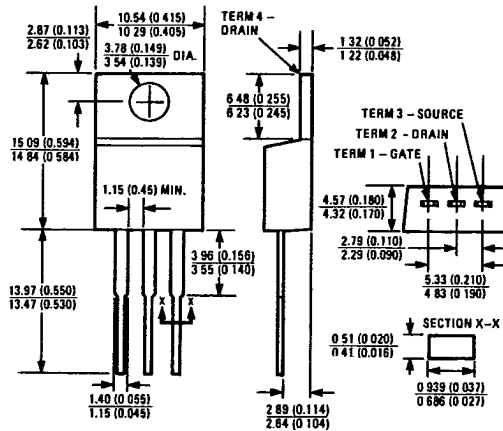
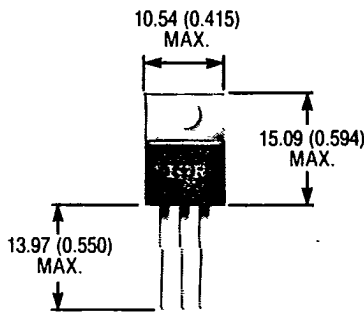
Product Summary

Part Number	BV _{DSS}	R _{DS(on)}	I _D
IRF540	100	0.077	28
IRF541	80	0.077	28
IRF542	100	0.100	25
IRF543	80	0.100	25

FEATURES:

- Repetitive Avalanche Ratings
- Dynamic dv/dt Rating
- Simple Drive Requirements
- Ease of Paralleling

CASE STYLE AND DIMENSIONS



Case Style TO-220AB
 Dimensions in Millimeters and (Inches)

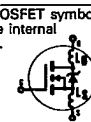
*This data sheet applies to product with batch codes that begin with a digit, ie. 2A3B

Absolute Maximum Ratings

Parameter	IRF540, IRF541	IRF542, IRF543	Units
$I_D @ T_C = 25^\circ\text{C}$ Continuous Drain Current	28	25	A
$I_D @ T_C = 100^\circ\text{C}$ Continuous Drain Current	20	17	A
I_{DM} Pulsed Drain Current $\text{\textcircled{1}}$	110	100	A
$P_D @ T_C = 25^\circ\text{C}$ Max. Power Dissipation	150		W
Linear Derating Factor	1.0		W/K $\text{\textcircled{2}}$
V_{GS} Gate-to-Source Voltage	± 20		V
E_{AS} Single Pulse Avalanche Energy $\text{\textcircled{2}}$	230 (See Fig. 14)		mJ
I_{AR} Avalanche Current $\text{\textcircled{2}}$ (Repetitive or Non-Repetitive)	28 (See E_{AR})		A
E_{AR} Repetitive Avalanche Energy $\text{\textcircled{2}}$	15 (See I_{AR})		mJ
dv/dt Peak Diode Recovery dv/dt $\text{\textcircled{3}}$	5.5 (See Fig. 17)		V/ns
T_J Operating Junction T_{STG} Storage Temperature Range	-55 to 175		$^\circ\text{C}$
Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)		$^\circ\text{C}$

Electrical Characteristics @ $T_J = 25^\circ\text{C}$ (Unless Otherwise Specified)


Parameter	Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS} Drain-to-Source Breakdown Voltage	IRF540 IRF542 IRF541 IRF543	100 80	-	-	V	$V_{GS} = 0V, I_D = 250 \mu\text{A}$
$R_{DS(on)}$ Static Drain-to-Source On-State Resistance $\text{\textcircled{4}}$	IRF540 IRF541 IRF542 IRF543	-	0.060 0.077	0.077 0.100	Ω	$V_{GS} = 10V, I_D = 17A$
$I_{D(on)}$ On-State Drain Current $\text{\textcircled{4}}$	IRF540 IRF541 IRF541 IRF543	28	-	-	A	$V_{DS} > I_{D(on)} \times R_{DS(on)}$ Max. $V_{GS} = 10V$
$V_{GS(th)}$ Gate Threshold Voltage	ALL	2.0	-	4.0	V	$V_{DS} = V_{GS}, I_D = 250 \mu\text{A}$
g_{fs} Forward Transconductance $\text{\textcircled{4}}$	ALL	8.7	13	-	S (D)	$V_{DS} \geq 50V, I_{DS} = 17A$
I_{DSS} Zero Gate Voltage Drain Current	ALL	-	-	250 1000	μA	$V_{DS} = \text{Max. Rating}, V_{GS} = 0V$ $V_{DS} = 0.8 \times \text{Max. Rating}$ $V_{GS} = 0V, T_J = 150^\circ\text{C}$
I_{GSS} Gate-to-Source Leakage Forward	ALL	-	-	500	nA	$V_{GS} = 20V$
I_{GSS} Gate-to-Source Leakage Reverse	ALL	-	-	-500	nA	$V_{GS} = -20V$
Q_g Total Gate Charge	ALL	-	39	59	nC	$V_{GS} = 10V, I_D = 28A$
Q_{gs} Gate-to-Source Charge	ALL	-	7.8	12	nC	$V_{DS} = 0.8 \times \text{Max. Rating}$ See Fig. 16
Q_{gd} Gate-to-Drain ("Miller") Charge		-	19	38	nC	(Independent of operating temperature)
$t_{d(on)}$ Turn-On Delay Time	ALL	-	15	23	ns	$V_{DD} = 50V, I_D = 28A, R_G = 9.1\Omega$
t_r Rise Time	ALL	-	72	110	ns	$R_D = 1.8\Omega$
$t_{d(off)}$ Turn-Off Delay Time	ALL	-	40	60	ns	See Fig. 15
t_f Fall Time	ALL	-	60	75	ns	(Independent of operating temperature)
L_D Internal Drain Inductance	ALL	-	4.5	-	nH	Measured from the drain lead, 6mm (0.25 in.) from package to center of dia.
L_S Internal Source Inductance	ALL	-	7.5	-	nH	Measured from the source lead, 6mm (0.25 in.) from package to source bonding pad.
C_{iss} Input Capacitance	ALL	-	1500	-	pF	$V_{GS} = 0V, V_{DS} = 25V$
C_{oss} Output Capacitance	ALL	-	500	-	pF	$f = 1.0 \text{ MHz}$
C_{rss} Reverse Transfer Capacitance	ALL	-	90	-	pF	See Fig. 10



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Source-Drain Diode Ratings and Characteristics

Parameter	Type	Min.	Typ.	Max.	Units	Test Conditions
I_S Continuous Source Current (Body Diode)	ALL	—	—	28	A	Modified MOSFET symbol showing the integral Reverse p-n junction rectifier. 
I_{SM} Pulsed Source Current (Body Diode) ①	ALL	—	—	110	A	
V_{SD} Diode Forward Voltage ④	ALL	—	—	2.5	V	$T_J = 25^\circ\text{C}$, $I_S = 28\text{A}$, $V_{GS} = 0\text{V}$
t_{rr} Reverse Recovery Time	ALL	70	150	300	ns	$T_J = 25^\circ\text{C}$, $I_F = 28\text{A}$, $di/dt = 100\text{A}/\mu\text{s}$
Q_{RR} Reverse Recovery Charge	ALL	0.44	0.91	1.9	μC	
t_{on} Forward Turn-On Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$.				

Thermal Resistance

R_{thJC} Junction-to-Case	ALL	—	—	1.0	K/W ②	
R_{thCS} Case-to-Sink	ALL	—	0.50	—	K/W ②	Mounting surface flat, smooth, and greased
R_{thJA} Junction-to-Ambient	ALL	—	—	80	K/W ②	Typical socket mount

Typical SPICE Computer Model Parameters (For More Information See Application Note AN-975)

Device	Level, SPICE MOSFET Model	W (m), Channel Width	L (μm), Channel Length	Theta (1/V), Mobility Modulation	UO (CM ² /V-S), Surface Mobility	VTO (V), Threshold Voltage	R1 (Ω), Drain Resistance	R2 (Ω), Source Resistance	RG (Ω), Gate Resistance
All	3	1.226	1.2	0.04	450	3.57	0.18	0.02	0.5

CGSO (pF), Gate-Source Capacitance	CGD (F), Gate-Drain Capacitance	E1 (V), Voltage Dependent Voltage Source	LD (nH), Drain Inductance	LS (nH), Source Inductance	LG (nH), Gate Inductance	IS (A), Diode Saturation Current	RS (Ω), Diode Bulk Resistance
730	C4	4 + 0.95 VDG	4.5	7.5	7.5	8.6×10^{-13}	0.011

$C4 = 1200\text{ pf} + 5.39 \times 10^{-20} (V_{GE})^{20} - 2.45 \times 10^{-21} (V_{GE})^{22}$

- ① Repetitive Rating: Pulse width limited by maximum junction temperature (see figure 5) Refer to current HEXFET reliability report
- ② @ $V_{DD} = 25\text{V}$, Starting $T_J = 25^\circ\text{C}$, $L = 440\ \mu\text{H}$, $R_G = 25\ \Omega$, Peak $I_L = 28\text{A}$.
- ③ $I_{SD} \leq 28\text{A}$, $di/dt \leq 170\text{A}/\mu\text{s}$, $V_{DD} \leq BV_{DSS}$, $T_J \leq 175^\circ\text{C}$, Suggested $R_G = 9.1\ \Omega$
- ④ Pulse width $\leq 300\ \mu\text{s}$; Duty Cycle $\leq 2\%$
- ⑤ $\text{K/W} = \text{K/W}$, $\text{W/K} = \text{W/K}$

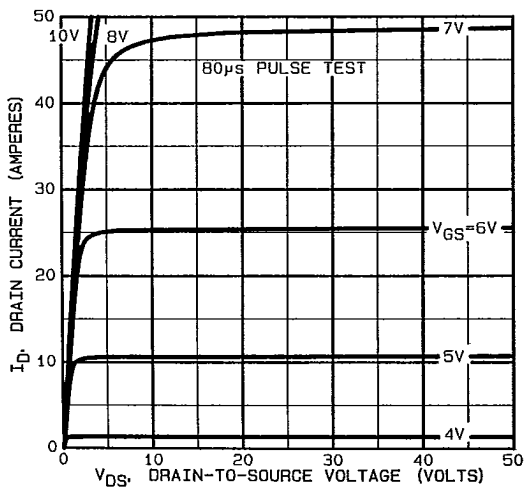


Fig. 1 — Typical Output Characteristics

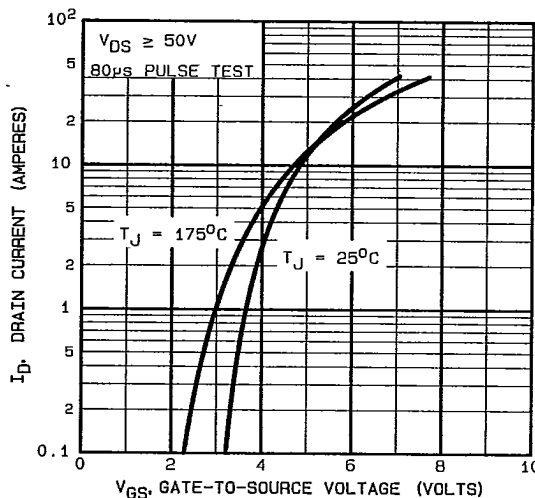


Fig. 2 — Typical Transfer Characteristics

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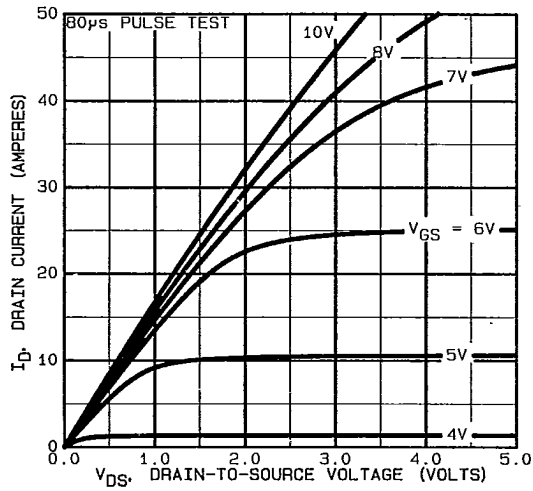


Fig. 3 — Typical Saturation Characteristics

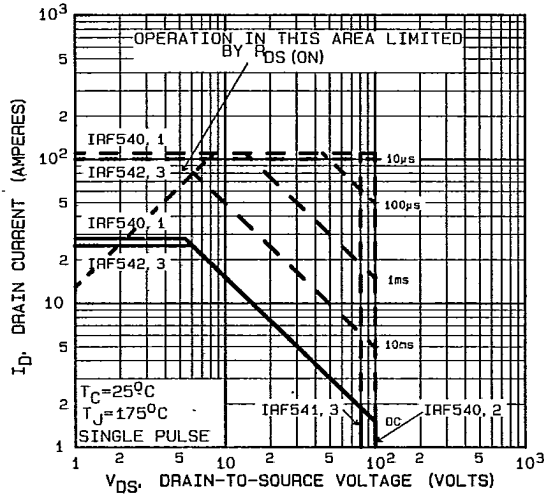


Fig. 4 — Maximum Safe Operating Area

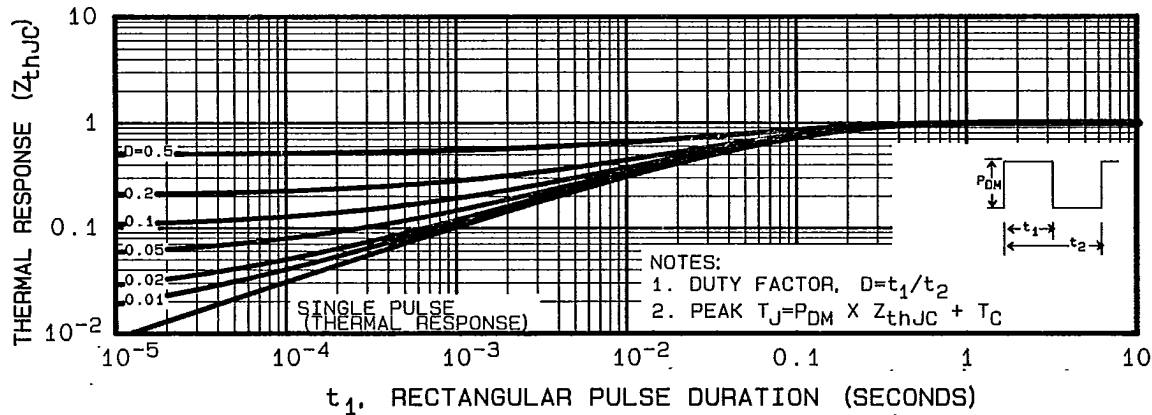


Fig. 5 — Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

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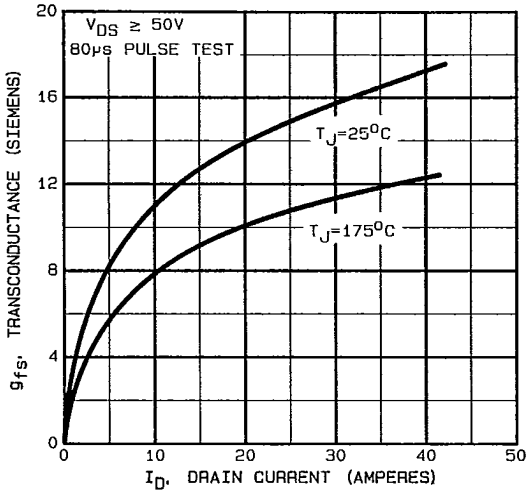


Fig. 6 — Typical Transconductance Vs. Drain Current

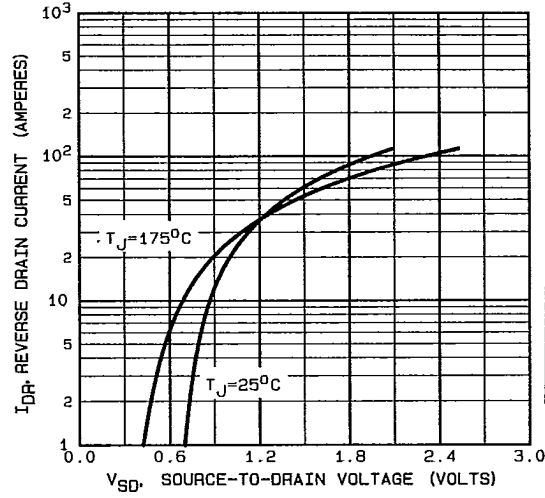


Fig. 7 — Typical Source-Drain Diode Forward Voltage

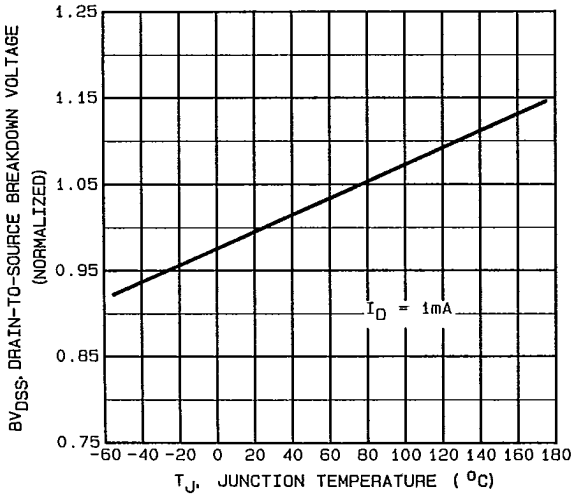


Fig. 8 — Breakdown Voltage Vs. Temperature

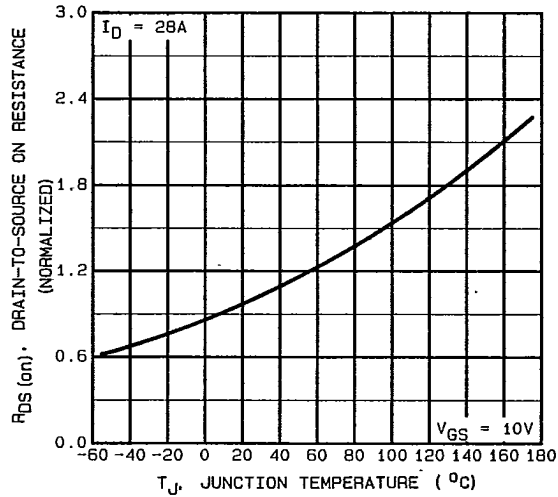


Fig. 9 — Normalized On-Resistance Vs. Temperature

IRF540, IRF541, IRF542, IRF543 Devices

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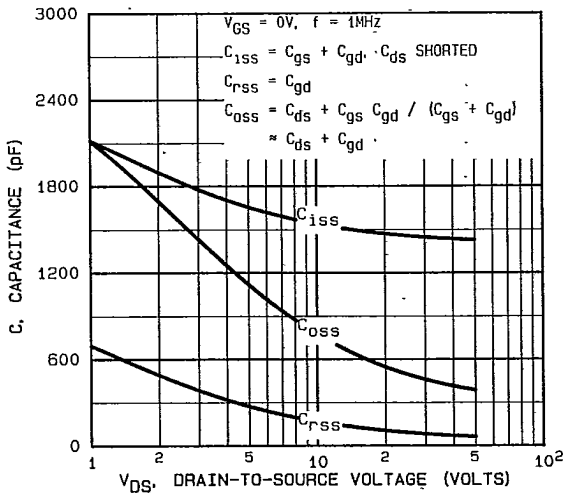


Fig. 10 — Typical Capacitance Vs. Drain-to-Source Voltage

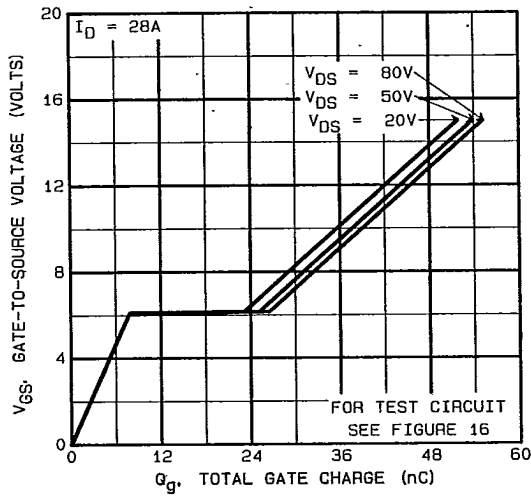


Fig. 11 — Typical Gate Charge Vs. Gate-to-Source Voltage

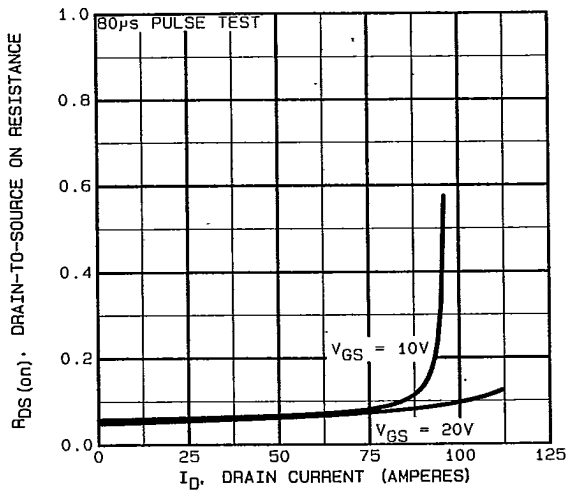


Fig. 12 — Typical On-Resistance Vs. Drain Current

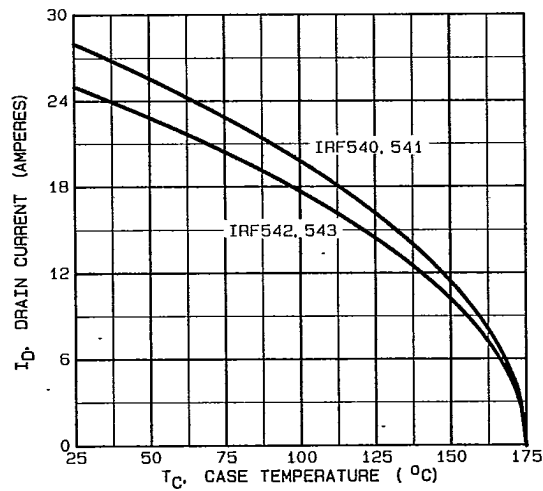


Fig. 13 — Maximum Drain Current Vs. Case Temperature

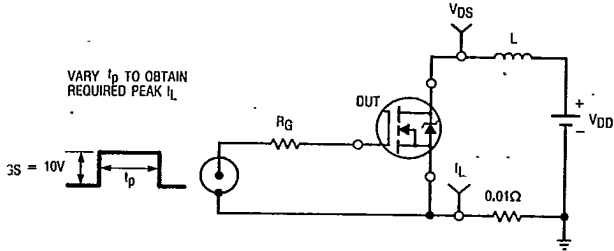


Fig. 14a — Unclamped Inductive Test Circuit

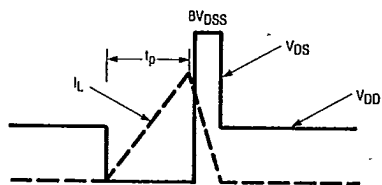


Fig. 14b — Unclamped Inductive Waveforms

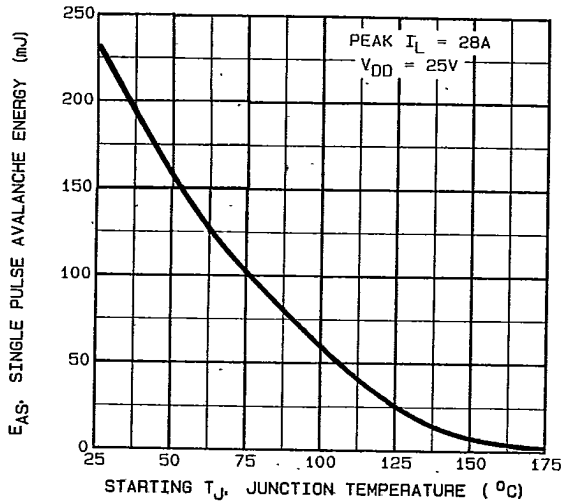


Fig. 14c — Maximum Avalanche Energy Vs. Starting Junction Temperature

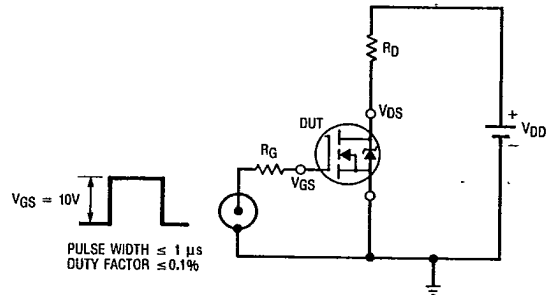


Fig. 15a — Switching Time Test Circuit

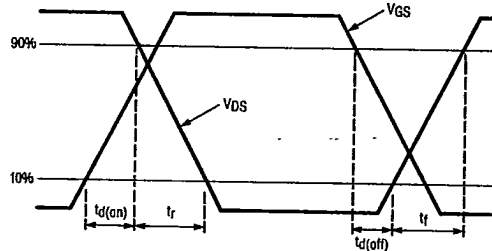


Fig. 15b — Switching Time Waveforms

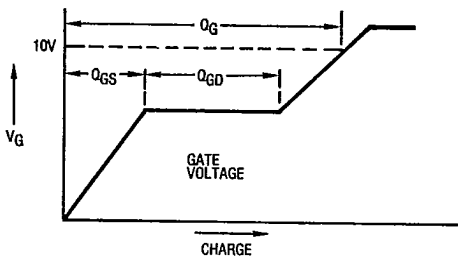


Fig. 16a — Basic Gate Charge Waveform

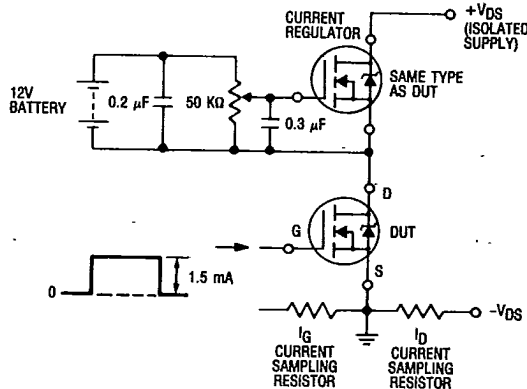


Fig. 16b — Gate Charge Test Circuit

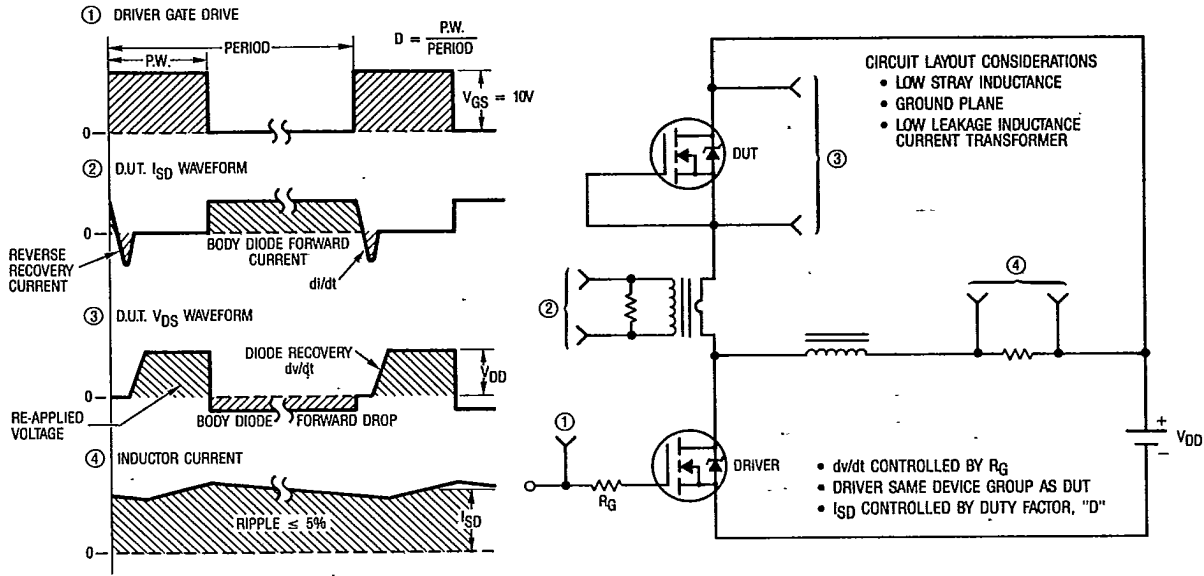
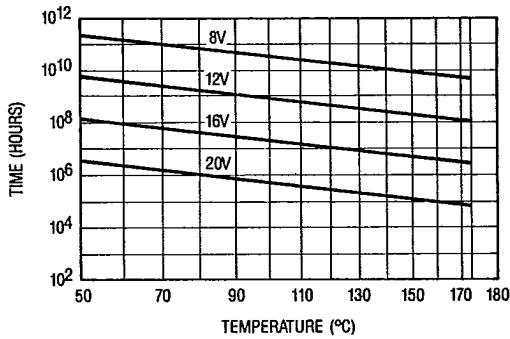
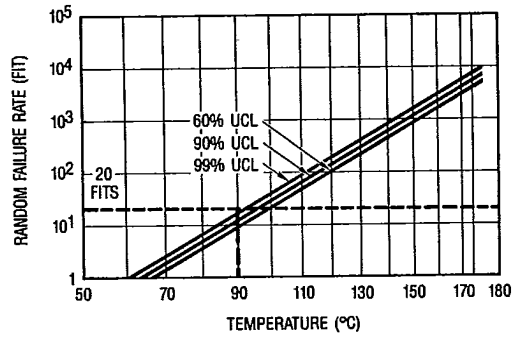


Fig. 17 — Peak Diode Recovery dv/dt Test Circuit



*Fig. 18 — Typical Time to Accumulated 1% Gate Failure



*Fig. 19 — Typical High Temperature Reverse Bias (HTRB) Failure Rate

*The data shown is correct as of January 15, 1987. This information is updated on a quarterly basis; for the latest reliability data, please contact your local IR field office.