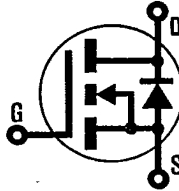


# HEXFET® TRANSISTORS IRFD110

## N-CHANNEL HEXDIP™

1-WATT RATED POWER MOSFETs  
(4 PIN, DUAL-IN-LINE PLASTIC PACKAGE)



IRFD113

4-PIN DIP

### 100 Volt, 0.6 Ohm, 1-Watt HEXDIP

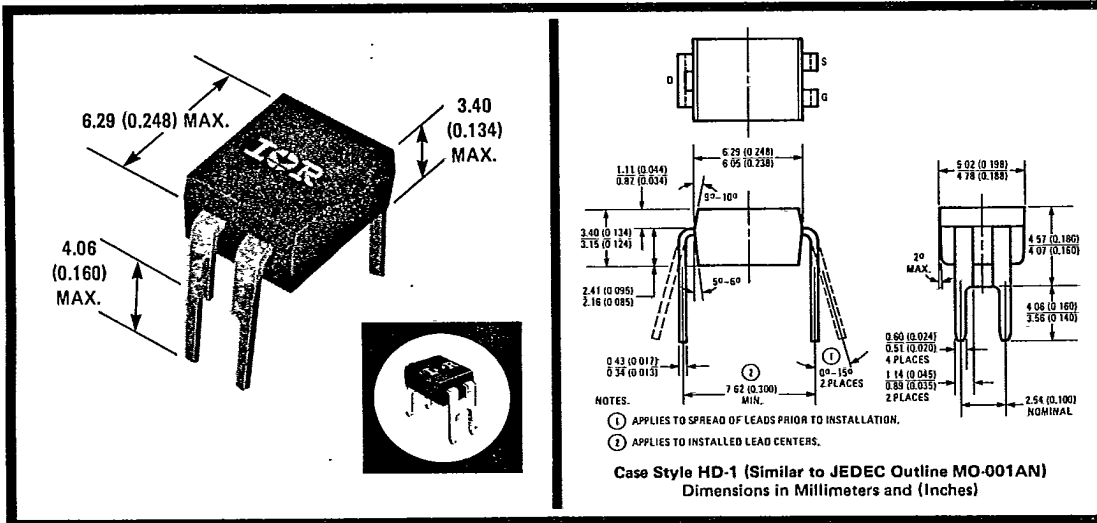
The HEXFET technology is the key to International Rectifier's advanced line of power MOSFET transistors. The efficient geometry and unique processing of the HEXFET design achieve very low on-state resistance combined with high transconductance and great device ruggedness. HEXFETs feature all of the established advantages of MOSFETs such as voltage control, very fast switching, ease of paralleling, and temperature stability of the electrical parameters.

The HEXDIP 4-pin, Dual-In-Line package brings the advantages of HEXFETs to high volume applications where automatic PC Board insertion is desirable, such as circuit boards for computers, printers, telecommunications equipment and consumer products. Their compatibility with automatic insertion equipment, low-profile and end-stackable features represent the state-of-the-art in power device packaging.

- For Automatic Insertion
- Compact Plastic Package
- End Stackable
- Fast Switching
- Low Drive Current
- Easily Paralleled
- Excellent Temperature Stability

### Product Summary

Part Number	V <sub>DS</sub>	R <sub>DS(on)</sub>	I <sub>D</sub>
IRFD110	100V	0.6Ω	1.0A
IRFD113	60V	0.8Ω	0.8A

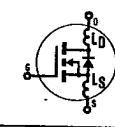


C-117

Absolute Maximum Ratings

Parameter	IRFD110	IRFD113	Units
V <sub>DS</sub> Drain - Source Voltage ①	100	60	V
V <sub>DGR</sub> Drain - Gate Voltage (R <sub>GS</sub> = 20 kΩ) ①	100	60	V
I <sub>D</sub> @ T <sub>A</sub> = 25°C Continuous Drain Current	1.0	0.8	A
I <sub>DM</sub> Pulsed Drain Current	8.0	6.4	A
V <sub>GS</sub> Gate - Source Voltage	± 20		V
P <sub>D</sub> @ T <sub>A</sub> = 25°C Max. Power Dissipation	1.0 (See Fig. 13)		W
Linear Derating Factor	0.008 (See Fig. 13)		W/K ③
L <sub>LM</sub> Inductive Current, Clamped	(See Fig. 14 and 15) L = 100μH		A
T <sub>J</sub> Operating Junction and Storage Temperature Range	-55 to 150		°C
T <sub>stg</sub> Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)		°C

Electrical Characteristics @ T<sub>C</sub> = 25°C (Unless Otherwise Specified)

Parameter	Type	Min.	Typ.	Max.	Units	Test Conditions	
BV <sub>DSS</sub> Drain - Source Breakdown Voltage	IRFD110	100	—	—	V	V <sub>GS</sub> = 0V I <sub>D</sub> = 250μA	
	IRFD113	60	—	—	V		
V <sub>GS(th)</sub> Gate Threshold Voltage	ALL	2.0	—	4.0	V	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250μA	
I <sub>GSS</sub> Gate - Source Leakage Forward	ALL	—	—	500	nA	V <sub>GS</sub> = 20V	
I <sub>GSS</sub> Gate - Source Leakage Reverse	ALL	—	—	-500	nA	V <sub>GS</sub> = -20V	
I <sub>DSS</sub> Zero Gate Voltage Drain Current	ALL	—	—	250	μA	V <sub>DS</sub> = Max. Rating, V <sub>GS</sub> = 0V	
I <sub>D(on)</sub> On-State Drain Current ②	IRFD110	1.0	—	—	A	V <sub>DS</sub> = Max. Rating x 0.8, V <sub>GS</sub> = 0V, T <sub>C</sub> = 125°C	
	IRFD113	0.8	—	—	A		
R <sub>DS(on)</sub> Static Drain-Source On-State Resistance ②	IRFD110	—	0.5	0.6	Ω	V <sub>DS</sub> > I <sub>D(on)</sub> x R <sub>DS(on)</sub> max., V <sub>GS</sub> = 10V	
	IRFD113	—	0.6	0.8	Ω		
g <sub>fs</sub> Forward Transconductance ②	ALL	0.8	1.2	—	S (Ω)	V <sub>DS</sub> > I <sub>D(on)</sub> x R <sub>DS(on)</sub> max., I <sub>D</sub> = 0.8A	
C <sub>iss</sub> Input Capacitance	ALL	—	135	200	pF	V <sub>GS</sub> = 0V, V <sub>DS</sub> = 25V, f = 1.0 MHz See Fig. 9	
C <sub>oss</sub> Output Capacitance	ALL	—	80	100	pF		
C <sub>rss</sub> Reverse Transfer Capacitance	ALL	—	20	25	pF		
t <sub>d(on)</sub> Turn-On Delay Time	ALL	—	10	20	ns	V <sub>DD</sub> = 0.5 BV <sub>DSS</sub> , I <sub>D</sub> = 0.8A, Z <sub>o</sub> = 50Ω See Fig. 16 (MOSFET switching times are essentially independent of operating temperature.)	
t <sub>r</sub> Rise Time	ALL	—	15	25	ns		
t <sub>d(off)</sub> Turn-Off Delay Time	ALL	—	15	25	ns		
t <sub>f</sub> Fall Time	ALL	—	10	20	ns		
Q <sub>g</sub> Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	—	5.0	7.0	nC	V <sub>GS</sub> = 10V, I <sub>D</sub> = 4.0A, V <sub>DS</sub> = 0.8 Max. Rating. See Fig. 17 for test circuit. (Gate charge is essentially independent of operating temperature.)	
Q <sub>gs</sub> Gate-Source Charge	ALL	—	2.0	—	nC		
Q <sub>gd</sub> Gate-Drain ("Miller") Charge	ALL	—	7.0	—	nC		
L <sub>D</sub> Internal Drain Inductance	ALL	—	4.0	—	nH	Measure from the drain lead, 2.0mm (0.08 in.) from package to center of die.	Modified MOSFET symbol showing the internal device inductances. 
L <sub>S</sub> Internal Source Inductance	ALL	—	6.0	—	nH	Measured from the source lead, 2.0mm (0.08 in.) from package to source bonding pad.	

Thermal Resistance

R <sub>thJA</sub> Junction-to-Ambient	ALL	—	—	120	K/W ③	Typical socket mount
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Source-Drain Diode Ratings and Characteristics

Parameter	IRFD110	IRFD113	Units	Test Conditions
I <sub>S</sub> Continuous Source Current (Body Diode)	—	—	1.0	A
I <sub>SM</sub> Pulse Source Current (Body Diode)	—	—	0.8	A
	IRFD110	—	8.0	A
	IRFD113	—	6.4	A
V <sub>SD</sub> Diode Forward Voltage ②	IRFD110	—	2.5	V
	IRFD113	—	2.0	V
t <sub>rr</sub> Reverse Recovery Time	ALL	—	100	ns
Q <sub>RR</sub> Reverse Recovered Charge	ALL	—	0.2	μC
t <sub>on</sub> Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L <sub>S</sub> + L <sub>D</sub> .		

① T<sub>J</sub> = 25°C to 150°C. ② Pulse Test: Pulse width < 300μs, Duty Cycle < 2%. ③ K/W = °C/W, W/K = W/°C

INTERNATIONAL RECTIFIER

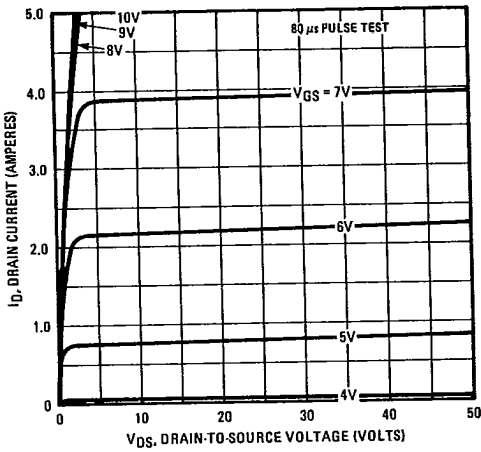


Fig. 1 - Typical Output Characteristics

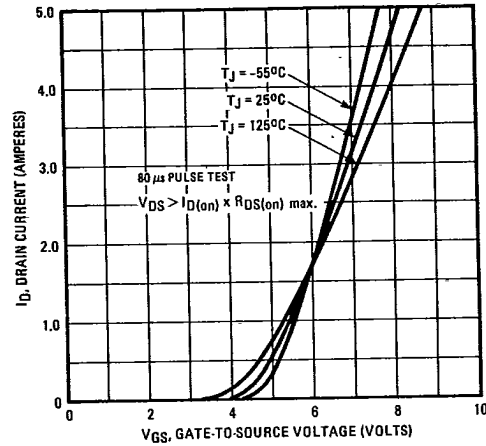


Fig. 2 - Typical Transfer Characteristics

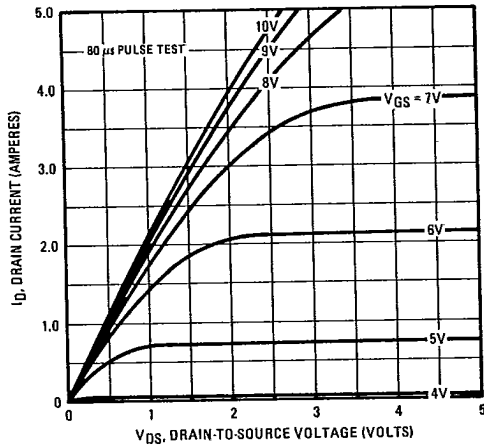


Fig. 3 - Typical Saturation Characteristics

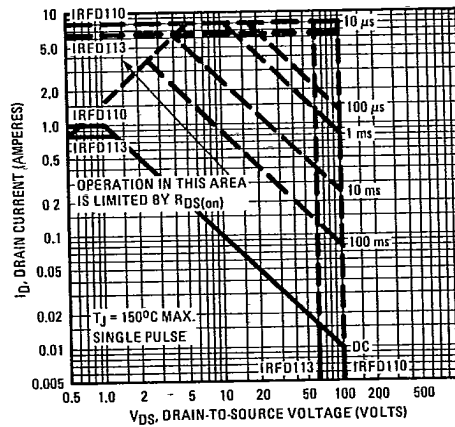


Fig. 4 - Maximum Safe Operating Area



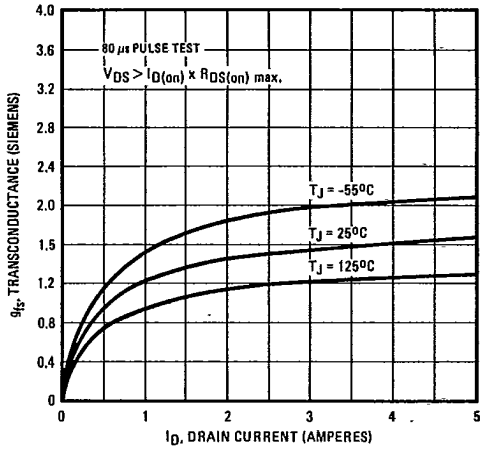


Fig. 5 – Typical Transconductance Vs. Drain Current

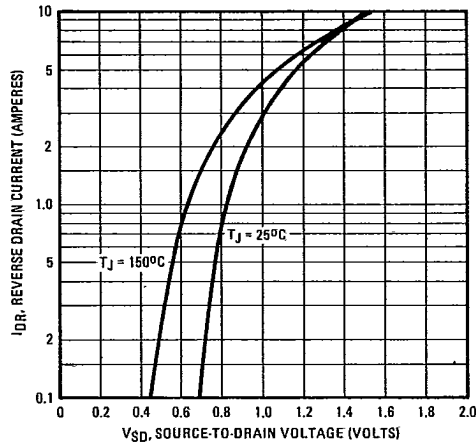


Fig. 6 – Typical Source-Drain Diode Forward Voltage

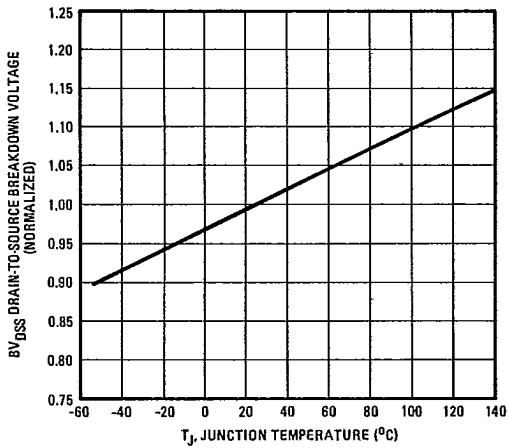


Fig. 7 – Breakdown Voltage Vs. Temperature

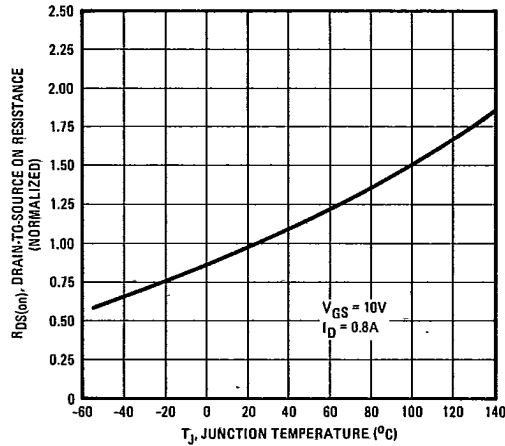


Fig. 8 – Normalized On-Resistance Vs. Temperature

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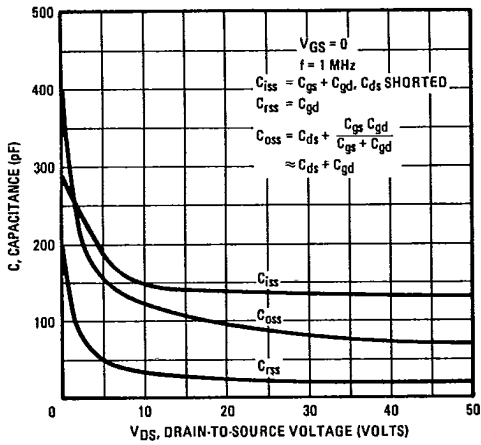


Fig. 9 — Typical Capacitance Vs. Drain-to-Source Voltage

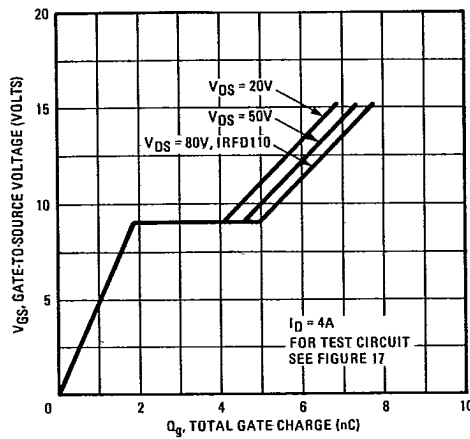


Fig. 10 — Typical Gate Charge Vs. Gate-to-Source Voltage

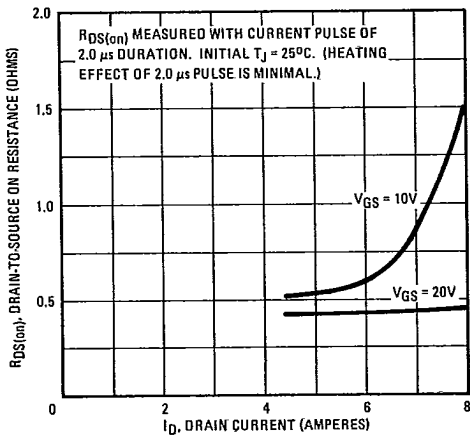


Fig. 11 — Typical On-Resistance Vs. Drain Current

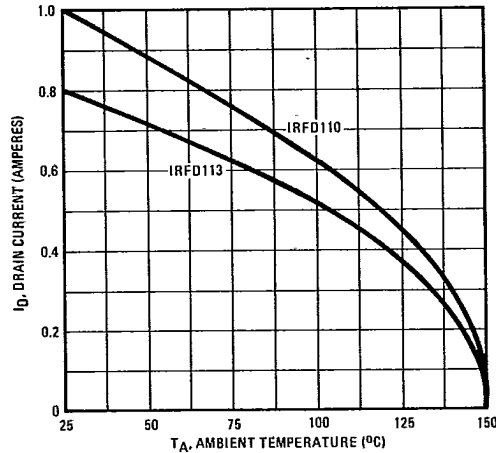


Fig. 12 — Maximum Drain Current Vs. Case Temperature

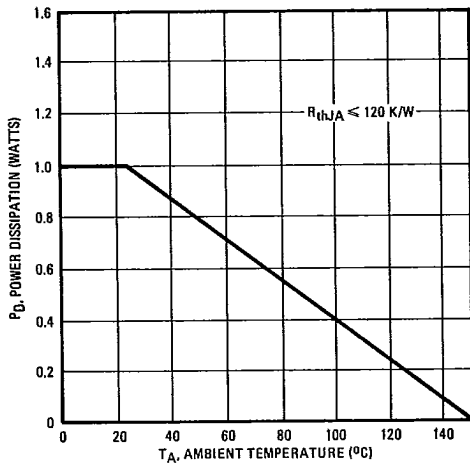


Fig. 13 — Power Vs. Temperature Derating Curve

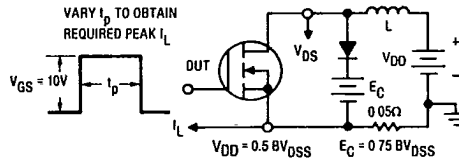


Fig. 14 — Clamped Inductive Test Circuit

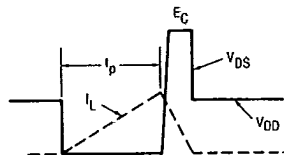


Fig. 15 — Clamped Inductive Waveforms

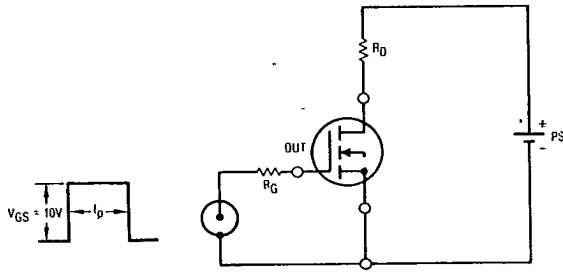


Fig. 16 - Switching Time Test Circuit

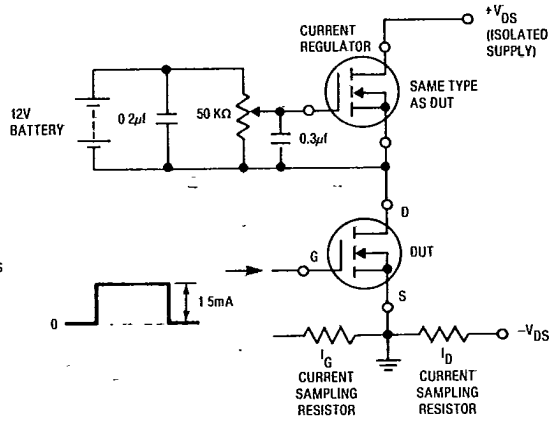
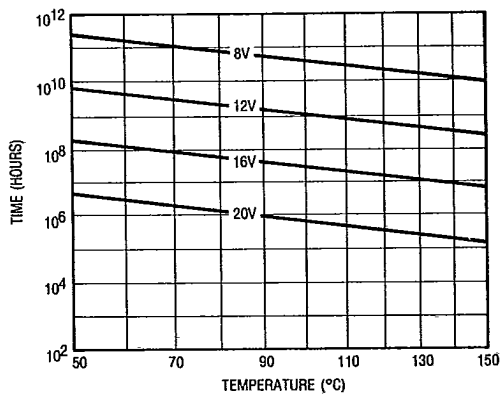
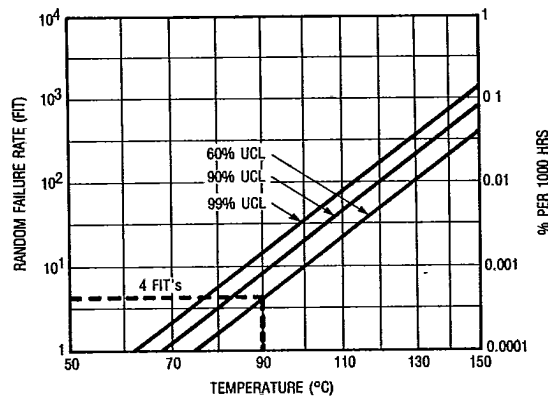


Fig. 17 - Gate Charge Test Circuit



\*Fig. 18 - Typical Time to Accumulated 1% Gate Failure



\*Fig. 19 - Typical High Temperature Reverse Bias (HTRB) Failure Rate

\*The data shown is correct as of April 15, 1987. This information is updated on a quarterly basis; for the latest reliability data, please contact your local IR field office.