



FAST CMOS PARITY BUS TRANSCEIVER

IDT74FCT833A/B

FEATURES:

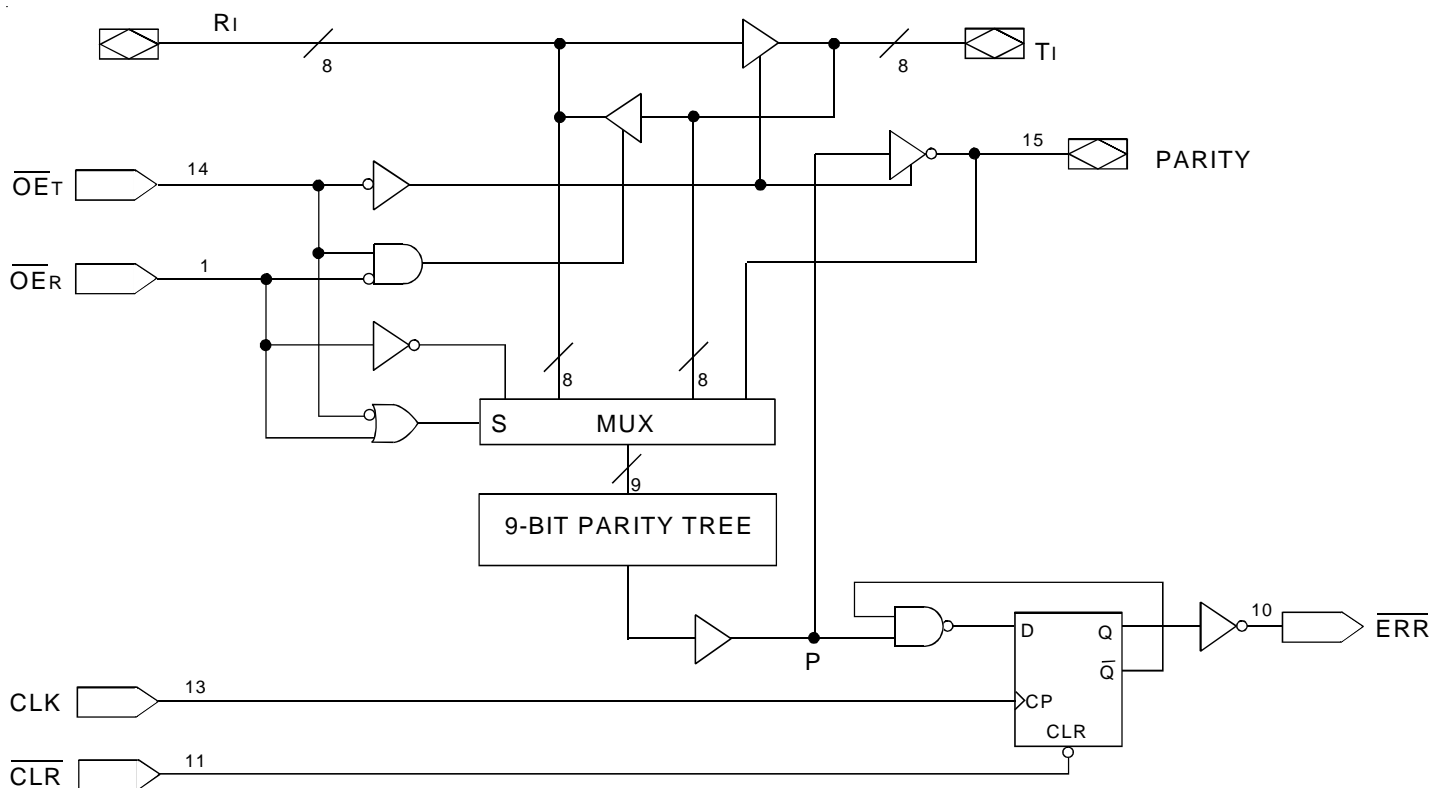
- Equivalent to AMD's Am29833 bipolar registers in pinout/function, speed, and output drive over full temperature and voltage supply extremes
- High-speed bidirectional bus transceiver for processor-organized devices
- IDT74FCT833A equivalent to Am29833 speed and output drive
- IDT74FCT833B 30% faster than Am29833
- Buffered direction and 3-state controls
- Error flag with open-drain output
- $I_{OL} = 48\text{mA}$
- TTL input and output level compatible
- CMOS output level compatible
- Substantially lower input current levels than AMD's bipolar Am29800 series ($5\mu\text{A max.}$)
- Available in SOIC package

DESCRIPTION:

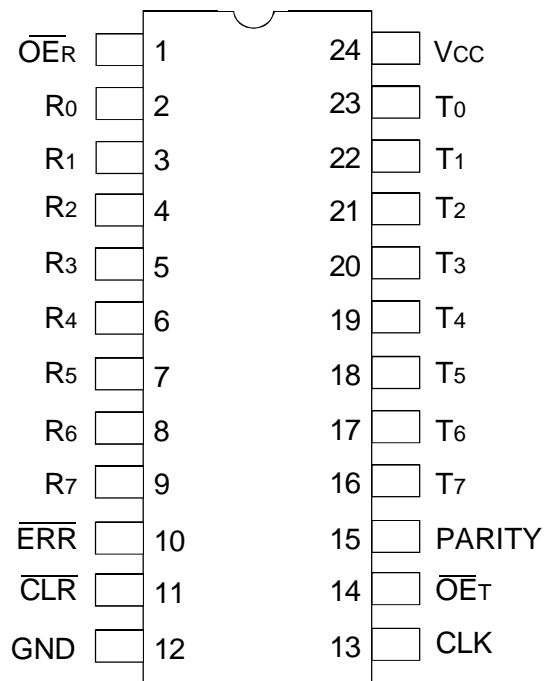
The IDT74FCT833s are high-performance bus transceivers designed for two-way communications. They each contain an 8-bit data path from the R (port) to the T (port), an 8-bit data path from the T (port) to the R (port), and a 9-bit parity checker/generator. The error flag can be clocked and stored in a register and read at the $\overline{\text{ERR}}$ output. The clear ($\overline{\text{CLR}}$) input is used to clear the error flag register.

The output enables $\overline{\text{OE}}_T$ and $\overline{\text{OE}}_R$ are used to force the port outputs to the high-impedance state so that the device can drive bus lines directly. In addition, $\overline{\text{OE}}_R$ and $\overline{\text{OE}}_T$ can be used to force a parity error by enabling both lines simultaneously. This transmission of inverted parity gives the designer more system diagnostic capability. The devices are specified at 48mA output sink current over the commercial temperature range.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



SOIC
TOP VIEW

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Symbol	Description	Max	Unit
VTERM ⁽²⁾	Terminal Voltage with Respect to GND	-0.5 to +7	V
VTERM ⁽³⁾	Terminal Voltage with Respect to GND	-0.5 to V _{CC}	V
T _A	Operating Temperature	0 to +70	°C
T _{BIAS}	Temperature under BIAS	-55 to +125	°C
T _{STG}	Storage Temperature	-55 to +125	°C
P _T	Power Dissipation	0.5	W
I _{OUT}	DC Output Current	120	mA

NOTES:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed V_{CC} by +0.5V unless otherwise noted.
- Input and V_{CC} terminals only.
- Output and I/O terminals only.

CAPACITANCE (T_A = +25°C, F = 1.0MHz)

Symbol	Parameter ⁽¹⁾	Conditions	Typ.	Max.	Unit
C _{IN}	Input Capacitance	V _{IN} = 0V	6	10	pF
C _{OUT}	Output Capacitance	V _{OUT} = 0V	8	12	pF

NOTE:

- This parameter is measured at characterization but not tested.

ERROR FLAG OUTPUT FUNCTION TABLE^(1,2)

Inputs		Internal To Device	Output Pre-State	Output	Function
CLR	CLK	Point "P"	ERR _{n-1}	ERR	
H	↑	H	H	H	Sample (1's Capture)
H	↑	X	L	L	
H	↑	L	X	L	
L	X	X	X	H	Clear

NOTES:

- OE_T is HIGH and OE_R is LOW.
- H = HIGH
L = LOW
↑ = LOW-to-HIGH transition of clock
X = Don't Care

PIN DESCRIPTION

Pin Name	I/O	Description
OE _R	I	RECEIVE enable input.
R _i	I/O	8-bit RECEIVE data input/output.
ERR	O	Output from fault registers. Register detection of odd parity fault on rising clock edge (CLK). A registered ERR output remains LOW until cleared. Open drain output, requires pull up resistor.
CLR	I	Clears the fault register output.
T _i	I/O	8-bit TRANSMIT data input/output.
PARITY	I/O	1-bit PARITY output.
OE _T	I	TRANSMIT enable input.
CLK	I	External clock pulse input for fault register flag.

FUNCTION TABLE⁽¹⁾

Inputs						Outputs				Function
\overline{OE}_T	\overline{OE}_R	\overline{CLR}	CLK	Ri (Σ or H's)	Ti Incl Parity (Σ of H's)	Ri	Ti	Parity	$\overline{ERR}^{(2)}$	
L	H	H	↑	H (Odd)	NA	NA	H	L	H	Transmit data from R Port to T Port with parity; receiving path is disabled.
L	H	H	↑	H (Even)	NA	NA	H	H	L	
L	H	H	↑	L (Odd)	NA	NA	L	L	H	
L	H	H	↑	L (Even)	NA	NA	L	H	L	
H	L	H	↑	NA	H (Odd)	H	NA	NA	H	Receive data from T Port to R Port with parity test resulting in flag; transmitting path is disabled.
H	L	H	↑	NA	H (Even)	H	NA	NA	L	
H	L	H	↑	NA	L (Odd)	L	NA	NA	H	
H	L	H	↑	NA	L (Even)	L	NA	NA	L	
X	X	L	X	X	X	NA	NA	NA	H	Clear the state of error flag register.
H	H	H	H or L	X	X	Z	Z	Z	*	Both transmitting and receiving paths are disabled. Parity logic defaults to transmit mode.
H	H	L	X	X	X	Z	Z	Z	H	
H	H	H	↑	H or L (Odd)	X	Z	Z	Z	H	
H	H	H	↑	H or L (Even)	X	Z	Z	Z	L	
L	L	H	↑	H (Odd)	NA	NA	H	H	L	Forced-error checking.
L	L	H	↑	H (Even)	NA	NA	H	L	H	
L	L	H	↑	L (Odd)	NA	NA	L	H	L	
L	L	H	↑	L (Even)	NA	NA	L	L	H	

NOTES:

- H = HIGH
 Z = High-Impedance
 Odd = Odd number of logic one's
 L = LOW
 NA = Not Applicable
 Even = Even number of logic one's
 ↑ = LOW-to-HIGH transition of clock
 X = Don't Care
 I = 0, 1, 2, 3, 4, 5, 6, 7
 * = No change to stored Error State
- Output state assumes HIGH output pre-state.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified: $V_{LC} = 0.2V$; $V_{HC} = V_{CC} - 0.2V$

Commercial: $T_A = 0^\circ C$ to $+70^\circ C$, $V_{CC} = 5.0V \pm 5\%$

Symbol	Parameter	Test Conditions ⁽¹⁾	Min.	Typ. ⁽²⁾	Max.	Unit			
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level	2	—	—	V			
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level	—	—	0.8	V			
I_{IH}	Input HIGH Current (Except I/O Pins)	$V_{CC} = \text{Max.}$	$V_I = V_{CC}$	—	—	5	μA		
			$V_I = 2.7V$	—	—	$5^{(4)}$			
			$V_I = 0.5V$	—	—	$-5^{(4)}$			
I_{IL}	Input LOW Current (Except I/O Pins)	$V_{CC} = \text{Max.}$	$V_I = GND$	—	—	-5	μA		
			$V_I = V_{CC}$	—	—	15			
			$V_I = 2.7V$	—	—	$15^{(4)}$			
		$V_{CC} = \text{Max.}$	$V_I = 0.5V$	—	—	$-15^{(4)}$	μA		
			$V_I = GND$	—	—	-15			
V_{IK}	Clamp Diode Voltage	$V_{CC} = \text{Min.}, I_N = -18mA$	—	-0.7	-1.2	V			
I_{OS}	Short Circuit Current	$V_{CC} = \text{Max.}^{(3)}, V_O = GND$	-60	-120	—	mA			
V_{OH}	Output HIGH Voltage (Except \overline{ERR})	$V_{CC} = 3V, V_{IN} = V_{LC} \text{ or } V_{HC}, I_{OH} = -32\mu A$		V_{HC}	V_{CC}	—	V		
		$V_{CC} = \text{Min.}$ $V_{IN} = V_{IH} \text{ or } V_{IL}$	$I_{OH} = -300\mu A$		V_{HC}	V_{CC}		—	
			$I_{OH} = -24mA$		2.4	4.3		—	
V_{OL}	Output LOW Voltage	$V_{CC} = 3V, V_{IN} = V_{LC} \text{ or } V_{HC}, I_{OL} = 300\mu A$		—	GND	V_{LC}	v		
		$V_{CC} = \text{Min.}$ $V_{IN} = V_{IH}$ or V_{IL}	Except \overline{ERR}	$I_{OL} = 300\mu A$		—		GND	$V_{LC}^{(4)}$
				$I_{OL} = 48mA$		—		0.3	0.5
			\overline{ERR}		$I_{OL} = 48mA$			—	0.3

NOTES:

- For conditions shown as Min. or Max., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at $V_{CC} = 5.0V$, $+25^\circ C$ ambient and maximum loading.
- Not more than one output should be tested at one time. Duration of the test should not exceed one second.
- This parameter is guaranteed but not tested.

POWER SUPPLY CHARACTERISTICS

$V_{LC} = 0.2V$; $V_{HC} = V_{CC} - 0.2V$

Symbol	Parameter	Test Conditions ⁽¹⁾	Min.	Typ. ⁽²⁾	Max.	Unit	
I _{CC}	Quiescent Power Supply Current	$V_{CC} = \text{Max.}; V_{IN} \geq V_{HC}, V_{IN} \leq V_{LC}$	—	0.2	1.5	mA	
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	$V_{CC} = \text{Max.}$ $V_{IN} = 3.4V^{(3)}$	—	0.5	2	mA	
I _{CCD}	Dynamic Power Supply Current ⁽⁴⁾ Outputs Open	$V_{CC} = \text{Max.}$ $V_{IN} \leq V_{LC}$ $\overline{OE}_T = \overline{OE}_R = \text{GND}$ One Input Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$	—	0.15	0.25 mA/ MHz	
I _C	Total Power Supply Current ⁽⁶⁾	$V_{CC} = \text{Max.}$ Outputs Open $f_{CP} = 10\text{MHz}$ 50% Duty Cycle $\overline{OE}_T = \text{GND}$ $\overline{OE}_R = V_{CC}$ $f_i = 2.5\text{MHz}$ One Bit Toggling	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	—	1.4	3.4	mA
			$V_{IN} = 3.4V$ $V_{IN} = \text{GND}$	—	1.9	5.4	
		$V_{CC} = \text{Max.}$ Outputs Open $f_{CP} = 10\text{MHz}$ 50% Duty Cycle $\overline{OE}_T = \text{GND}$ $f_i = 2.5\text{MHz}$ $\overline{OE}_R = V_{CC}$ Eight Bits Toggling	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	—	4	7.8 ⁽⁵⁾	
			$V_{IN} = 3.4V$ $V_{IN} = \text{GND}$	—	6.2	16.8 ⁽⁵⁾	

NOTES:

1. For conditions shown as Min. or Max., use appropriate value specified under Electrical Characteristics for the applicable device type.

2. Typical values are at $V_{CC} = 5.0V$, +25°C ambient.

3. Per TTL driven input ($V_{IN} = 3.4V$). All other inputs at V_{CC} or GND.

4. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.

5. Values for these conditions are examples of ΔI_{CC} formula. These limits are guaranteed but not tested.

6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$

$I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$

I_{CC} = Quiescent Current

ΔI_{CC} = Power Supply Current for a TTL High Input ($V_{IN} = 3.4V$)

D_H = Duty Cycle for TTL Inputs High

N_T = Number of TTL Inputs at D_H

I_{CCD} = Dynamic Current caused by an Input Transition Pair (HLH or LHL)

f_{CP} = Clock Frequency for register devices (zero for non-register devices)

f_i = Input Frequency

N_i = Number of Inputs at f_i

All currents are in milliamps and all frequencies are in megahertz.

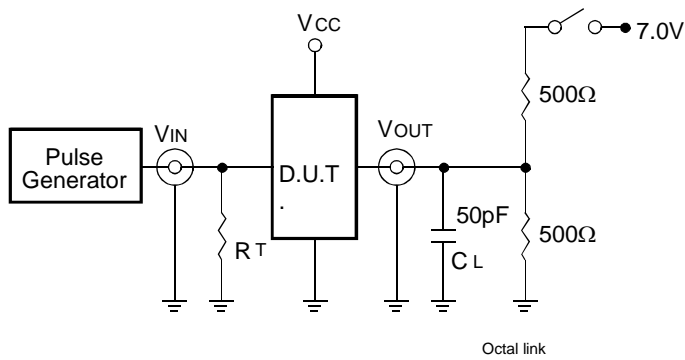
SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Symbol	Parameter	Conditions ⁽¹⁾	IDT74FCT833A		IDT74FCT833B		Unit	
			Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.		
t _{PLH}	Propagation Delay	CL = 50pF	—	10	—	7	ns	
t _{PHL}	Ri to Ti, Ti to Ri	CL = 300pF ⁽³⁾	—	17.5	—	14.5		
t _{PLH}	Propagation Delay	CL = 50pF	—	15	—	10.5	ns	
t _{PHL}	Ri to PARITY	CL = 300pF ⁽³⁾	—	22.5	—	18		
t _{PZH}	Output Enable Time	CL = 50pF	—	12	—	8.5	ns	
t _{PZL}	$\overline{OE}_R, \overline{OE}_T$ to Ri, Ti	CL = 300pF ⁽³⁾	—	19.5	—	16		
t _{PHZ}	Output Disable Time	CL = 5pF ⁽³⁾	—	10.7	—	7.2	ns	
t _{PLZ}	$\overline{OE}_R, \overline{OE}_T$ to Ri, Ti	CL = 50pF	—	12	—	8.5		
t _{SU}	Ti, PARITY to CLK Set-up Time	CL = 50pF	12	—	8.5	—	ns	
t _H	Ti, PARITY to CLK Hold Time		0	—	0	—	ns	
t _{REM}	Clear Recovery Time \overline{CLR} to CLK		15	—	10.5	—	ns	
t _w	Clock Pulse Width HIGH or LOW		7	—	5.5	—	ns	
t _w	Clear Pulse Width LOW		7	—	5.5	—	ns	
t _{PHL}	Propagation Delay CLK to \overline{ERR}		—	12	—	8.5	ns	
t _{PLH}	Propagation Delay \overline{CLR} to \overline{ERR}		—	16	—	15	ns	
t _{PLH}	Propagation Delay		CL = 50pF	—	15	—	10.5	ns
t _{PHL}	\overline{OE}_R to PARITY		CL = 300pF ⁽³⁾	—	22.5	—	18	

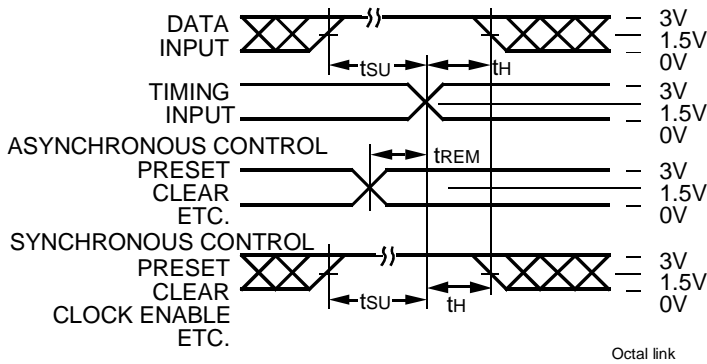
NOTES:

1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. These parameters are guaranteed but not tested.

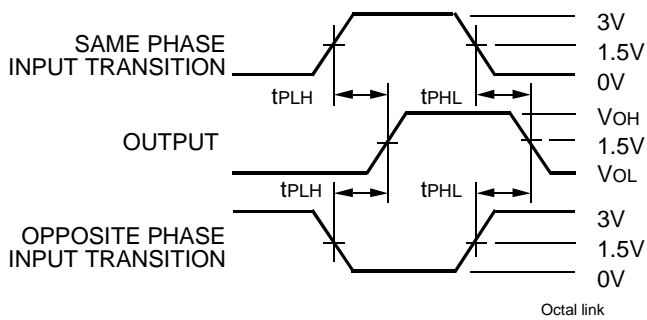
TEST CIRCUITS AND WAVEFORMS



Test Circuits for All Outputs



Set-Up, Hold, and Release Times



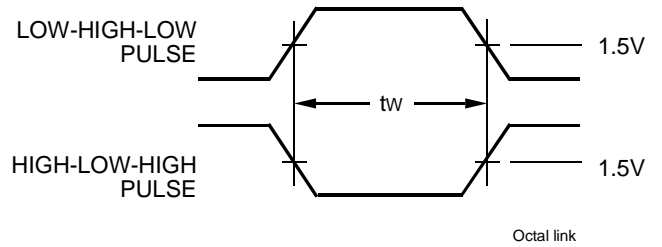
Propagation Delay

SWITCH POSITION

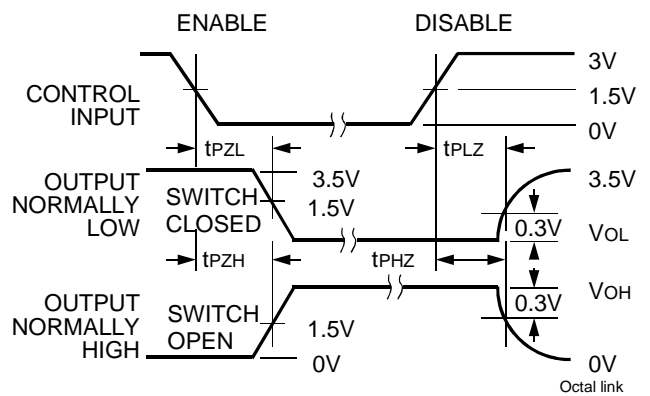
Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Tests	Open

DEFINITIONS:

CL = Load capacitance: includes jig and probe capacitance.
RT = Termination resistance: should be equal to ZOUT of the Pulse Generator.



Pulse Width

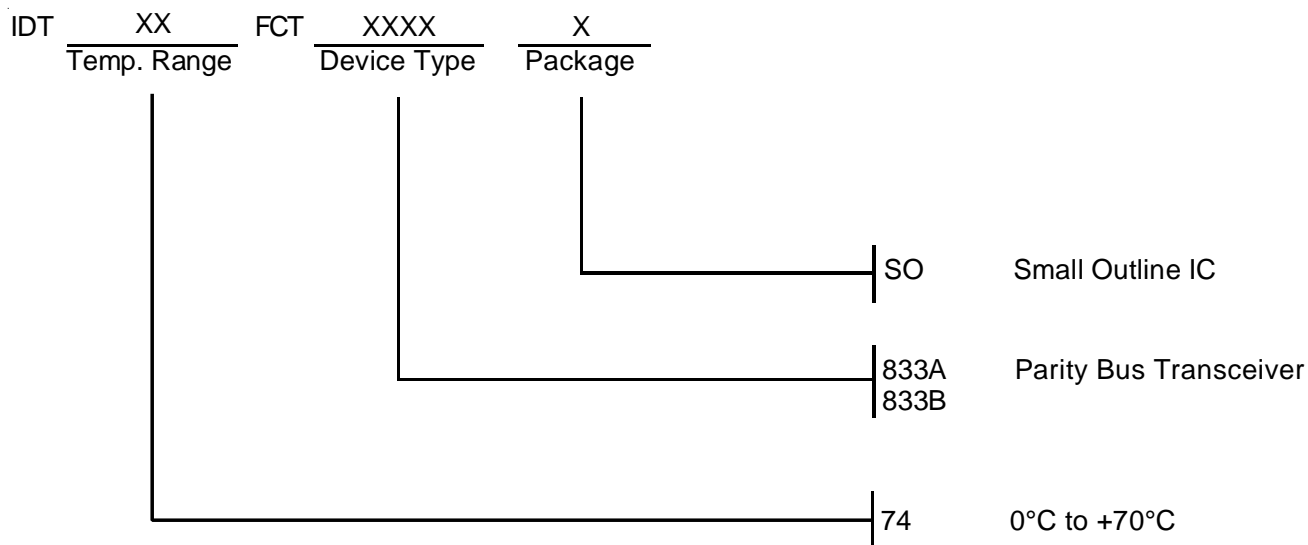


Enable and Disable Times

NOTES:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.
2. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; Zo ≤ 50Ω; tr ≤ 2.5ns; tr ≤ 2.5ns.

ORDERING INFORMATION



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