Integrated Circuit Systems, Inc.

Dual Video/Memory Clock Generator

Features

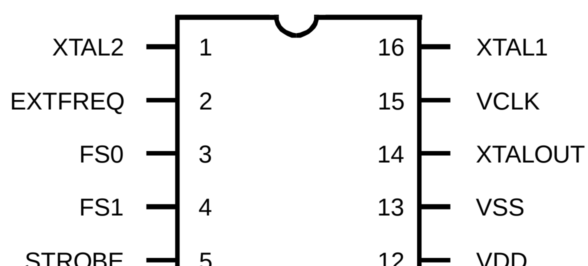
- Low cost - eliminates need for multiple crystal clock oscillators in video display subsystems
- Mask-programmable frequencies
- Pre-programmed versions for Industry Standard VGA chips
- Glitch-free frequency transitions
- Internal clock remains locked when the external frequency input is selected
- Low power CMOS device technology
- Small footprint - 16-pin DIP or SOIC
- Buffered Xtal Out
- Integral Loop Filter components
- Fast acquisition of selected frequencies, strobed or non-strobed
- Guaranteed performance up to 135 MHz
- Excellent power supply rejection
- Advanced PLL for low phase-jitter
- Frequency change detection circuitry enhances new frequency acquisition and eliminates problems caused by programs that rewrite frequency information

Description

The **ICS2495** Clock Generator is an integrated circuit dual phase-locked loop frequency synthesizer capable of generating 16 video frequencies and 4 memory clock frequencies for use with high performance video display systems. Utilizing CMOS technology to implement all linear, digital and memory functions, the **ICS2495** provides a low-power, small-footprint, low-cost solution to the generation of video dot clocks. Outputs are compatible with **XGA**, **VGA**, **EGA**, **MCGA**, **CGA**, **MDA**, as well as the higher frequencies needed for advanced applications in desktop publishing and workstation graphics. Provision is made via a single level custom mask to implement customer specific frequency sets. Phase-locked loop circuitry permits rapid glitch-free transitions between clock frequencies.

In addition to providing 16 clock rates, the **ICS2495** has provisions to multiplex an externally-generated signal source into the VCLK signal path. Internal phase-locked frequencies continue to remain locked at their preset values when this mode is selected. This feature permits instantaneous transition from an external frequency to an internally-generated frequency. Printed circuit board testing is simplified by the use of these modes as an external clock generated by the ATE tester can be fed through, permitting synchronous testing of the entire system.

Pin Configuration



16-Pin DIP or SOIC

Notes:
1. ICS2495M(SOIC) pinout is identical to ICS2495N(DIP).

Reference Oscillator & Crystal Selection

In cases where the on-chip crystal oscillator is used to generate the reference frequency, the accuracy of the crystal oscillation frequency will have a very small effect on output accuracy.

The external crystal and the on-chip circuit implement a Pierce oscillator. In a Pierce oscillator, the crystal is operated in its parallel-resonant (also called anti-resonant mode). This means that its actual frequency of oscillation depends on the effective capacitance that appears across the terminals of the quartz crystal. Use of a crystal that is characterized for use in a series-resonant circuit is fine, although the actual oscillation frequency will be slightly higher than the value stamped on the crystal can (typically 0.025%-0.05% or so). Normally, this error is not significant in video graphics applications, which is why the **ICS2495** will typically derive its frequency reference from a series resonant crystal connected between pins 1 and 16.

As the entire operation of the phase-locked loop depends on having a stable reference frequency, the crystal should be mounted as close as possible to the package. Avoid routing digital signals or the **ICS2495** outputs underneath or near these traces. It is also desirable to ground the crystal can to the ground plane, if possible.

Power Supply Conditioning

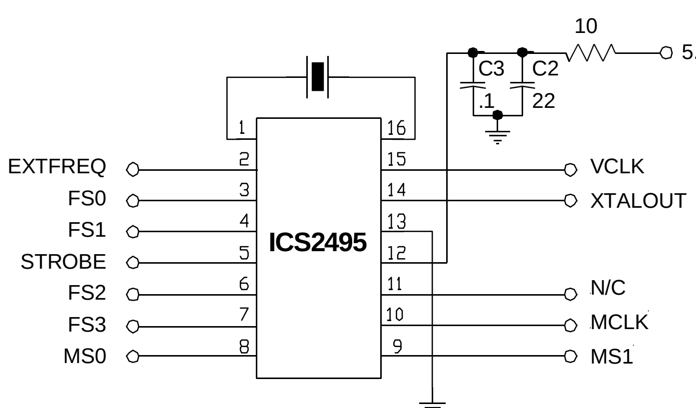
The **ICS2495** is a member of the second generation of dot clock products. By incorporating the loop filter on chip and upgrading the VCO, the ease of application has been substantially improved over earlier products. If a stable and noise-free power supply is available, no external components are required. However, in most applications it is judicious to decouple the power supply as shown in Figure 1.

Layout Considerations

Utilizing the **ICS2495** in video graphics adapter cards or on PS2 motherboards is simple, but does require precautions in board layout if satisfactory jitter-free performance is to be realized. Care should be exercised to ensure that components not related to the **ICS2495** do not share its ground. In applications utilizing a multi-layer board, V_{SS} should be directly connected to the ground plane.

Frequency Reference

The internal reference oscillator contains all of the passive components required. An appropriate crystal should be connected between **XTAL1 (16)** and **XTAL2 (1)**. In IBM compatible applications this will typically be a 14.31818 MHz crystal, but fundamental mode crystals between 10 MHz and 25 MHz have been tested. Maintain short lead lengths between the crystal and the **ICS2495**. In some applications, it may be desirable to utilize the bus clock. If the signal amplitude is equal to or greater than 3.5 volts, it may be connected directly to **XTAL1 (16)**. If the signal amplitude is less than 3.5 volts, connect the clock through a .047 microfarad capacitor to **XTAL1 (16)**, and keep the lead length of the capacitor to **XTAL1 (16)** to a minimum to reduce noise susceptibility**.** This input is internally biased at $V_{DD}/2$. Since TTL compatible clocks typically guarantee a V_{OH} of only 2.8V, capacitively coupling the input restores noise immunity. The **ICS2495** is not sensitive to the duty cycle of the bus clock; however, the quality of this signal varies considerably with different motherboard designs. As the quality of this signal is typically outside of the control of the graphics adapter card manufacturer, it is suggested that this signal be buffered on the graphics adapter board. **XTAL2 (1)** must be left open in this configuration.



NOTES: FS3-FS0, MS1-MS0, EXTFREQ, and STROBE inputs are all equipped with pull-ups and need not be tied high.
Mount decoupling capacitors as close as possible to the device and connect device ground to the ground plane where available.
Mount crystal and its circuit traces away from switching digital lines and the VCLK, MCLK and XTALOUT lines.

Figure 1

Buffered XTALOUT

In motherboard applications it may be desirable to have the **ICS2495** provide the bus clock for the rest of the system. This eliminates the need for an additional 14.31818 MHz crystal oscillator in the system, saving money as well as board space. Depending on the load, it may be judicious to buffer XTALOUT when using it to provide the system clock.

Output Circuit Considerations

As the dot clock is usually the highest frequency present in a video graphics system, consideration should be given to EMI. To minimize problems with meeting FCC EMI requirements, the trace which connects **VCLK** or **MCLK** and other components in the system should be kept as short as possible. The **ICS2495** outputs have been designed to minimize overshoot. In addition, it may be helpful to place a ferrite bead in these signal paths to limit the propagation of high-order harmonics of this signal. A suitable device would be a Ferroxcube 56-590-65/4B or equivalent. This device should be placed physically close to the **ICS2495**. A 33 to 47 Ohm series resistor, sometimes called source termination, in this path may be necessary to reduce ringing and reflection of the signal and may thereby reduce phase jitter as well as EMI.

External Frequency Sources

EXTFREQ on versions so equipped by the programming, is an input to a digital multiplexer. When this input is enabled by the FS0-3 selection, the signal driving pin 2 will appear at **VCLK (15)** instead of the PLL output. Internally, the PLL will remain in lock at the frequency selected by the ROM code.

The programming option also exists to output the crystal oscillator output on VCLK. In the case where XTAL1 is being driven by an external oscillator, then this frequency would appear on VCLK if so programmed.

Digital Inputs

FS0 (3), **FS1 (4)**, **FS2 (6)**, and **FS3 (7)**, are the TTL compatible frequency select inputs for the binary code corresponding to the frequency desired. **STROBE (5)** when high, allows new data into the frequency select latches; and when low, prevents address changes per Figure 2. The internal power-on-clear signal will force an initial frequency code corresponding to an all zeros input state. **MS0 (8)** and **MS1 (9)** are the corresponding memory select inputs and are not strobed.

Pin Descriptions

The following table provides the pin description for the 16-pin **ICS2495** packages.

PIN NUMBER	PIN SYMBOL	TYPE	DESCRIPTION
1	XTAL2	OUT	Crystal interface
2	EXTFREQ	IN	External clock input (if so programmed)
3	FS0	IN	Control input for VCLK selection
4	FS1	IN	Control input for VCLK selection
5	STROBE	IN	Strobe for latching FS (0-3) (*High enable*)
6	FS2	IN	Control input for VCLK selection
7	FS3	IN	Control input for VCLK selection
8	MS0	IN	Select input for MCLK selection
9	MS1	IN	Select input for MCLK selection
10	MCLK	OUT	Memory Clock Output
11	N/C	-	Not Connected
12	VDD	-	Power
13	VSS	-	Ground
14	XTALOUT	OUT	Buffered Crystal Output
15	VCLK	OUT	Video Clock Output
16	XTAL1	IN	Reference input clock from system

Absolute Maximum Ratings

Ambient Temperature under bias	0 °C to 70 °C
Storage temperature	-40 °C to 125 °C
Voltage on all inputs and outputs with respect to V_{SS}	0.3 to 7 Volts

Note: Stresses above those listed under Absolute Maximum Rating may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Standard Test Conditions

The characteristics below apply for the following standard test conditions, unless otherwise noted. All voltages are referenced to V_{SS} (OV Ground). Positive current flows into the referenced pin.

Operating Temperature range	0 °C to 70 °C
Power supply voltage	4.75 to 5.25 Volts

DC Characteristics at 5 Volts V_{DD}

SYMBOL	PARAMETER		MIN	MAX	UNITS	CONDITIONS
V_{DD}	Operating Voltage Range		4.75	5.25	V	
V_{IL}	Input Low Voltage		V_{SS}	0.8	V	$V_{DD} = 5V$
V_{IH}	Input High Voltage		2.0	V_{DD}	V	$V_{DD} = 5V$
I_{IH}	Input Leakage Current		-	10	µA	$V_{in} = V_{CC}$
V_{OL}	Output Low Voltage:	VCLK, MCLK	-	0.4	V	$I_{OL} = 8.0$ mA
		XTALOUT	-	0.4	V	$I_{OL} = 4.0$ mA
V_{OH}	Output High Voltage:	VCLK, MCLK	2.4	-	V	$I_{OH} = 8.0$ mA
		XTALOUT	2.4	-	V	$I_{OH} = 4.0$ mA
I_{DD}	Supply Current		-	30	mA	VDD = 5V
R_{UP}	Internal Pullup Resistors		50	-	K ohms	$V_{IN} = 0.0V$
C_{in}	Input Pin Capacitance		-	8	pF	$F_C = 1$ MHz
C_{out}	Output Pin Capacitance		-	12	pF	$F_C = 1$ MHz

AC Timing Characteristics

The following notes apply to all of the parameters presented in this section.

1. REFCLK = 14.318 MHz
2. $T_C = 1/F_C$
3. All units are in nanoseconds (ns).
4. Maximum jitter within a range of 30 µs after triggering on a 400 MHz scope.
5. Rise and fall time between 0.8 and 2.0 VDC unless otherwise stated.
6. Output pin loading = 15pF.
7. Duty cycle measured at 1.4 volts.

SYMBOL	PARAMETER	MIN	MAX	NOTES
	STROBE TIMING			
Tpw	Strobe Pulse Width	20	-	
Tsu	Setup Time Data to Strobe	10	-	
Thd	Hold Time Data to Strobe	10	-	
	MCLK and VCLK TIMINGS			
Tr	Rise Time	-	2	Duty Cycle 40% min. to
Tf	Fall Time	-	2	60% max.
-	Frequency Error		0.5	%
-	Maximum Frequency		135	MHz
-	Propagation Delay for Pass Through Frequency	-	20	ns
-	Output Enable to Tristate (into and out of) time		15	ns

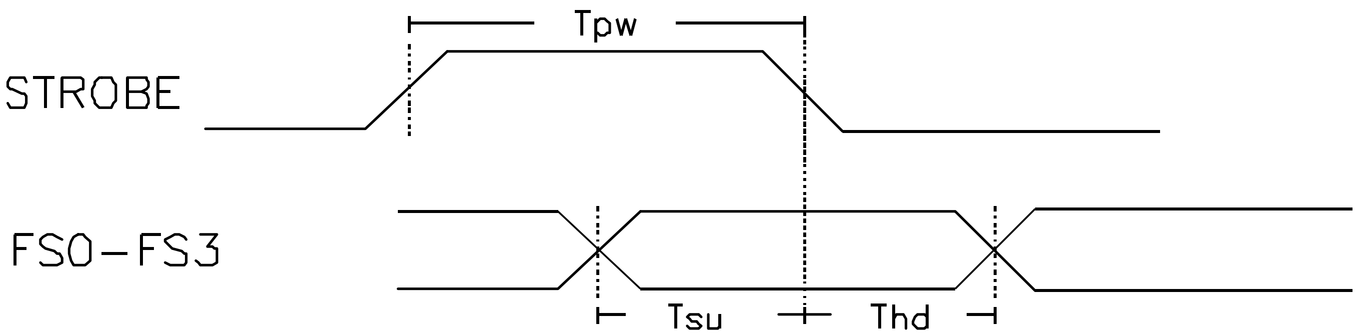


Figure 2

Ordering Information

ICS2495N-XXX or ICS2495M-XXX

Example:

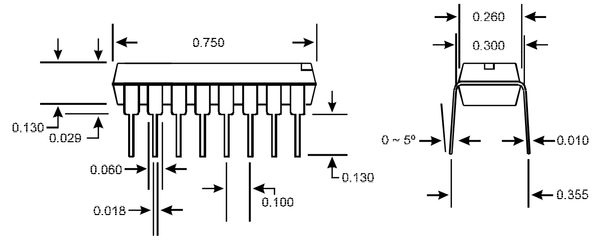
ICS XXXX M -XXX

- **Pattern Number (2 or 3 digit number for parts with ROM code patterns)**
- **Package Type**
  - N=DIP (Plastic)
  - M=SOIC
- **Device Type (consists of 3 or 4 digit numbers)**
- **Prefix**
  - ICS, AV=Standard Device; GSP=Genlock Device

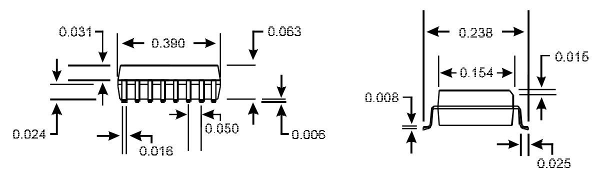
ICS2495 Pattern Request Form

ICS produces a selection of standard pattern **ICS2495**'s pre-programmed for compatibility with many popular VGA chipsets. Custom patterns are also available although a significant volume commitment and/or one-time mask charge will apply. Contact ICS Sales for details.

ICS Part Number	ICS	ICS-	ICS-
Compatible VGA Chipsets			
Video Clock Address (HEX)	Frequency (MHz)	Frequency (MHz)	Frequency (MHz)
6			
7			
8			
9			
A			
B			
C			
D			
E			
F			
Memory Clock Address (HEX)	Frequency (MHz)	Frequency (MHz)	
0			



16-Pin DIP Package



16-Pin SOIC Package

Custom pattern #1 reference frequency = __________
Standard frequencies shown have been specified by and are supported by the respective VGA manufacturer.

All standard patterns shown above use 14.31818 MHz as the input reference frequency.

If the internal frequency that the ICS2495 remains locked to when EXTFREQ is selected is critical, it should be specified.

Ordering Information

ICS2495N-XXX or ICS2495M-XXX

Example:

ICS XXXX M -XXX

Pattern Number (2 or 3 digit number for parts with ROM code patterns)
Package Type
N=DIP (Plastic)
M=SOIC
Device Type (consists of 3 or 4 digit numbers)
Prefix
ICS, AV=Standard Device; GSP=Genlock Device

Littlediode supplies new, hard to find or obsolete electronic components and semiconductors all over the world.

With over two million different components listed you are sure to find the part you need.

Feel free to visit us today at our online store:

LittleDiode.com

Looking forward to providing you with the best possible service.