



Integrated Device Technology, Inc.

# HIGH-SPEED 4K x 9 DUAL-PORT STATIC RAM

IDT7014S

## FEATURES:

- True Dual-Ported memory cells which allow simultaneous access of the same memory location
- High-speed access
  - Military: 20/25/35ns (max.)
  - Commercial: 12/15/20/25ns (max.)
- Low-power operation
  - IDT7014S  
Active: 900mW (typ.)
- Fully asynchronous operation from either port
- TTL-compatible; single 5V ( $\pm 10\%$ ) power supply
- Available in 52-pin PLCC and a 64-pin TQFP
- Industrial temperature range ( $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ ) is available, tested to military electrical specifications

## DESCRIPTION:

The IDT7014 is an extremely high-speed 4K x 9 Dual-Port Static RAM designed to be used in systems where on-chip hardware port arbitration is not needed. This part lends itself to high-speed applications which do not need on-chip arbitration to manage simultaneous access.

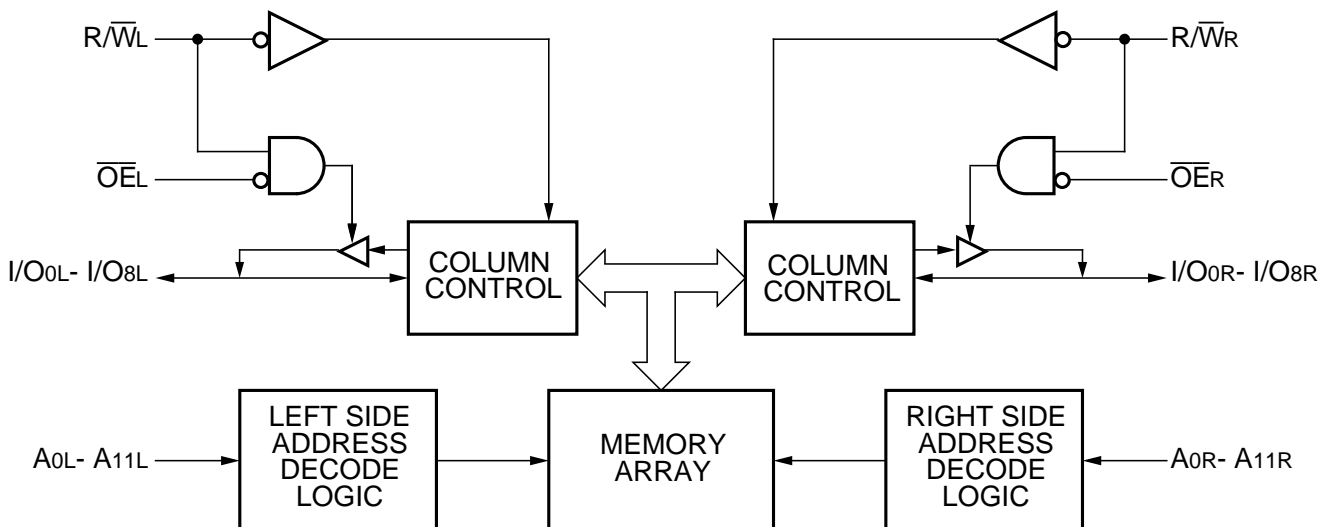
The IDT7014 provides two independent ports with separate control, address, and I/O pins that permit independent, asynchronous access for reads or writes to any location in memory. See functional description.

The IDT7014 utilizes a 9-bit wide data path to allow for parity at the user's option. This feature is especially useful in data communication applications where it is necessary to use a parity bit for transmission/reception error checking.

Fabricated using IDT's high-performance technology, the IDT7014 Dual-Ports typically operate on only 900mW of power at maximum access times as fast as 12ns.

The IDT7014 is packaged in a 52-pin PLCC and a 64-pin thin plastic quad flatpack (TQFP).

## FUNCTIONAL BLOCK DIAGRAM



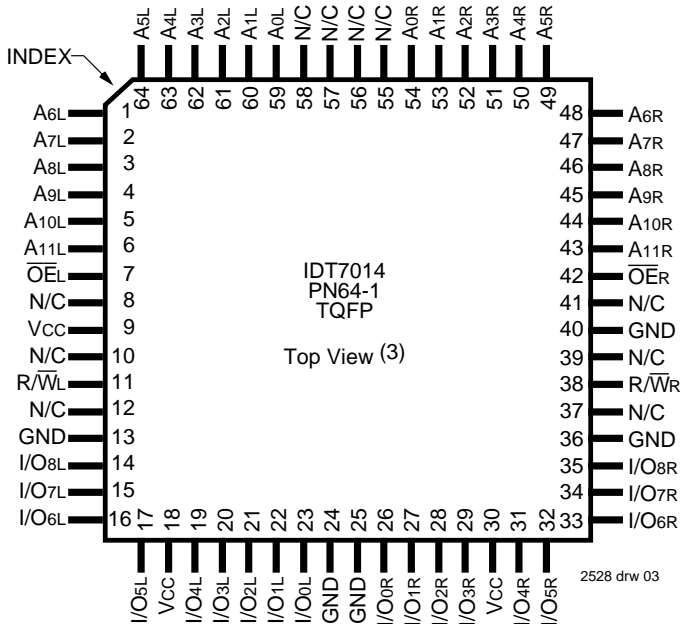
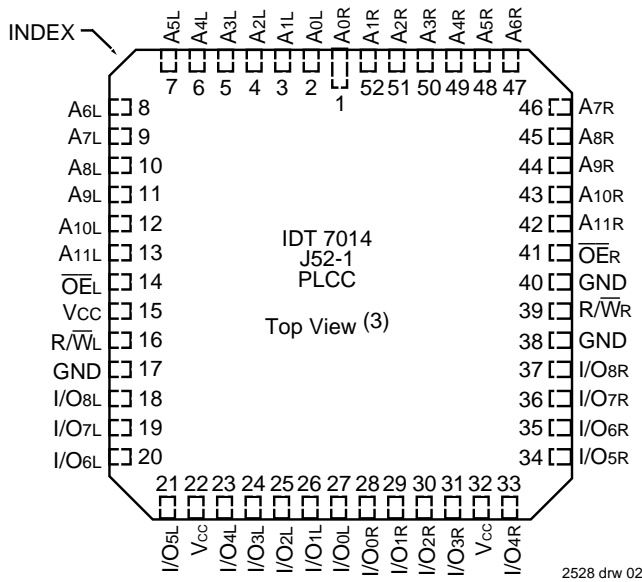
2528 drw 01

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MILITARY AND COMMERCIAL TEMPERATURE RANGES

OCTOBER 1996

**PIN CONFIGURATIONS<sup>(1,2)</sup>**



**NOTES:**

1. All Vcc pins must be connected to power supply.
2. All ground pins must be connected to ground supply.
3. This text does not indicate the orientation of the actual part-marking

**ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>**

Symbol	Rating	Commercial	Military	Unit
VTERM <sup>(2)</sup>	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
VTERM <sup>(3)</sup>	Terminal Voltage	-0.5 to Vcc	-0.5 to Vcc	V
TA	Operating Temperature	0 to +70	-55 to +125	°C
TBIAS	Temperature Under Bias	-55 to +125	-65 to +135	°C
TSTG	Storage Temperature	-55 to +125	-65 to +150	°C
IOUT	DC Output Current	50	50	mA

**NOTES:**

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. VTERM must not exceed Vcc + 0.5V for more than 25% of the cycle time or 10ns maximum, and is limited to ≤ 20mA for the period of VTERM ≥ Vcc + 0.5V.

2528 tbl 01

**RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE**

Grade	Ambient Temperature	GND	VCC
Military	-55°C to +125°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 10%

2528 tbl 02

**RECOMMENDED DC OPERATING CONDITIONS**

Symbol	Parameter	Min.	Typ.	Max.	Unit
VCC	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
VIH	Input High Voltage	2.2	—	6.0 <sup>(2)</sup>	V
VIL	Input Low Voltage	-0.5 <sup>(1)</sup>	—	0.8	V

**NOTES:**

1. VIL ≥ -1.5V for pulse width less than 10ns.
2. VTERM must not exceed Vcc + 0.5V.

2528 tbl 03

### DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE ( $V_{CC} = 5.0V \pm 10\%$ )

Symbol	Parameter	Test Condition	IDT7014S		Unit
			Min.	Max.	
I <sub>LI</sub>	Input Leakage Current	$V_{CC} = 5.5V, V_{IN} = 0V \text{ to } V_{CC}$	—	10	$\mu A$
I <sub>LO</sub>	Output Leakage Current	$V_{OUT} = 0V \text{ to } V_{CC}$	—	10	$\mu A$
V <sub>OL</sub>	Output Low Voltage	I <sub>OL</sub> = 4mA	—	0.4	V
V <sub>OH</sub>	Output High Voltage	I <sub>OH</sub> = -4mA	2.4	—	V

2528 tbl 04

### DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE ( $V_{CC} = 5V \pm 10\%$ )

Symbol	Parameter	Test Condition	Version	IDT7014S12 Com'l. Only		IDT7014S15 Com'l. Only		IDT7014S20		IDT7014S25		IDT7014S35 Mil. Only		Unit
				Typ.	Max.	Typ.	Max.	Typ.	Max.	Typ.	Max.	Typ.	Max.	
I <sub>CC</sub>	Dynamic Operating Current (Both Ports Active)	Outputs Open $f = f_{MAX}^{(1)}$	Mil.	—	—	160	260	155	260	150	255	150	250	mA
			Com'l.	160	250	160	250	155	245	150	240	—	—	

**NOTE:**

1. At  $f = f_{max}$ , address inputs are cycling at the maximum read cycle of  $1/t_{RC}$  using the "AC Test Conditions" input levels of GND to 3V.

2528 tbl 05

### AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	3ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	Figures 1, 2, and 3

2528 tbl 06

### CAPACITANCE<sup>(1)</sup>

( $T_A = +25^\circ C, f = 1.0MHz$ ) TQFP Package Only

Symbol	Parameter	Condition <sup>(2)</sup>	Max.	Unit
C <sub>IN</sub>	Input Capacitance	$V_{IN} = 3dV$	9	pF
C <sub>OUT</sub>	Output Capacitance	$V_{OUT} = 3dV$	10	pF

**NOTES:**

- This parameter is determined by device characteristics but is not tested.
- 3dv references the interperlated capacitance when the input and output signals switch from 0V to 3V or from 3V to 0V.

2528 tbl 07

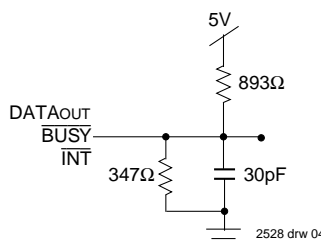


Figure 1. AC Output Test Load.

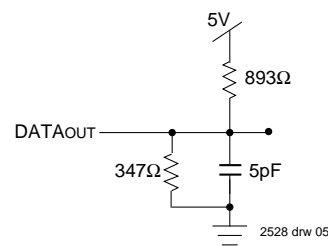


Figure 2. Output Test Load (for  $t_{HZ}$ ,  $t_{WZ}$ , and  $t_{OW}$ ) Including scope and jig.

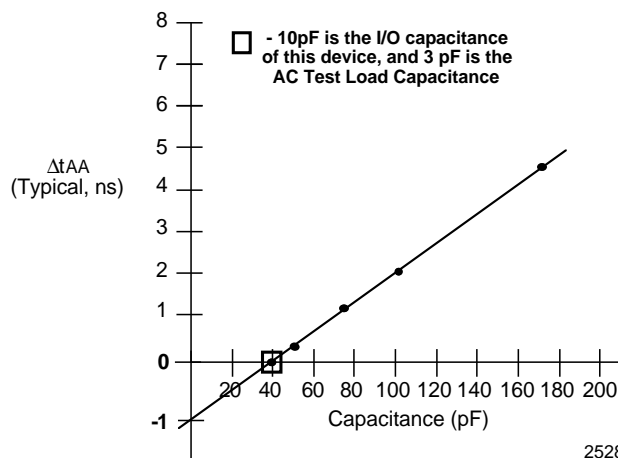


Figure 3. Typical Output Derating (Lumped Capacitive Load).

2528 drw 06

## AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE

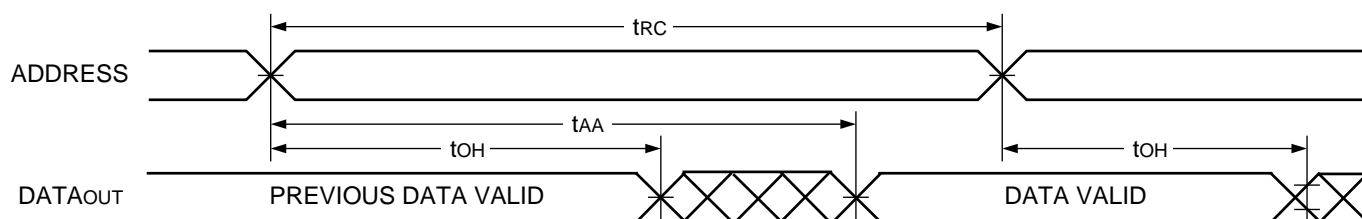
Symbol	Parameter	7014S12		7014S15		7014S20		7014S25		7014S35		Unit
		Com'l. Only		Com'l. Only						Mil. Only		
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
<b>READ CYCLE</b>												
t <sub>RC</sub>	Read Cycle Time	12	—	15	—	20	—	25	—	35	—	ns
t <sub>AA</sub>	Address Access Time	—	12	—	15	—	20	—	25	—	35	ns
t <sub>AOE</sub>	Output Enable Access Time	—	8	—	8	—	10	—	12	—	20	ns
t <sub>OH</sub>	Output Hold from Address Change	3	—	3	—	3	—	3	—	3	—	ns
t <sub>LZ</sub>	Output Low-Z Time <sup>(1, 2)</sup>	3	—	3	—	3	—	3	—	3	—	ns
t <sub>HZ</sub>	Output High-Z Time <sup>(1, 2)</sup>	—	7	—	7	—	9	—	11	—	15	ns

**NOTES:**

1. Transition is measured  $\pm 200\text{mV}$  from Low or High-impedance voltage with Output Test Load (Figure 2).
2. This parameter is determined by device characterization, but is not production tested.

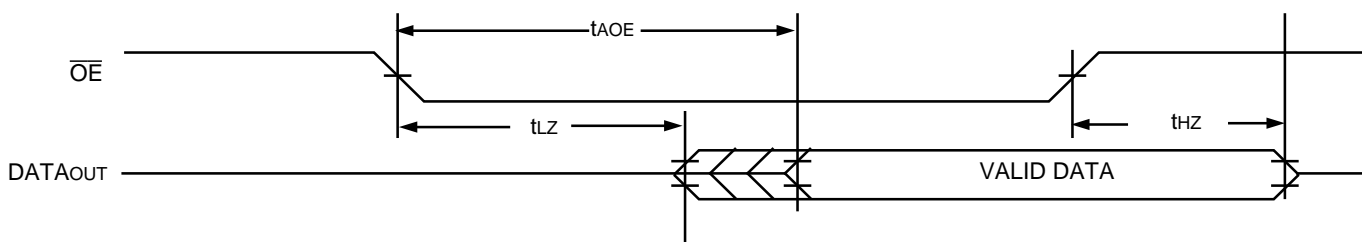
2528 tbl 08

### TIMING WAVEFORM OF READ CYCLE NO. 1, EITHER SIDE<sup>(1,2)</sup>



2528 drw 07

### TIMING WAVEFORM OF READ CYCLE NO. 2, EITHER SIDE<sup>(1, 3)</sup>



2528 drw 08

**NOTES:**

1.  $R/\bar{W} = V_{IH}$  for Read Cycles.
2.  $\bar{OE} = V_{IL}$ .
3. Addresses valid prior to  $\bar{OE}$  transition LOW.

## AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE

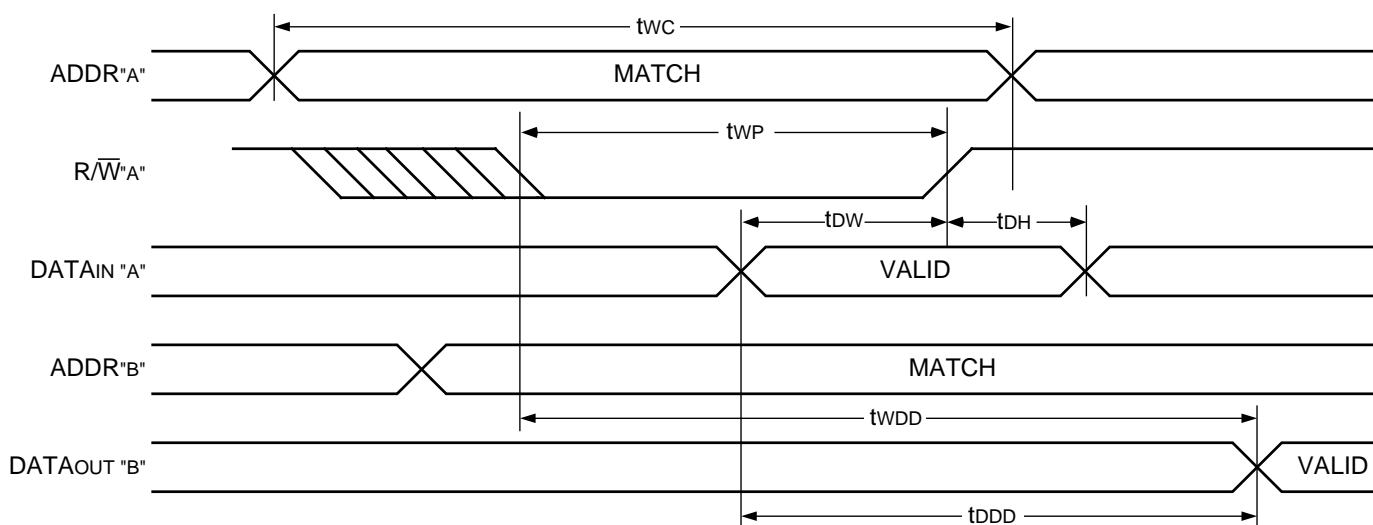
Symbol	Parameter	7014S12		7014S15		7014S20		7014S25		7014S35		Unit
		Com'l. Only		Com'l. Only						Mil. Only		
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
<b>WRITE CYCLE</b>												
tWC	Write Cycle Time	12	—	15	—	20	—	25	—	35	—	ns
tAV	Address Valid to End-of-Write	10	—	14	—	15	—	20	—	30	—	ns
tAS	Address Set-up Time	0	—	0	—	0	—	0	—	0	—	ns
tWP	Write Pulse Width	10	—	12	—	15	—	20	—	30	—	ns
tWR	Write Recovery Time	1	—	1	—	2	—	2	—	2	—	ns
tDW	Data Valid to End-of-Write	8	—	10	—	12	—	15	—	25	—	ns
tHZ	Output High-Z Time <sup>(1, 2)</sup>	—	7	—	7	—	9	—	11	—	15	ns
tDH	Data Hold Time <sup>(3)</sup>	0	—	0	—	0	—	0	—	0	—	ns
twZ	Write Enabled to Output in High-Z <sup>(1, 2)</sup>	—	7	—	7	—	9	—	11	—	15	ns
tOW	Output Active from End-of-Write <sup>(1, 2, 3)</sup>	0	—	0	—	0	—	0	—	0	—	ns
twDD	Write Pulse to Data Delay <sup>(4)</sup>	—	25	—	30	—	40	—	45	—	55	ns
tDDD	Write Data Valid to Read Data Delay <sup>(4)</sup>	—	22	—	25	—	30	—	35	—	45	ns

**NOTES:**

2528 tbl 09

1. Transition is measured ±200mV from Low or High-impedance voltage with Output Test Load (Figure 2).
2. This parameter is guaranteed by device characterization, but is not production tested.
3. The specification for t<sub>DH</sub> must be met by the device supplying write data to the RAM under all operating conditions. Although t<sub>DH</sub> and t<sub>OW</sub> values will vary over voltage and temperature, the actual t<sub>DH</sub> will always be smaller than the actual t<sub>OW</sub>.
4. Port-to-port delay through RAM cells from writing port to reading port, refer to "Timing Waveform of Write With Port-to-Port Read".

### TIMING WAVEFORM OF WRITE WITH PORT-TO-PORT READ <sup>(1,2)</sup>

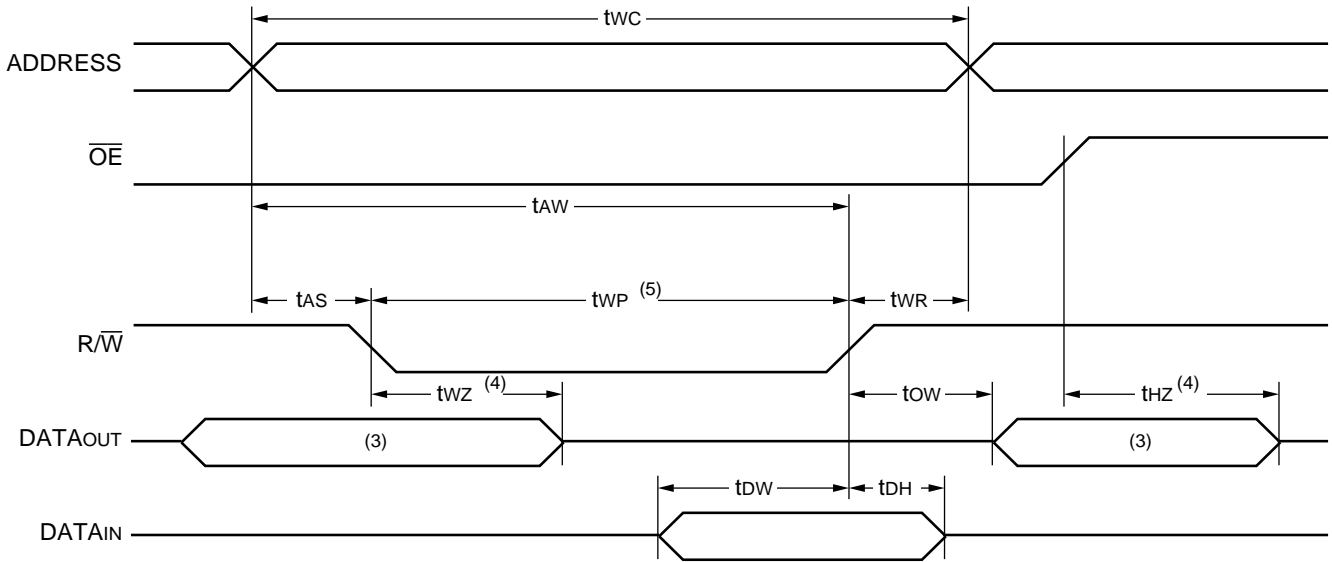


**NOTES:**

2528 drw 09

1. R/W'B' = V<sub>IH</sub>, Read cycle pass through.
2. All timing is the same for left and right ports. Port "A" may be either left or right port. Port "B" is opposite from port "A".

**TIMING WAVEFORM OF WRITE CYCLE**(1, 2, 3, 4, 5)



2528 drw 10

**NOTES:**

1.  $R/\overline{W}$  must be HIGH during all address transitions.
2.  $t_{WR}$  is measured from  $R/\overline{W}$  going HIGH to the end of write cycle.
3. During this period, the I/O pins are in the output state, and input signals must not be applied.
4. Transition is measured  $\pm 200\text{mV}$  from the Low or High-impedance voltage with the Output Test Load (Figure 2).
5. If  $\overline{OE}$  is LOW during a  $R/\overline{W}$  controlled write cycle, the write pulse width must be the larger of  $t_{WP}$  or  $(t_{WZ} + t_{DW})$  to allow the I/O drivers to turn off data to be placed on the bus for the required  $t_{OW}$ . If  $\overline{OE}$  is HIGH during a  $R/\overline{W}$  controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified  $t_{WP}$ .

**FUNCTIONAL DESCRIPTION**

The IDT7014 provides two ports with separate control, address, and I/O pins that permit independent access for reads or writes to any location in memory. It lacks the chip enable feature of most Dual-Ports, thus it operates in active mode as soon as power is applied. Each port has its own Output Enable control ( $\overline{OE}$ ). In the read mode, the port's  $\overline{OE}$  turns on the output drivers when set LOW. The user application should avoid simultaneous write operations to the same memory location. There is no on-chip arbitration circuitry to resolve write priority and partial data from both ports may be written. READ/WRITE conditions are illustrated in Table 1.

**TABLE I – READ/WRITE CONTROL**

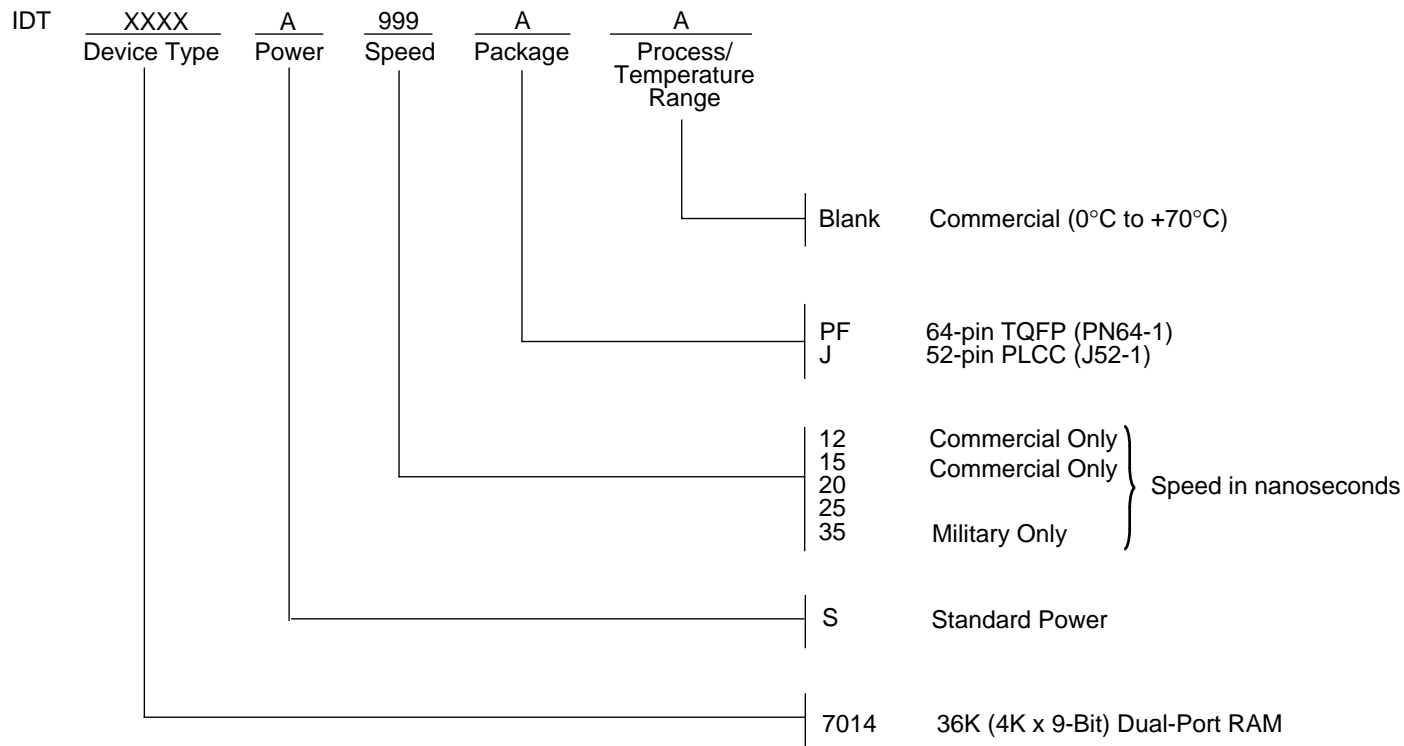
Left or Right Port <sup>(1)</sup>			Function
$R/\overline{W}$	$\overline{OE}$	D <sub>0-8</sub>	
L	X	DATA <sub>IN</sub>	Data written into memory
H	L	DATA <sub>OUT</sub>	Data in memory output on port
X	H	Z	High-impedance outputs

**NOTE:**

1. A<sub>0L</sub> - A<sub>11L</sub> is not equal to A<sub>0R</sub> - A<sub>11R</sub>.  
'H' = HIGH, 'L' = LOW, 'X' = Don't Care, and 'Z' = High-impedance.

2528 tbl 10

**ORDERING INFORMATION**



2528 drw 11

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