

HD74LS170 ●4-by-4 Register File (with open collector outputs)

The HD74LS170 is organized as 4 words of 4 bits each and separate on-chip decoding is provided for addressing the four word locations to either write-in or retrieve data. This permits simultaneous writing into one location and reading from another word location.

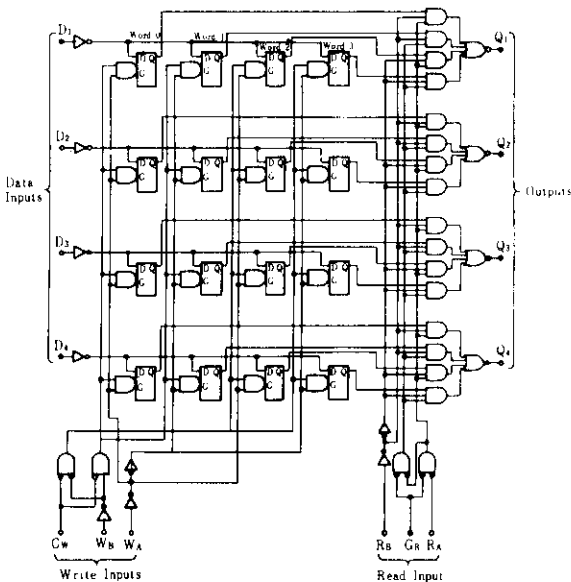
Four data inputs are available which are used to supply the 4-bit word to be stored. Location of the word is determined by the write-address inputs A and B in conjunction with a write-enable signal.

Data applied at the inputs should be in its true form. That is, if a high-level signal is desired from the output, a high level is applied at the data input for that particular bit location. The latch inputs are arranged so that new data will be accepted only if both internal address gate inputs are high. When this condition exists, data at the D input is transferred to the latch output. When the write-enable input, G_W , is high, the data inputs are inhibited and their levels can cause no change in the information stored in the internal latches.

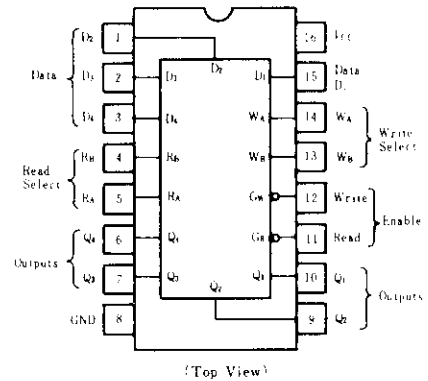
When the read-enable input, G_R , is high, the data outputs are inhibited and remain high, the individual address lines permit direct acquisition of data stored in any four of the latches. Four individual decoding gates are used to complete the address for reading a word.

When the read address is made in conjunction with the read-enable signal the word appears at the four outputs.

■BLOCK DIAGRAM



■PIN ARRANGEMENT



■FUNCTION TABLE

| Write Inputs | | | Word | | | |
|--------------|-------|-------|-------------|-------------|-------------|-------------|
| W_R | W_A | G_W | 0 | 1 | 2 | 3 |
| L | L | L | $Q_0 = D_0$ | $Q_1 = D_1$ | $Q_2 = D_2$ | $Q_3 = D_3$ |
| L | H | L | $Q_0 = D_0$ | $Q_1 = D_1$ | $Q_2 = D_2$ | $Q_3 = D_3$ |
| H | L | L | $Q_0 = D_0$ | $Q_1 = D_1$ | $Q_2 = D_2$ | $Q_3 = D_3$ |
| H | H | L | $Q_0 = D_0$ | $Q_1 = D_1$ | $Q_2 = D_2$ | $Q_3 = D_3$ |
| X | X | H | $Q_0 = Q_0$ | $Q_1 = Q_1$ | $Q_2 = Q_2$ | $Q_3 = Q_3$ |

| Read Inputs | | | Outputs | | | |
|-------------|-------|-------|-----------|-----------|-----------|-----------|
| W_R | W_A | G_W | 0 | 1 | 2 | 3 |
| L | L | L | $W_0 B_1$ | $W_1 B_2$ | $W_2 B_3$ | $W_3 B_4$ |
| L | H | L | $W_1 B_1$ | $W_1 B_2$ | $W_1 B_3$ | $W_1 B_4$ |
| H | L | L | $W_2 B_1$ | $W_2 B_2$ | $W_2 B_3$ | $W_2 B_4$ |
| H | H | L | $W_3 B_1$ | $W_3 B_2$ | $W_3 B_3$ | $W_3 B_4$ |
| X | X | H | H | H | H | H |

- Notes: H = high level, L = low level, X = irrelevant.
 (Q=D) = The four selected internal flip-flop outputs will assume the states applied to the four external data inputs.
 Q_0 = The level of Q before the indicated input conditions were established.
 $W_0 B_1$ = The first bit of word 0, etc.

RECOMMENDED OPERATING CONDITIONS

| Item | | Symbol | min | typ | max | Unit |
|----------------|--------------|-------------|------|-----|------|------|
| Supply Voltage | | V_{CC} | 4.75 | 5 | 5.25 | V |
| Output Voltage | | V_{OH} | — | — | 5.5 | V |
| Output Current | | I_{OL} | — | — | 8 | mA |
| Pulse width | Read enable | t_w | 25 | — | — | ns |
| | Write enable | | 60 | — | — | |
| Setup Time | Data input | t_{su} | 10 | — | — | ns |
| | Write select | | 15 | — | — | |
| Hold Time | Data input | t_h | 15 | — | — | ns |
| | Write select | | 5 | — | — | |
| Latch time | | t_{latch} | 60 | — | — | ns |

ELECTRICAL CHARACTERISTICS ($T_a = -20 \sim +75^\circ\text{C}$)

| Item | | Symbol | Test Condition | min | typ* | max | Unit |
|---------------------------------|---------------------------------|--------------------------------------|---|---------------------|------|------|---------------|
| Input Voltage | | V_{IH} | | 2.0 | — | — | V |
| | | V_{IL} | | — | — | 0.8 | V |
| Output Current | | I_{OH} | $V_{CC}=4.75\text{V}, V_{OH}=5.5\text{V}, V_{IL}=0.8\text{V}, V_{IH}=2\text{V}$ | — | — | 100 | μA |
| Output Voltage | | V_{OL} | $V_{CC}=4.75\text{V}, V_{IH}=2\text{V}, V_{IL}=0.8\text{V}$ | $I_{OL}=4\text{mA}$ | — | 0.4 | V |
| | | | | $I_{OL}=8\text{mA}$ | — | 0.5 | |
| Input Current | Any D, R or W G_R or G_W | I_{IH} | $V_{CC}=5.25\text{V}, V_I=2.7\text{V}$ | — | — | 20 | μA |
| | — | | | — | 40 | | |
| | Any D, R or W G_R or G_W | I_{IL} | $V_{CC}=5.25\text{V}, V_I=0.4\text{V}$ | — | — | -0.4 | mA |
| | — | | | — | -0.8 | | |
| Any D, R or W G_R or G_W | I_i | $V_{CC}=5.25\text{V}, V_I=7\text{V}$ | — | — | 0.1 | mA | |
| | | | — | — | 0.2 | | |
| Supply Current | | I_{CC}^{**} | $V_{CC}=5.25\text{V}$ | — | 25 | 40 | mA |
| Input clamp voltage | | V_{IK} | $V_{CC}=4.75\text{V}, I_{IH}=-18\text{mA}$ | — | — | -1.5 | V |

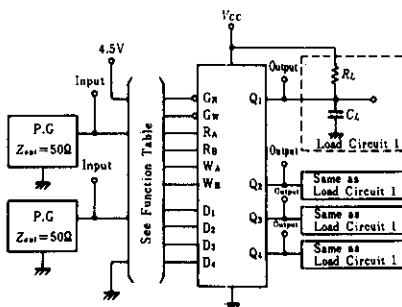
* $V_{CC}=5\text{V}, T_a=25^\circ\text{C}$

** : Typical I_{CC} shown is an average for 50% duty cycle. Maximum I_{CC} is guaranteed for the following worst case conditions: 4.5V is applied to all data inputs and both enable inputs, all address inputs are grounded, and all outputs are open.

SWITCHING CHARACTERISTICS ($V_{CC}=5\text{V}, T_a=25^\circ\text{C}$)

| Item | Symbol | Inputs | Outputs | Test Conditions | min | typ | max | Unit | |
|------------------------|-----------|--------------|----------------|--|-----|-----|-----|------|----|
| Propagation Delay Time | t_{PLH} | Read enable | $Q_1 \sim Q_4$ | $C_L=15\text{pF}$ $R_L=2\text{k}\Omega$ | — | 20 | 30 | ns | |
| | t_{PHL} | Read select | $Q_1 \sim Q_4$ | | — | 20 | 30 | | |
| | t_{PLH} | Write enable | $Q_1 \sim Q_4$ | | — | 25 | 40 | | |
| | t_{PHL} | Write enable | $Q_1 \sim Q_4$ | | — | 24 | 40 | | |
| | t_{PLH} | Data | $Q_1 \sim Q_4$ | | — | 30 | 45 | | |
| | t_{PHL} | Data | $Q_1 \sim Q_4$ | | — | 30 | 45 | | |
| | t_{PLH} | Data | $Q_1 \sim Q_4$ | | — | — | 26 | | 40 |
| | t_{PHL} | Data | $Q_1 \sim Q_4$ | | — | — | 22 | | 30 |

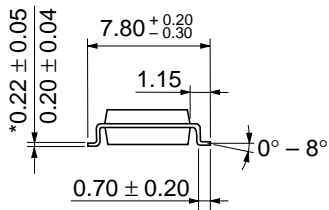
TESTING METHOD



- Notes: 1. C_L includes probe and jig capacitance.
2. All diodes are 1S2074 (Ⓢ).

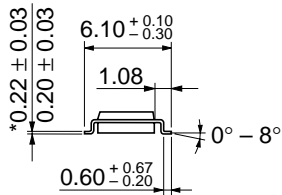


| | |
|--------------------------|----------|
| Hitachi Code | DP-16 |
| JEDEC | Conforms |
| EIAJ | Conforms |
| Weight (reference value) | 1.07 g |



*Dimension including the plating thickness
Base material dimension

| | |
|--------------------------|----------|
| Hitachi Code | FP-16DA |
| JEDEC | — |
| EIAJ | Conforms |
| Weight (reference value) | 0.24 g |



*Dimension including the plating thickness
Base material dimension

| | |
|--------------------------|----------|
| Hitachi Code | FP-16DN |
| JEDEC | Conforms |
| EIAJ | Conforms |
| Weight (reference value) | 0.15 g |

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