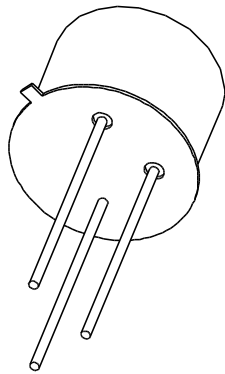


DATA SHEET



BFX30

PNP switching transistor

Product specification
Supersedes data of September 1994
File under Discrete Semiconductors, SC04

1997 Apr 16

PNP switching transistor

BFX30

FEATURES

- High current (max.600 mA)
- Low voltage (max. 65 V).

APPLICATIONS

- Switching applications.

DESCRIPTION

PNP transistor in a TO-39 metal package.

PINNING

PIN	DESCRIPTION
1	emitter
2	base
3	collector, connected to case

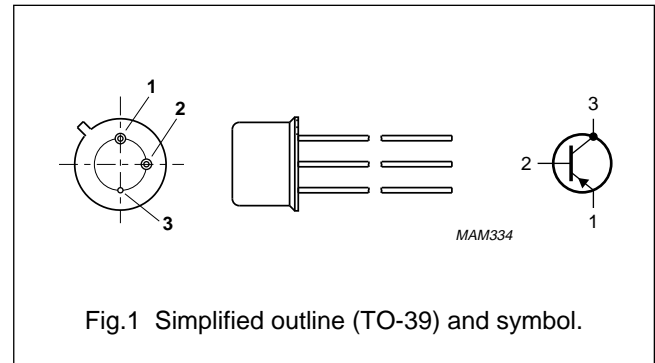


Fig.1 Simplified outline (TO-39) and symbol.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CBO}	collector-base voltage	open emitter	–	–	–65	V
V_{CEO}	collector-emitter voltage	open base	–	–	–65	V
I_C	collector current (DC)		–	–	–600	mA
P_{tot}	total power dissipation	$T_{amb} \leq 25\text{ }^\circ\text{C}$	–	–	600	mW
h_{FE}	DC current gain	$I_C = -10\text{ mA}; V_{CE} = -400\text{ mV}$	50	90	200	
f_T	transition frequency	$I_C = -50\text{ mA}; V_{CE} = -10\text{ V}; f = 100\text{ MHz}$	100	–	–	MHz
t_{off}	turn-off time	$I_{Con} = -150\text{ mA}; I_{Bon} = -15\text{ mA}; I_{Boff} = 10\text{ mA}$	–	–	300	ns

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LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V _{CBO}	collector-base voltage	open emitter	–	–65	V
V _{CEO}	collector-emitter voltage	open base	–	–65	V
V _{EBO}	emitter-base voltage	open collector	–	–5	V
I _C	collector current (DC)		–	–600	mA
I _{CM}	peak collector current		–	–600	mA
I _{BM}	peak base current		–	–200	mA
P _{tot}	total power dissipation	T _{amb} ≤ 25 °C	–	600	mW
T _{stg}	storage temperature		–65	+150	°C
T _j	junction temperature		–	200	°C
T _{amb}	operating ambient temperature		–65	+150	°C

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
R _{th j-a}	thermal resistance from junction to ambient	in free air	300	K/W

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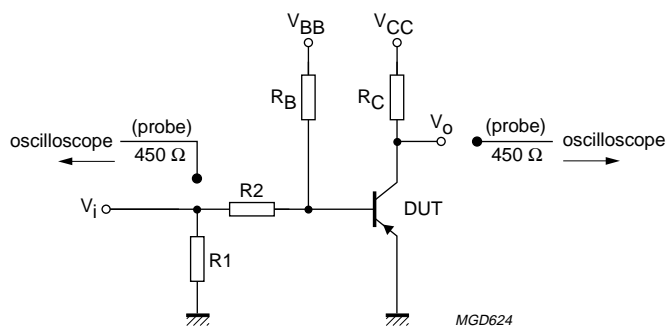
CHARACTERISTICS

$T_j = 25\text{ }^\circ\text{C}$ unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{CBO}	collector cut-off current	$I_E = 0; V_{CB} = -65\text{ V}$	-	-	-500	nA
		$I_E = 0; V_{CB} = -50\text{ V}$	-	-	-50	nA
		$I_E = 0; V_{CB} = -50\text{ V}; T_j = 100\text{ }^\circ\text{C}$	-	-	-2	μA
I_{EBO}	emitter cut-off current	$I_C = 0; V_{EB} = -5\text{ V}$	-	-	-500	nA
		$I_C = 0; V_{EB} = -3\text{ V}$	-	-	-100	nA
h_{FE}	DC current gain	$I_C = -1\text{ mA}; V_{CE} = -400\text{ mV}$	40	-	-	
		$I_C = -10\text{ mA}; V_{CE} = -400\text{ mV}$	50	90	200	
		$I_C = -50\text{ mA}; V_{CE} = -400\text{ mV}$	20	-	-	
		$I_C = -150\text{ mA}; V_{CE} = -400\text{ mV}$	10	-	-	
V_{CEsat}	collector-emitter saturation voltage	$I_C = -150\text{ mA}; I_B = -15\text{ }\mu\text{A}$	-	-	-400	mV
V_{BEsat}	base-emitter saturation voltage	$I_C = -30\text{ mA}; I_B = -1\text{ mA}$	-	-	-900	mV
		$I_C = -150\text{ mA}; I_B = -15\text{ mA}$	-	-	-1.3	V
C_c	collector capacitance	$I_E = i_e = 0; V_{CB} = -10\text{ V}; f = 1\text{ MHz}$	-	6	-	pF
C_e	emitter capacitance	$I_C = i_c = 0; V_{EB} = -2\text{ V}; f = 1\text{ MHz}$	-	18	-	pF
f_T	transition frequency	$I_C = -50\text{ mA}; V_{CE} = -10\text{ V}; f = 100\text{ MHz}$	100	-	-	MHz

Switching Times (between 10% and 90% levels); see Fig.2

t_{on}	turn-on time	$I_{Con} = -150\text{ mA}; I_{Bon} = -15\text{ mA};$ $I_{Boff} = 15\text{ mA}$	-	-	45	ns
t_d	delay time		-	-	15	ns
t_r	rise time		-	-	35	ns
t_{off}	turn-off time		-	-	300	ns
t_s	storage time		-	-	250	ns
t_f	fall time		-	-	50	ns



$V_{CC} = -29.5\text{ V}; V_{BB} = 3.5\text{ V}; V_i = -9.5\text{ V};$
 $T = 500\text{ }\mu\text{s}; t_p = 10\text{ }\mu\text{s}; t_r = t_f \leq 3\text{ ns.}$
 $R_1 = 68\text{ }\Omega; R_2 = 325\text{ }\Omega; R_B = 325\text{ }\Omega; R_C = 160\text{ }\Omega.$
 Oscilloscope: input impedance $Z_i = 50\text{ }\Omega.$

Fig.2 Test circuit for switching times.

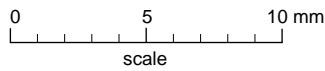
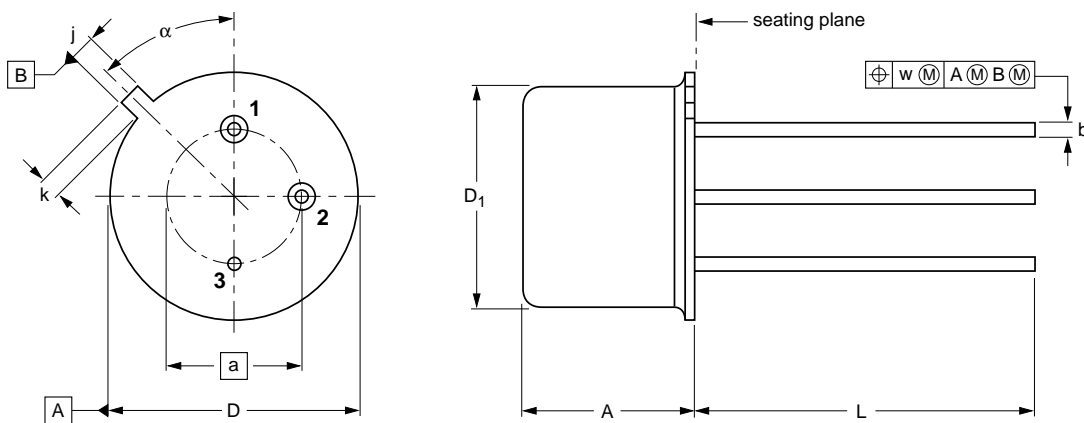
PNP switching transistor

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PACKAGE OUTLINE

Metal-can cylindrical single-ended package; 3 leads

SOT5/11



DIMENSIONS (mm are the original dimensions)

UNIT	A	a	b	D	D ₁	j	k	L	w	α
mm	6.60 6.35	5.08	0.48 0.41	9.39 9.08	8.33 8.18	0.85 0.75	0.95 0.75	14.2 12.7	0.2	45°

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT5/11		TO-39				97-04-11

PNP switching transistor

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DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

LIFE SUPPORT APPLICATIONS

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PNP switching transistor

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