

## DM54L95 4-Bit Parallel Access Shift Registers

### General Description

These 4-bit registers feature parallel and serial inputs, parallel output, mode control, and two clock inputs. The registers have three modes of operation.

- Parallel (broadside) load
- Shift right (the direction  $Q_A$  toward  $Q_D$ )
- Shift left (the direction  $Q_D$  toward  $Q_A$ )

Parallel loading is accomplished by applying the four bits of data and taking the mode control input high. The data is loaded into the associated flip-flops and appears at the outputs after the high-to-low transition of the clock-2 input. During loading, the entry of serial data is inhibited.

Shift right is accomplished on the high-to-low transition of clock 1 when the mode control is low; shift left is accomplished on the high-to-low transition of clock 2 when the

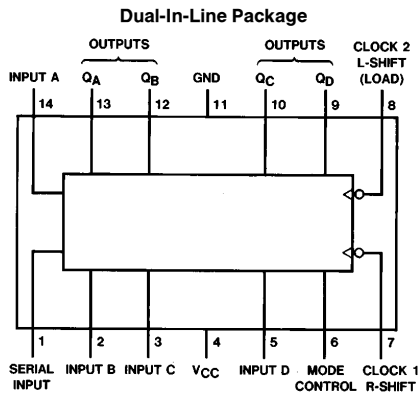
mode control is high by connecting the output of each flip-flop to the parallel input of the previous flip-flop ( $Q_D$  to input C, etc.) and serial data is entered at input D. The clock input may be applied simultaneously to clock 1 and clock 2 if both modes can be clocked from the same source.

Changes at the mode control input should normally be made while both clock inputs are low; however, conditions described in the last three lines of the truth table will also ensure that register contents are protected.

### Features

- Typical maximum clock frequency 14 MHz
- Typical power dissipation mW

### Connection Diagram



Order Number DM54L95J  
or DM54L95W  
See NS Package Number  
J14A or W14B

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### Function Table

Mode Control	Inputs							Outputs			
	Clocks		Serial	Parallel				$Q_A$	$Q_B$	$Q_C$	$Q_D$
	2 (L)	1 (R)		A	B	C	D				
H	H	X	X	X	X	X	X	$Q_{AO}$	$Q_{BO}$	$Q_{CO}$	$Q_{DO}$
H	↓	X	X	a	b	c	d	a	b	c	d
H	↓	X	X	$Q_B^\dagger$	$Q_C^\dagger$	$Q_D^\dagger$	d	$Q_{Bn}$	$Q_{Cn}$	$Q_{Dn}$	d
L	L	H	X	X	X	X	X	$Q_{AO}$	$Q_{BO}$	$Q_{CO}$	$Q_{DO}$
L	X	↓	H	X	X	X	X	H	$Q_{An}$	$Q_{Bn}$	$Q_{Cn}$
L	X	↓	L	X	X	X	X	L	$Q_{An}$	$Q_{Bn}$	$Q_{Cn}$
↑	L	L	X	X	X	X	X	$Q_{AO}$	$Q_{Bn}$	$Q_{CO}$	$Q_{DO}$
↓	L	L	X	X	X	X	X	$Q_{AO}$	$Q_{BO}$	$Q_{CO}$	$Q_{DO}$
↓	L	H	X	X	X	X	X	$Q_{AO}$	$Q_{BO}$	$Q_{CO}$	$Q_{DO}$
↑	H	L	X	X	X	X	X	$Q_{AO}$	$Q_{BO}$	$Q_{CO}$	$Q_{DO}$
↑	H	H	X	X	X	X	X	$Q_{AO}$	$Q_{BO}$	$Q_{CO}$	$Q_{DO}$

† Shifting left requires external connection of  $Q_B$  to A,  $Q_C$  to B,  $Q_D$  to C. Serial data is entered at input D.  
H = High Level (Steady State), L = Low Level (Steady State), X = Don't Care (Any input, including transitions).  
↓ = Transition from high to low level. ↑ = Transition from low to high level.  
a, b, c, d, = The level of steady state input at inputs A, B, C, or D, respectively.  
 $Q_{AO}$ ,  $Q_{BO}$ ,  $Q_{CO}$ ,  $Q_{DO}$  = The level of  $Q_A$ ,  $Q_B$ ,  $Q_C$ , or  $Q_D$ , respectively, before the indicated steady state input conditions were established.  
 $Q_{An}$ ,  $Q_{Bn}$ ,  $Q_{Cn}$ ,  $Q_{Dn}$  = The level of  $Q_A$ ,  $Q_B$ ,  $Q_C$ , or  $Q_D$ , respectively, before the most recent ↓ transition of the clock.

## Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	8V
Input Voltage	5.5V
Operating Free Air Temperature Range	
DM54L	–55°C to +125°C
Storage Temperature Range	–65°C to +150°C

Note: The “Absolute Maximum Ratings” are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the “Electrical Characteristics” table are not guaranteed at the absolute maximum ratings. The “Recommended Operating Conditions” table will define the conditions for actual device operation.

## Recommended Operating Conditions

Symbol	Parameter		DM54L95			Units
			Min	Nom	Max	
V <sub>CC</sub>	Supply Voltage		4.5	5	5.5	V
V <sub>IH</sub>	High Level Input Voltage		2			V
V <sub>IL</sub>	Low Level Input Voltage				0.7	V
I <sub>OH</sub>	High Level Output Current				–0.2	mA
I <sub>OL</sub>	Low Level Output Current				2	mA
f <sub>CLK</sub>	Clock Frequency (Note 1)		0		6	MHz
t <sub>W(CLK)</sub>	Pulse Width of Clock (Note 1)		90			ns
t <sub>SU</sub>	Data Setup Time (Note 1)		50			ns
t <sub>EN</sub>	Time to Enable Clock (Note 1)	Clock 1	120			ns
		Clock 2	100			ns
t <sub>H</sub>	Data Hold Time (Note 1)		0			ns
t <sub>IN</sub>	Time to Inhibit Clock 1 or Clock 2 (Note 1)		0			ns
T <sub>A</sub>	Free Air Operating Temperature		–55		125	°C

Note 1: T<sub>A</sub> = 25°C and V<sub>CC</sub> = 5V.

## Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 1)	Max	Units
V <sub>OH</sub>	High Level Output Voltage	V <sub>CC</sub> = Min, I <sub>OH</sub> = Max V <sub>IL</sub> = Max, V <sub>IH</sub> = Min	2.4	3.1		V
V <sub>OL</sub>	Low Level Output Voltage	V <sub>CC</sub> = Min, I <sub>OL</sub> = Max V <sub>IL</sub> = Max, V <sub>IH</sub> = Min		0.13	0.3	V
I <sub>I</sub>	Input Current @ Max Input Voltage	V <sub>CC</sub> = Max V <sub>I</sub> = 5.5V	Mode		0.2	mA
			Others		0.1	
I <sub>IH</sub>	High Level Input Current	V <sub>CC</sub> = Max V <sub>I</sub> = 2.4V	Mode		20	μA
			Others		10	
I <sub>IL</sub>	Low Level Input Current	V <sub>CC</sub> = Max V <sub>I</sub> = 0.3V	Mode		–0.36	mA
			Others		–0.18	
I <sub>OS</sub>	Short Circuit Output Current	V <sub>CC</sub> = Max (Note 2)	–3		–15	mA
I <sub>CC</sub>	Supply Current	V <sub>CC</sub> = Max (Note 3)		4.8	8	mA

Note 1: All typicals are at V<sub>CC</sub> = 5V, T<sub>A</sub> 25°C

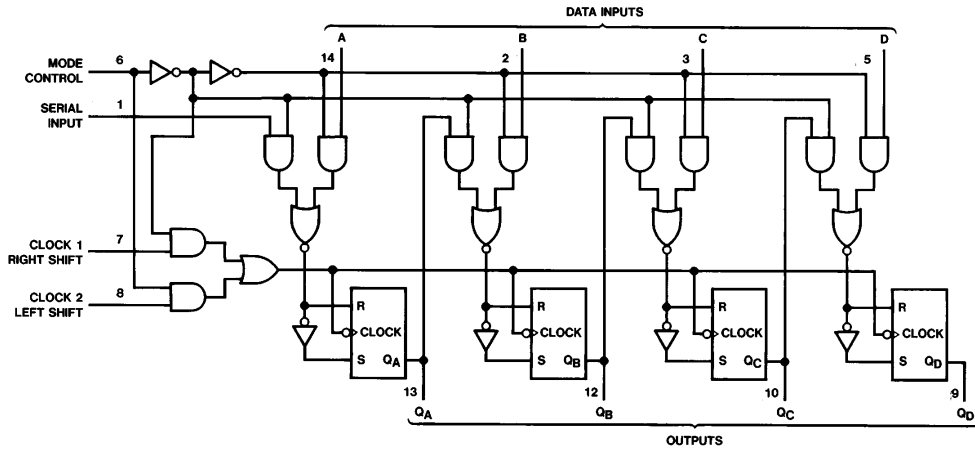
Note 2: Not more than one output should be shorted at a time.

Note 3: I<sub>CC</sub> is measured with all outputs and serial input open; A, B, C, and D inputs grounded; mode control at 4.5V; and a momentary 3V, then ground, applied to both clock inputs.

**Switching Characteristics** at  $V_{CC} = 5V$  and  $T_A 25^\circ C$  (See Section 1 for Test Waveforms and Output Load)

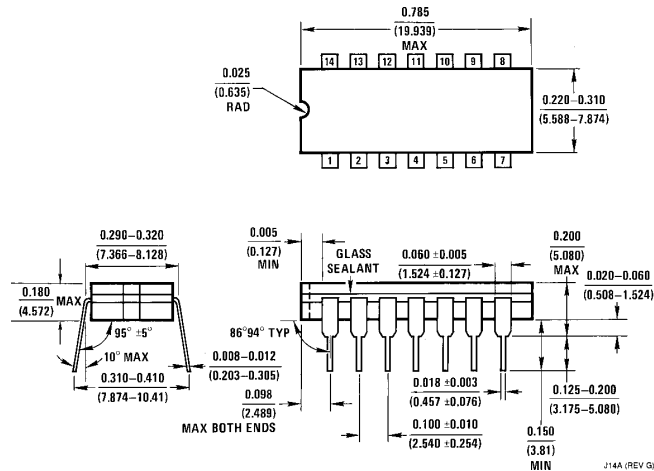
Symbol	Parameter	From (Input) To (Output)	$R_L = 4\Omega, C_L = 50\text{ pF}$		Units
			Min	Max	
$f_{MAX}$	Maximum Clock Frequency		6		MHz
$t_{PLH}$	Propagation Delay Time Low to High Level Output	Clock to Output		90	ns
$t_{PHL}$	Propagation Delay Time High to Low Level Output	Clock to Output		90	ns

**Logic Diagram**



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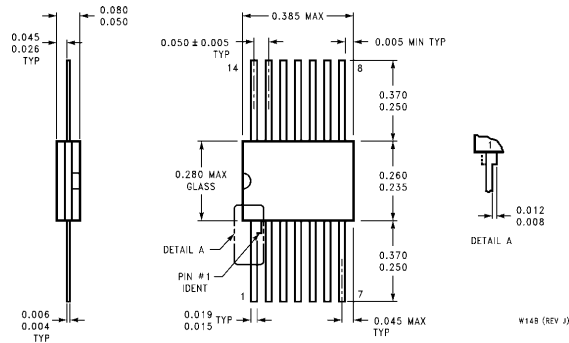
**Physical Dimensions** inches (millimeters)



**14-Lead Ceramic Dual-In-Line Package (J)**  
**Order Number DM54L95J**  
**NS Package Number J14A**

J14A (REV G)

**Physical Dimensions** inches (millimeters) (Continued)



**14-Lead Ceramic Flat Package (W)**  
**Order Number DM54L95W**  
**NS Package Number W14B**

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