

# HD74LS166A ●8-bit Shift Registers

The inputs are buffered to lower the drive requirements to one series 74 or 74LS standard load, respectively. Input clamping diodes minimize switching transients and simplify system design. This parallel-in or serial-in, serial-out shift register has a complexity of 77 equivalent gates on a monolithic chip. This device features gated clock inputs and an overriding clear input.

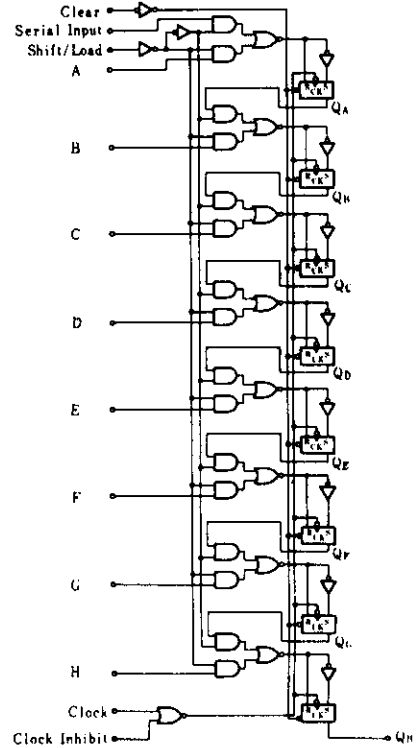
The parallel-in or serial-in modes are established by the shift/load input.

When high, this input enables the serial data input and couples the eight flip-flops for serial shifting with each clock pulse. When low, the parallel (broadside) data inputs are enabled and synchronous loading occurs on the next clock pulse. During parallel loading, serial data flow is inhibited.

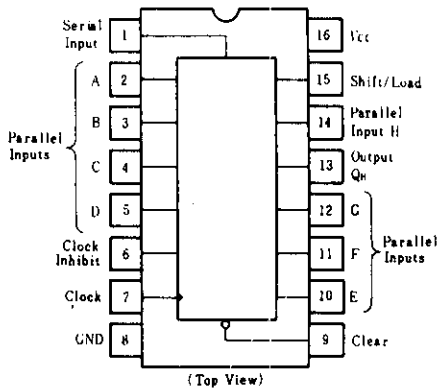
Clocking is accomplished on the low-to-high-level edge of the clock pulse through a two-input positive NOR gate permitting one input to be used as a clock-enable or clock-inhibit function. Holding either of the clock inputs high inhibits clocking; holding either low enables the other clock input.

This, of course, allows the system clock to be free-running and the register can be stopped on command with the other clock input. The clock-inhibit input should be changed to the high level only while the clock input is high. A buffered, direct clear input overrides all other inputs, including the clock, and sets all flip-flops to zero.

## ■ BLOCK DIAGRAM



## ■ PIN ARRANGEMENT



## ■ FUNCTION TABLE

Inputs							Internal Outputs		Outputs
Clear	Shift Load	Clock Inhibit	Clock	Serial	Parallel A...H	QA	QH	QH	
L	X	X	X	X	X	L	L	L	
H	X	L	L	X	X	QA(i)	QH(i)	QH(i)	
H	L	L	↑	X	a...h	a	b	h	
H	H	L	↑	H	X	H	QA,n	QH,n	
H	H	L	↑	L	X	L	QA,n	QH,n	
H	X	H	↑	X	X	QA(i)	QH(i)	QH(i)	

- Notes) 1. H; high level, L; low level, X; irrelevant  
 2. ↑; transition from low to high level  
 3. ↓; transition from high to low level  
 4. a~h; the level of steady-state input at inputs A to H respectively  
 5. QA0~QH0; the level of QA to QH, respectively, before the indicated steady-state input conditions were established.  
 6. QA,n~QH,n; the level of QA to QH, respectively, before the most recent ↓ transition of the clock.

## ■ RECOMMENDED OPERATING CONDITIONS

Item	Symbol	min	nom	max	Unit
High level output current	$I_{OH}$	—	—	-400	$\mu A$
Low level output current	$I_{OL}$	—	—	8	mA
Clock frequency	$f_{clock}$	0	—	25	MHz
Clock and clear pulse width	$t_w$	20	—	—	ns
Mode control setup time	$t_{su}$	30	—	—	ns
Data setup time	$t_{su}$	20	—	—	ns
Hold time	$t_h$	0	—	—	ns

# HD74LS166A

## ■ ELECTRICAL CHARACTERISTICS ( $T_a = -20 \sim +75^\circ\text{C}$ )

Item	Symbol	Test Conditions	min	typ*	max	Unit
Input voltage	$V_{IH}$		2.0	---	---	V
	$V_{IL}$		---	---	0.8	V
Output voltage	$V_{OH}$	$V_{CC} = 4.75\text{V}$ , $V_{IH} = 2\text{V}$ , $V_{IL} = 0.8\text{V}$ , $I_{OH} = -400\mu\text{A}$	2.7	---	---	V
	$V_{OL}$	$V_{CC} = 4.75\text{V}$ , $V_{IH} = 2\text{V}$ $I_{OL} = 4\text{mA}$	---	---	0.4	V
		$V_{IL} = 0.8\text{V}$ $I_{OL} = 8\text{mA}$	---	---	0.5	V
Input current	$I_{IH}$	$V_{CC} = 5.25\text{V}$ , $V_I = 2.7\text{V}$	---	---	20	$\mu\text{A}$
	$I_{IL}$	$V_{CC} = 5.25\text{V}$ , $V_I = 0.4\text{V}$	---	---	-0.4	$\text{mA}$
	$I_I$	$V_{CC} = 5.25\text{V}$ , $V_I = 7\text{V}$	---	---	0.1	$\text{mA}$
Short-circuit output current	$I_{OS}$	$V_{CC} = 5.25\text{V}$	-20	---	-100	$\text{mA}$
Supply current**	$I_{CC}$	$V_{CC} = 5.25\text{V}$	---	20	32	$\text{mA}$
Input clamp voltage	$V_{IK}$	$V_{CC} = 4.75\text{V}$ , $I_{IK} = -18\text{mA}$	---	---	-1.5	V

\*  $V_{CC} = 5\text{V}$ ,  $T_a = 25^\circ\text{C}$

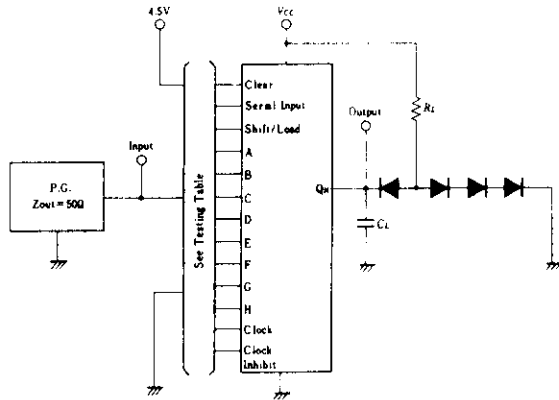
\*\* With all outputs open, 4.5V applied to the serial input and all other inputs except the clock grounded,  $I_{CC}$  is measured after a momentary ground, then 4.5V, is applied to clock.

## ■ SWITCHING CHARACTERISTICS ( $V_{CC} = 5\text{V}$ , $T_a = 25^\circ\text{C}$ )

Item	Symbol	Inputs	Test Conditions	min	typ	max	Unit
Maximum clock frequency	$f_{max}$			25	35	---	MHz
Propagation delay time	$t_{PHL}$	Clear	$C_L = 15\text{pF}$	---	19	30	ns
	$t_{PHL}$	Clock	$R_L = 2\text{k}\Omega$	7	14	25	ns
	$t_{PLH}$			5	11	20	ns

## ■ TESTING METHOD

### 1) Test Circuit

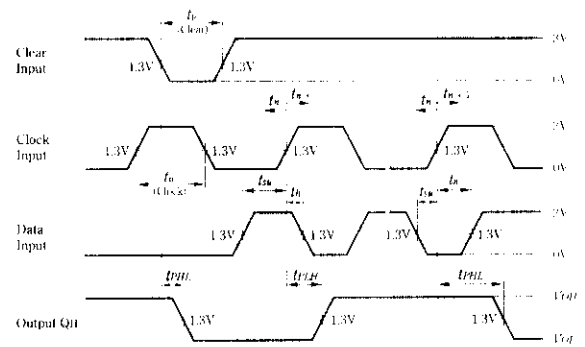


- Notes) 1.  $C_L$  includes probe and jig capacitance.  
2. All diodes are 1S2074 (H).

### 2) Testing Table

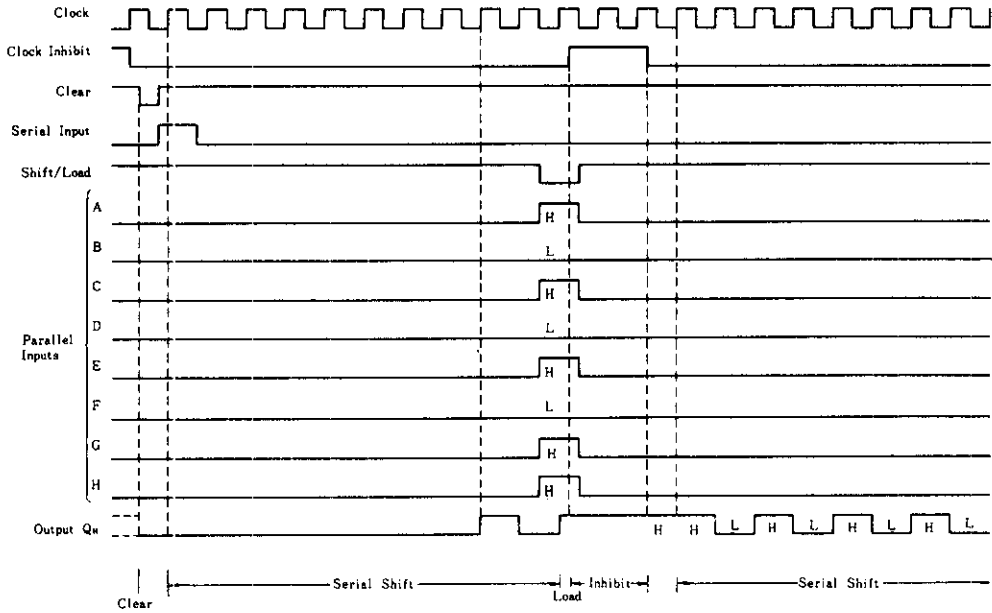
Data inputs	Shift/Load	Output	Bit time
Data H	0V	$Q_H$	$t_{n+1}$
Serial-in	4.5V	$Q_H$	$t_{n+8}$

### Waveform



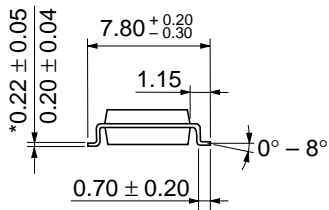
- Notes) 1. Input pulse:  $t_{TLH} \leq 15\text{ns}$ ,  $t_{THL} \leq 6\text{ns}$ ,  $PRR = 1\text{MHz}$  duty cycle 50%  
Clock input:  $t_w \geq 20\text{ns}$   
Clear input:  $t_w \geq 20\text{ns}$ ,  $t_h = 10\text{ns}$ , when testing  $f_{max}$ , vary the clock  $PRR$ .  
2. Propagation delay time ( $t_{PLH}$  and  $t_{PHL}$ ) are measured at  $t_{n+1}$ . Proper shifting of data is verified at  $t_{n+8}$  with a functional test.  
3.  $t_n$ ; bit time before clocking transition.  
 $t_{n+1}$ ; bit time after one clocking transition.  
 $t_{n+8}$ ; bit time after eight clocking transition.

## ■ TYPICAL CLEAR, SHIFT, LOAD, INHIBIT, AND SHIFT SEQUENCES



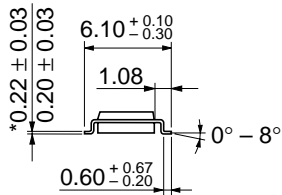


Hitachi Code	DP-16
JEDEC	Conforms
EIAJ	Conforms
Weight (reference value)	1.07 g



\*Dimension including the plating thickness  
Base material dimension

Hitachi Code	FP-16DA
JEDEC	—
EIAJ	Conforms
Weight (reference value)	0.24 g



\*Dimension including the plating thickness  
Base material dimension

Hitachi Code	FP-16DN
JEDEC	Conforms
EIAJ	Conforms
Weight (reference value)	0.15 g

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