

## DM54LS165/DM74LS165 8-Bit Parallel In/Serial Output Shift Registers

### General Description

This device is an 8-bit serial shift register which shifts data in the direction of  $Q_A$  toward  $Q_H$  when clocked. Parallel-in access is made available by eight individual direct data inputs, which are enabled by a low level at the shift/load input. These registers also feature gated clock inputs and complementary outputs from the eighth bit.

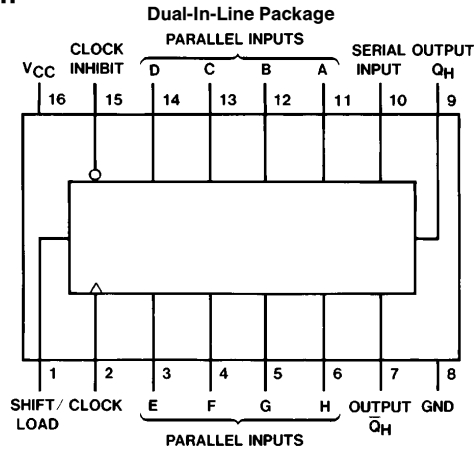
Clocking is accomplished through a 2-input NOR gate, permitting one input to be used as a clock-inhibit function. Holding either of the clock inputs high inhibits clocking, and holding either clock input low with the load input high enables the other clock input. The clock-inhibit input should be changed to the high level only while the clock input is high. Parallel loading is inhibited as long as the load input is high.

Data at the parallel inputs are loaded directly into the register on a high-to-low transition of the shift/load input, regardless of the logic levels on the clock, clock inhibit, or serial inputs.

### Features

- Complementary outputs
- Direct overriding (data) inputs
- Gated clock inputs
- Parallel-to-serial data conversion
- Typical frequency 35 MHz
- Typical power dissipation 105 mW

### Connection Diagram



TL/F/6399-1

Order Number DM54LS165J, DM54LS165W, DM74LS165WM or DM74LS165N  
See NS Package Number J16A, M16B, N16E or W16A

### Function Table

Inputs					Internal Outputs		Output $Q_H$
Shift/Load	Clock Inhibit	Clock	Serial	Parallel	$Q_A$	$Q_B$	
				A...H			
L	X	X	X	a...h	a	b	h
H	L	L	X	X	$Q_{A0}$	$Q_{B0}$	$Q_{H0}$
H	L	↑	H	X	H	$Q_{An}$	$Q_{Gn}$
H	L	↑	L	X	L	$Q_{An}$	$Q_{Gn}$
H	H	X	X	X	$Q_{A0}$	$Q_{B0}$	$Q_{H0}$

H = High Level (steady state), L = Low Level (steady state)

X = Don't Care (any input, including transitions)

↑ = Transition from low-to-high level

a...h = The level of steady-state input at inputs A through H, respectively.

$Q_{A0}$ ,  $Q_{B0}$ ,  $Q_{H0}$  = The level of  $Q_A$ ,  $Q_B$ , or  $Q_H$ , respectively, before the indicated steady-state input conditions were established.

$Q_{An}$ ,  $Q_{Gn}$  = The level of  $Q_A$  or  $Q_G$ , respectively, before the most recent ↑ transition of the clock.

## Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54LS	−55°C to +125°C
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

## Recommended Operating Conditions

Symbol	Parameter	DM54LS165			DM74LS165			Units
		Min	Nom	Max	Min	Nom	Max	
V <sub>CC</sub>	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V <sub>IH</sub>	High Level Input Voltage	2			2			V
V <sub>IL</sub>	Low Level Input Voltage			0.7			0.8	V
I <sub>OH</sub>	High Level Output Current			−0.4			−0.4	mA
I <sub>OL</sub>	Low Level Output Current			4			8	mA
f <sub>CLK</sub>	Clock Frequency (Note 1)			30	0		25	MHz
f <sub>CLK</sub>	Clock Frequency (Note 2)				0		20	MHz
t <sub>W</sub>	Pulse Width (Note 2)	Clock	18		25			ns
		Load	15		15			
t <sub>SU</sub>	Setup Time (Note 6)	Parallel	10		10			ns
		Serial	10		20			
		Enable	10		30			
		Shift	10		45			
t <sub>H</sub>	Hold Time (Note 6)	5			0			ns
T <sub>A</sub>	Free Air Operating Temperature	−55		125	0		70	°C

## Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 3)	Max	Units
V <sub>I</sub>	Input Clamp Voltage	V <sub>CC</sub> = Min, I <sub>I</sub> = −18 mA			−1.5	V
V <sub>OH</sub>	High Level Output Voltage	V <sub>CC</sub> = Min, I <sub>OH</sub> = Max	DM54	2.5		V
		V <sub>IL</sub> = Max, V <sub>IH</sub> = Min	DM74	2.7	3.4	
V <sub>OL</sub>	Low Level Output Voltage	V <sub>CC</sub> = Min, I <sub>OL</sub> = Max	DM54		0.4	V
		V <sub>IL</sub> = Max, V <sub>IH</sub> = Min	DM74	0.35	0.5	
		I <sub>OL</sub> = 4 mA, V <sub>CC</sub> = Min		0.25	0.4	
I <sub>I</sub>	Input Current @ Max Input Voltage	V <sub>CC</sub> = Max, V <sub>I</sub> = 7V (DM74)	Shift/Load		0.3	mA
		V <sub>I</sub> = 10V (DM54)	Others		0.1	
I <sub>IH</sub>	High Level Input Current	V <sub>CC</sub> = Max	Shift/Load		60	μA
		V <sub>I</sub> = 2.7V	Others		20	
I <sub>IL</sub>	Low Level Input Current	V <sub>CC</sub> = Max	Shift/Load		−1.2	mA
		V <sub>I</sub> = 0.4V	Others		−0.4	
I <sub>OS</sub>	Short Circuit Output Current	V <sub>CC</sub> = Max (Note 4)	DM54	−20	−100	mA
			DM74	−20	−100	
I <sub>CC</sub>	Supply Current	V <sub>CC</sub> = Max (Note 5)		21	36	mA

Note 1: C<sub>L</sub> = 15 pF, R<sub>L</sub> = 2 kΩ, T<sub>A</sub> = 25°C and V<sub>CC</sub> = 5V

Note 2: C<sub>L</sub> = 50 pF, R<sub>L</sub> = 2 kΩ, T<sub>A</sub> = 25°C and V<sub>CC</sub> = 5V

Note 3: All typicals are at V<sub>CC</sub> = 5V, T<sub>A</sub> = 25°C.

Note 4: Not more than one output should be shorted at a time, and the duration should not exceed one second.

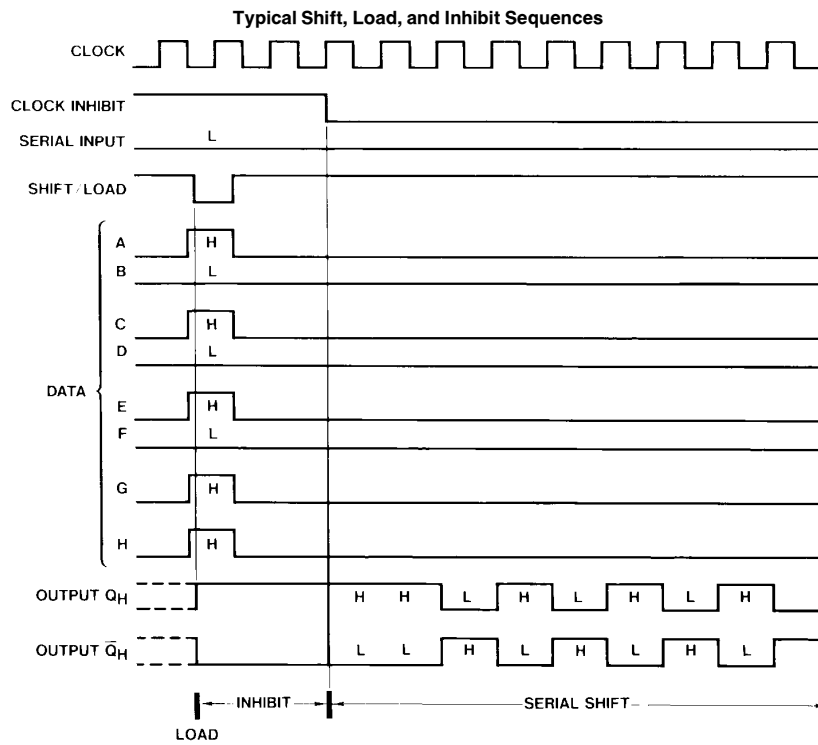
Note 5: With all outputs open, clock inhibit and shift/load at 4.5V, and a clock pulse applied to the CLOCK input, I<sub>CC</sub> is measured first with the parallel inputs at 4.5V, then again grounded.

Note 6: T<sub>A</sub> = 25°C and V<sub>CC</sub> = 5V.

## Switching Characteristics at $V_{CC} = 5V$ and $T_A = 25^\circ C$

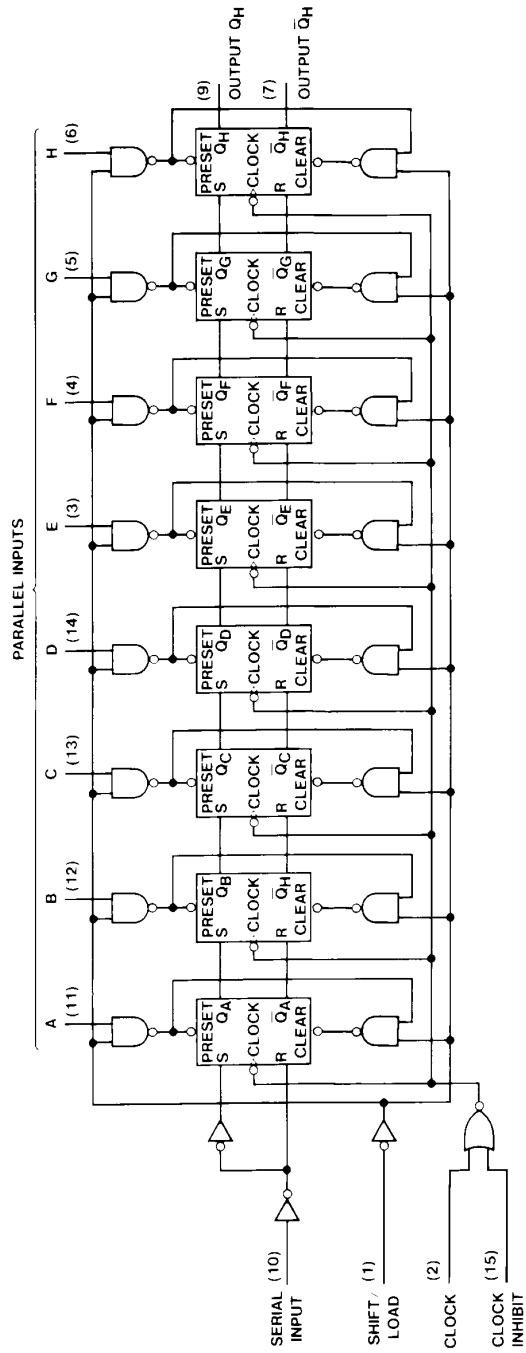
Symbol	Parameter	From (Input) To (Output)	DM54LS		DM74LS		DM74LS		Units
			$C_L = 15 \text{ pF}$		$C_L = 15 \text{ pF}$		$R_L = 2 \text{ k}\Omega$ $C_L = 50 \text{ pF}$		
			Min	Max	Min	Max	Min	Max	
$f_{MAX}$	Maximum Clock Frequency		25		25		20		MHz
$t_{PLH}$	Propagation Delay Time Low to High Level Output	Load to Any Q		30		35		37	ns
$t_{PHL}$	Propagation Delay Time High to Low Level Output	Load to Any Q		30		35		42	ns
$t_{PLH}$	Propagation Delay Time Low to High Level Output	Clock to Any Q		30		40		42	ns
$t_{PHL}$	Propagation Delay Time High to Low Level Output	Clock to Any Q		30		40		47	ns
$t_{PLH}$	Propagation Delay Time Low to High Level Output	H to $Q_H$		20		25		27	ns
$t_{PHL}$	Propagation Delay Time High to Low Level Output	H to $Q_H$		30		30		37	ns
$t_{PLH}$	Propagation Delay Time Low to High Level Output	H to $\bar{Q}_H$		30		30		32	ns
$t_{PHL}$	Propagation Delay Time High to Low Level Output	H to $\bar{Q}_H$		25		25		32	ns

## Timing Diagram



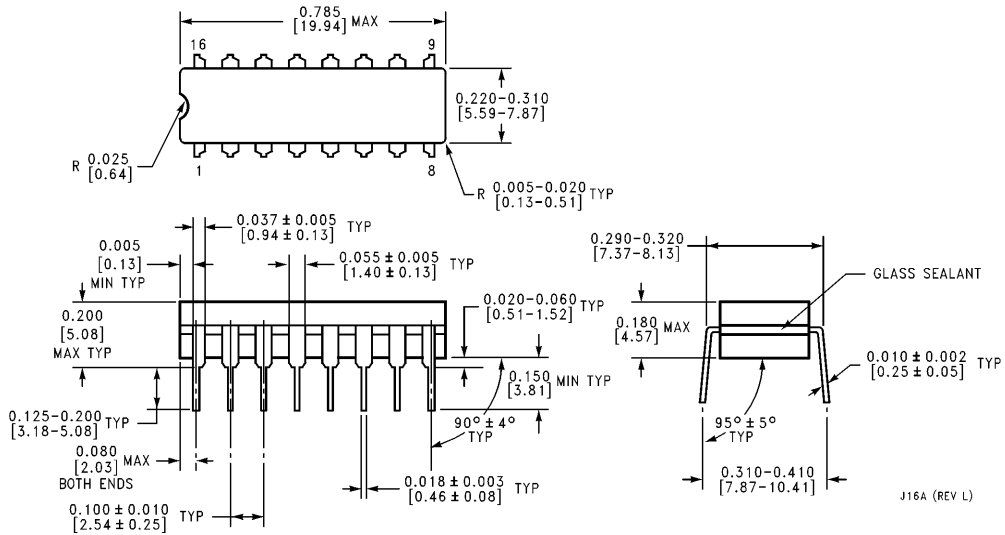
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# Logic Diagram

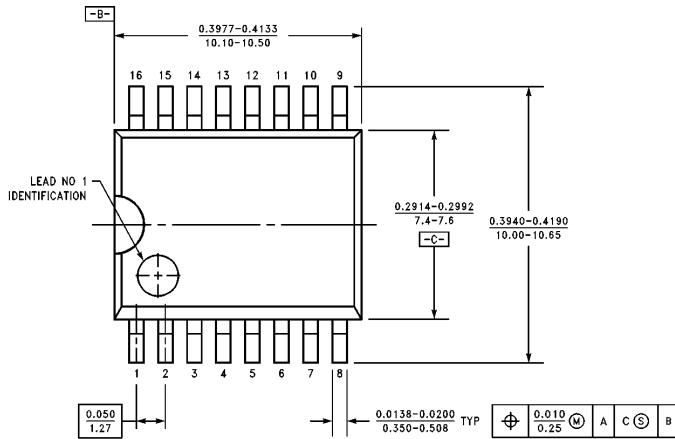


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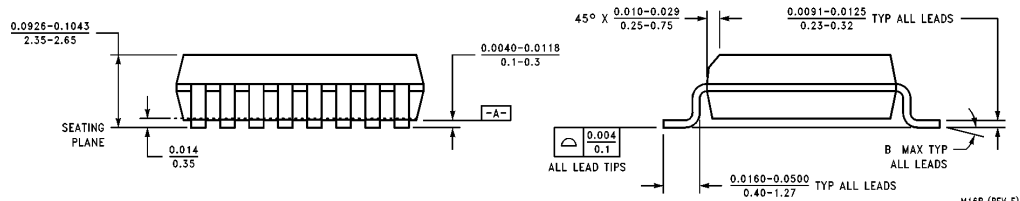
**Physical Dimensions** inches (millimeters)



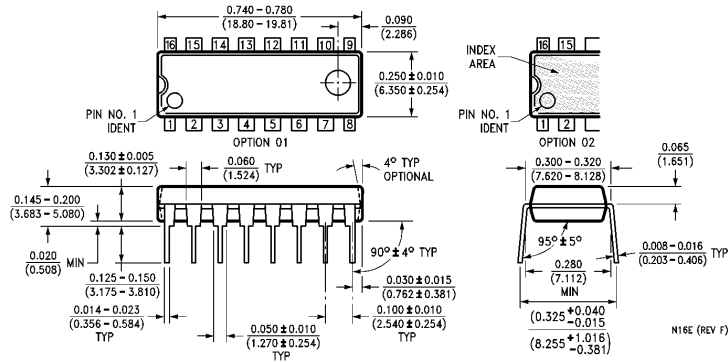
**16-Lead Ceramic Dual-In-Line Package (J)**  
**Order Number DM54LS165J**  
**NS Package Number J16A**



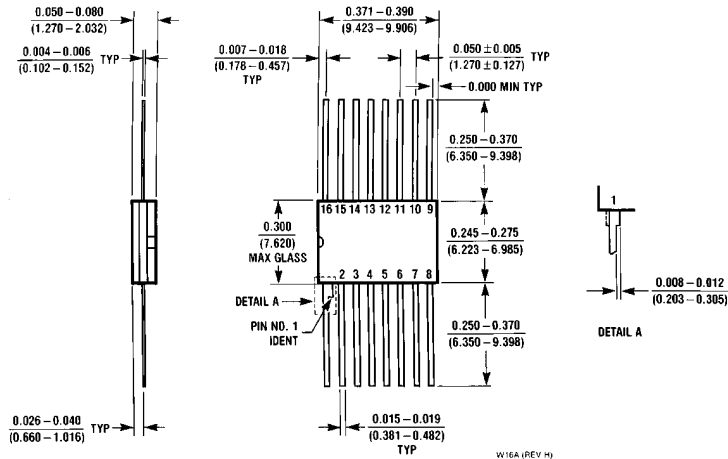
**16-Lead Wide Small Outline Molded Package (M)**  
**Order Number DM74LS165WM**  
**NS Package Number M16B**



**Physical Dimensions** inches (millimeters) (Continued)



**16-Lead Molded Dual-In-Line Package (N)**  
**Order Number DM74LS165N**  
**NS Package Number N16E**




**16-Lead Ceramic Flat Package (W)**  
**Order Number DM54LS165W**  
**NS Package Number W16A**

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