

CD4023M/CD4023C Triple 3-Input NAND Gate CD4025M/CD4025C Triple 3-Input NOR Gate

General Description

These triple gates are monolithic complementary MOS (CMOS) integrated circuits constructed with N- and P-channel enhancement mode transistors. All inputs are protected against static discharge with diodes to V_{DD} and V_{SS} .

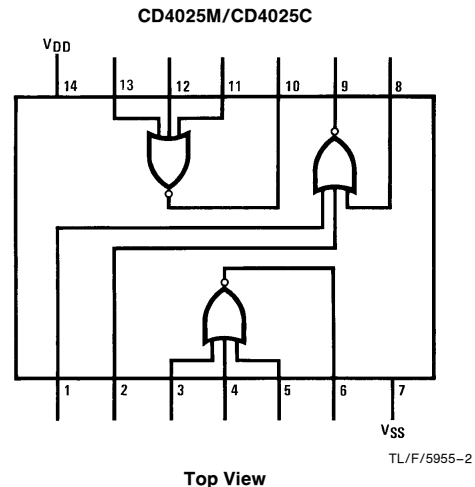
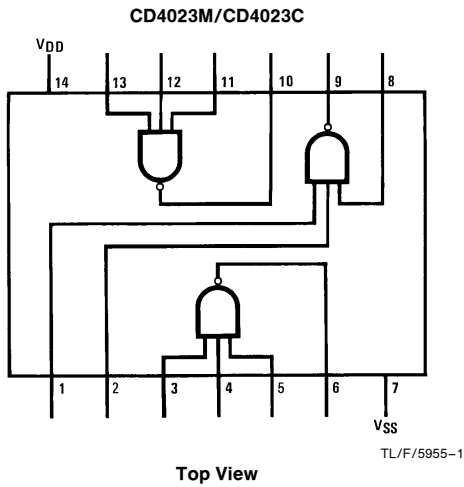
Features

- Wide supply voltage range
- High noise immunity
- 5V–10V parametric ratings
- Low power

3.0V to 15V
0.45 V_{DD} (typ.)

Connection Diagrams

Dual-In-Line Packages



Order Number CD4023 or CD4025

CD4023M/CD4023C Triple 3-Input NAND Gate
CD4025M/CD4025C Triple 3-Input NOR Gate

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Voltage at Any Pin $V_{SS} -$ to $V_{DD} + 0.3V$

Operating Temperature Range
 CD4023M, CD4025M $-55^{\circ}C$ to $+125^{\circ}C$
 CD4023C, CD4025C $-40^{\circ}C$ to $+85^{\circ}C$

Storage Temperature Range $-65^{\circ}C$ to $+150^{\circ}C$

Power Dissipation (P_D)
 Dual-In-Line 700 mW
 Small Outline 500 mW

Operating V_{DD} Range $V_{SS} + 3.0V$ to $V_{SS} + 15V$

Lead Temperature (Soldering, 10 seconds) $260^{\circ}C$

DC Electrical Characteristics CD4023M, CD4025M

Symbol	Parameter	Conditions	Limits						Units	
			$-55^{\circ}C$		$+25^{\circ}C$			$+125^{\circ}C$		
			Min	Max	Min	Typ	Max	Min		Max
I_L	Quiescent Device Current	$V_{DD} = 5.0V$ $V_{DD} = 10V$		0.05		0.001	0.05		3.0	μA
				0.1		0.001	0.1		6.0	μA
P_D	Quiescent Device Dissipation/Package	$V_{DD} = 5.0V$ $V_{DD} = 10V$		0.25		0.005	0.25		15	μW
				1.0		0.01	1.0		60	μW
V_{OL}	Output Voltage Low Level	$V_{DD} = 5.0V, V_I = V_{DD}, I_O = 0A$ $V_{DD} = 10V, V_I = V_{DD}, I_O = 0A$		0.05		0	0.05		0.05	V
				0.05		0	0.05		0.05	V
V_{OH}	Output Voltage High Level	$V_{DD} = 5.0V, V_I = V_{SS}, I_O = 0A$ $V_{DD} = 10V, V_I = V_{SS}, I_O = 0A$	4.95		4.95	5.0		4.95		V
			9.95		9.95	10		9.95		V
V_{NL}	Noise Immunity (All Inputs)	$V_{DD} = 5.0V, V_O = 3.6V, I_O = 0A$ $V_{DD} = 10V, V_O = 7.2V, I_O = 0A$	1.5		1.5	2.25		1.4		V
			3.0		3.0	4.5		2.9		V
V_{NH}	Noise Immunity (All Inputs)	$V_{DD} = 5.0V, V_O = 0.95V, I_O = 0A$ $V_{DD} = 10V, V_O = 2.9V, I_O = 0A$	1.4		1.5	2.25		1.5		V
			2.9		3.0	4.5		3.0		V
I_{DN}	Output Drive Current N-Channel (4025) (Note 2)	$V_{DD} = 5.0V, V_O = 0.4V, V_I = V_{DD}$ $V_{DD} = 10V, V_O = 0.5V, V_I = V_{DD}$	0.5		0.40	1.0		0.28		mA
			1.1		0.9	2.5		0.65		mA
I_{DP}	Output Drive Current P-Channel (4025) (Note 2)	$V_{DD} = 5.0V, V_O = 2.5V, V_I = V_{SS}$ $V_{DD} = 10V, V_O = 9.5V, V_I = V_{SS}$	-0.62		-0.5	-2.0		-0.35		mA
			-0.62		-0.5	-1.0		-0.35		mA
I_{DN}	Output Drive Current N-Channel (4023) (Note 2)	$V_{DD} = 5.0V, V_O = 0.4V, V_I = V_{DD}$ $V_{DD} = 10V, V_O = 0.5V, V_I = V_{DD}$	0.31		0.25	0.5		0.175		mA
			0.63		0.5	0.6		0.35		mA
I_{DP}	Output Drive Current P-Channel (4023) (Note 2)	$V_{DD} = 5.0V, V_O = 2.5V, V_I = V_{SS}$ $V_{DD} = 10V, V_O = 9.5V, V_I = V_{SS}$	-0.31		-0.25	-0.5		-0.175		mA
			-0.75		-0.6	-1.2		-0.4		mA
I_I	Input Current				10				pA	

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The tables of "Recommended Operating Conditions" and "Electrical Characteristics" provide conditions for actual device operation.

Note 2: I_{DN} and I_{DP} are tested one output at a time.

DC Electrical Characteristics CD4023C, CD4025C

Symbol	Parameter	Conditions	Limits						Units	
			-40°C		+25°C		+85°C			
			Min	Max	Min	Typ	Max	Min		Max
I _L	Quiescent Device Current	V _{DD} = 5.0V V _{DD} = 10V		0.05		0.005	0.5		15	μA
				5.0		0.005	5.0		30	μA
P _D	Quiescent Device Dissipation/Package	V _{DD} = 5.0V V _{DD} = 10V		2.5		0.025	2.5		75	μW
				50		0.05	50		300	μW
V _{OL}	Output Voltage Low Level	V _{DD} = 5.0V, V _I = V _{DD} , I _O = 0A V _{DD} = 10V, V _I = V _{DD} , I _O = 0A		0.01		0	0.01		0.05	V
				0.01		0	0.01		0.05	V
V _{OH}	Output Voltage High Level	V _{DD} = 5.0V, V _I = V _{SS} , I _O = 0A V _{DD} = 10V, V _I = V _{SS} , I _O = 0A	4.99		4.99	5.0		4.95		V
			9.99		9.99	10		9.95		V
I _I	Input Current				10					pA
V _{NL}	Noise Immunity (All Inputs)	V _{DD} = 5.0V, V _O = 3.6V, I _O = 0A V _{DD} = 10V, V _O = 7.2V, I _O = 0A	1.5		1.5	2.25		1.4		V
			3.0		3.0	4.5		2.9		V
V _{NH}	Noise Immunity (All Inputs)	V _{DD} = 5.0V, V _O = 0.95V, I _O = 0A V _{DD} = 10V, V _O = 2.9V, I _O = 0A	1.4		1.5	2.25		1.5		V
			2.9		3.0	4.5		3.0		V
I _{DN}	Output Drive Current N-Channel (4025) (Note 2)	V _{DD} = 5.0V, V _O = 0.4V, V _I = V _{DD} V _{DD} = 10V, V _O = 0.5V, V _I = V _{DD}	0.35		0.3	1.0		0.24		mA
			0.72		0.6	2.5		0.48		mA
I _{DP}	Output Drive Current P-Channel (4025) (Note 2)	V _{DD} = 5.0V, V _O = 2.5V, V _I = V _{SS} V _{DD} = 10V, V _O = 9.5V, V _I = V _{SS}	-0.35		-0.3	-2.0		-0.24		mA
			-0.3		-0.25	-1.0		-0.2		mA
I _{DN}	Output Drive Current N-Channel (4023) (Note 2)	V _{DD} = 5.0V, V _O = 0.4V, V _I = V _{DD} V _{DD} = 10V, V _O = 0.5V, V _I = V _{DD}	0.145		0.12	0.5		0.095		mA
			0.3		0.25	0.6		0.2		mA
I _{DP}	Output Drive Current P-Channel (4023) (Note 2)	V _{DD} = 5.0V, V _O = 2.5V, V _I = V _{SS} V _{DD} = 10V, V _O = 9.5V, V _I = V _{SS}	-0.145		-0.12	-0.5		-0.095		mA
			-0.35		-0.3	-1.2		-0.24		mA
I _I	Input Current				10					pA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The tables of "Recommended Operating Conditions" and "Electrical Characteristics" provide conditions for actual device operation.

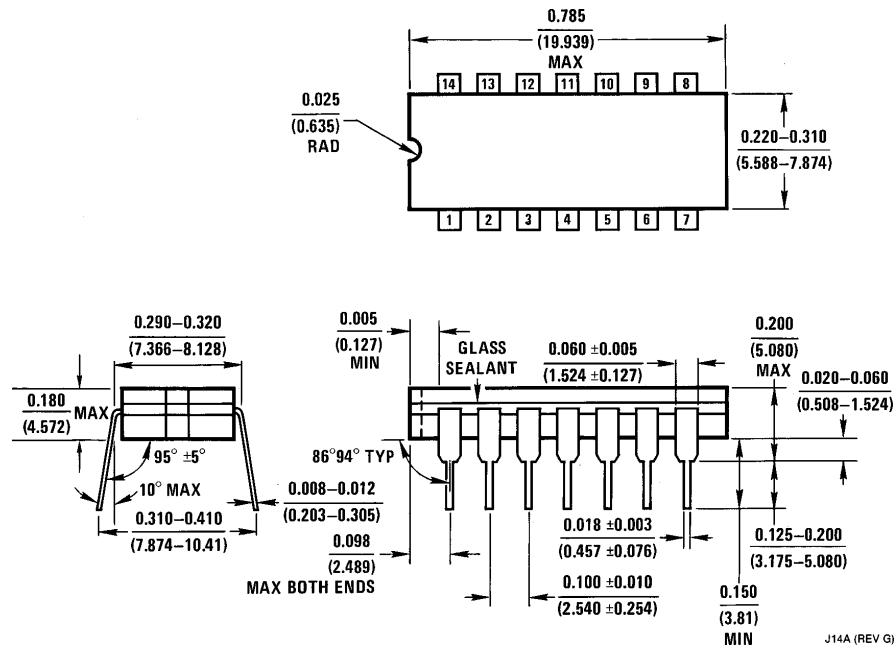
Note 2: I_{DN} and I_{DP} are tested one output at a time.

AC Electrical Characteristics* $T_A = 25^\circ\text{C}$, $C_L = 15\text{ pF}$, and input rise and fall times = 20 ns. Typical temperature coefficient for all values of $V_{DD} = 0.3\%/^\circ\text{C}$

Symbol	Parameter	Conditions	Min	Typ	Max	Units
CD4025M						
t_{PHL}	Propagation Delay Time High to Low Level	$V_{DD} = 5.0\text{V}$		35	50	ns
		$V_{DD} = 10\text{V}$		25	40	ns
t_{PLH}	Propagation Delay Time Low to High Level	$V_{DD} = 5.0\text{V}$		35	40	ns
		$V_{DD} = 10\text{V}$		25	70	ns
t_{THL}	Transition Time High to Low Level	$V_{DD} = 5.0\text{V}$		65	125	ns
		$V_{DD} = 10\text{V}$		35	70	ns
t_{TLH}	Transition Time Low to High Level	$V_{DD} = 5.0\text{V}$		65	175	ns
		$V_{DD} = 10\text{V}$		35	75	ns
C_I	Input Capacitance	Any Input		5.0		pF
CD4025C						
t_{PHL}	Propagation Delay Time High to Low Level	$V_{DD} = 5.0\text{V}$		35	80	ns
		$V_{DD} = 10\text{V}$		25	55	ns
t_{PLH}	Propagation Delay Time Low to High Level	$V_{DD} = 5.0\text{V}$		35	120	ns
		$V_{DD} = 10\text{V}$		25	65	ns
t_{THL}	Transition Time High to Low Level	$V_{DD} = 5.0\text{V}$		65	200	ns
		$V_{DD} = 10\text{V}$		35	115	ns
t_{TLH}	Transition Time Low to High Level	$V_{DD} = 5.0\text{V}$		65	300	ns
		$V_{DD} = 10\text{V}$		35	125	ns
C_I	Input Capacitance	Any Input		5.0		pF
CD4023M						
t_{PHL}	Propagation Delay Time High to Low Level	$V_{DD} = 5.0\text{V}$		50	75	ns
		$V_{DD} = 10\text{V}$		25	40	ns
t_{PLH}	Propagation Delay Time Low to High Level	$V_{DD} = 5.0\text{V}$		50	75	ns
		$V_{DD} = 10\text{V}$		25	40	ns
t_{THL}	Transition Time High to Low Level	$V_{DD} = 5.0\text{V}$		75	125	ns
		$V_{DD} = 10\text{V}$		50	75	ns
t_{TLH}	Transition Time Low to High Level	$V_{DD} = 5.0\text{V}$		75	100	ns
		$V_{DD} = 10\text{V}$		40	60	ns
C_I	Input Capacitance	Any Input		5.0		pF
CD4023C						
t_{PHL}	Propagation Delay Time High to Low Level	$V_{DD} = 5.0\text{V}$		50	100	ns
		$V_{DD} = 10\text{V}$		25	50	ns
t_{PLH}	Propagation Delay Time Low to High Level	$V_{DD} = 5.0\text{V}$		50	100	ns
		$V_{DD} = 10\text{V}$		25	50	ns
t_{THL}	Transition Time High to Low Level	$V_{DD} = 5.0\text{V}$		75	150	ns
		$V_{DD} = 10\text{V}$		50	100	ns
t_{TLH}	Transition Time Low to High Level	$V_{DD} = 5.0\text{V}$		75	125	ns
		$V_{DD} = 10\text{V}$		40	75	ns
C_I	Input Capacitance	Any Input		5.0		pF

*AC Parameters are guaranteed by DC correlated testing.

Physical Dimensions inches (millimeters)

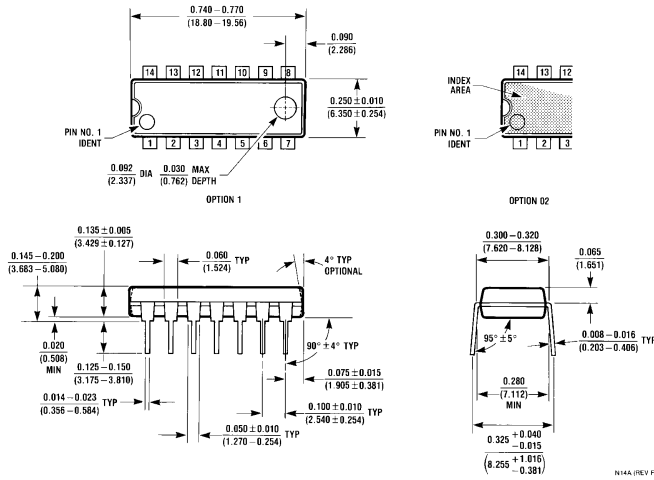


Ceramic Dual-In-Line Package (J)
Order Number CD4023MJ, CD4023CJ, CD4025MJ or CD4025CJ
NS Package Number J14A

J14A (REV G)

**CD4023M/CD4023C Triple 3-Input NAND Gate
CD4025M/CD4025C Triple 3-Input NOR Gate**

Physical Dimensions inches (millimeters) (Continued)



Molded Dual-In-Line Package (N)
Order Number CD4023MN, CD4023CN, CD4025MN or CD4025CN
NS Package Number N14A

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