

FEATURES

0.0025% THD

Fast settling permits 2×, 4×, and 8× oversampling

±3 V output

Optional trim allows superlinear performance

±5 V to ±12 V operation

16-lead plastic SOIC package

Serial input

APPLICATIONS

Compact disc players

Digital audio amplifiers

DAT recorders and players

Synthesizers and keyboards

GENERAL DESCRIPTION

The **AD1856** is a monolithic, 16-bit pulse code modulation (PCM) audio DAC. The device provides a voltage output amplifier, 16-bit DAC, 16-bit serial-to-parallel input register, and voltage reference. The digital portion of the **AD1856** is fabricated with CMOS logic elements that are provided by the Analog Devices, Inc., BiMOS II process. The analog portion of the **AD1856** is fabricated with bipolar and MOS devices, as well as thin film resistors.

This combination of circuit elements, as well as careful design and layout techniques, results in high performance audio playback. Laser trimming of the linearity error affords extremely low total harmonic distortion. An optional linearity trim pin is provided to allow residual differential linearity error at midscale to be eliminated. This feature is particularly valuable for low distortion reconstructions of low amplitude signals. Output glitch is also small, contributing to the overall high level of performance. The output amplifier achieves fast settling and high slew rates, providing a full ±3 V signal at load currents of up to ±8 mA. The output amplifier is short-circuit protected and can withstand indefinite shorts to ground.

The serial input interface consists of the clock, data, and latch enable pins. The serial twos complement data-word is clocked into the DAC, MSB first, by the external data clock. The latch enable signal transfers the input word from the internal serial input register to the parallel DAC input register. The input clock can support a 10 MHz clock rate. The serial input port is compatible with popular digital filter chips used in consumer audio products. These filters operate at oversampling rates of 2×, 4×, and 8× the sampling frequency.

Rev. C

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FUNCTIONAL BLOCK DIAGRAM

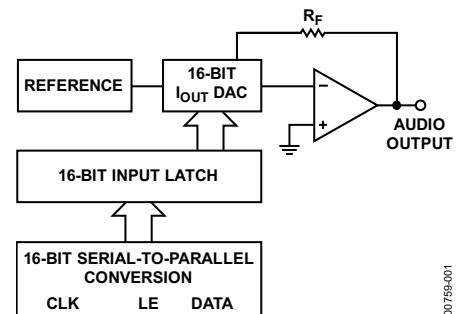


Figure 1.

00786-001

The **AD1856** can operate with ±5 V to ±12 V power supplies, making it suitable for both the portable and home-use markets. The digital supplies, +V_L and -V_L, can be separated from the analog supplies, +V_S and -V_S, for reduced digital crosstalk. Separate analog and digital ground pins are also provided.

Power dissipation is 110 mW (typical) with ±5 V supplies and 135 mW (typical) when ±12 V supplies are used.

The **AD1856** is packaged in a 16-lead plastic SOIC package and incorporates the industry-standard pinout. Operation is guaranteed over the temperature range of -25°C to +70°C and over the voltage supply range of ±4.75 V to ±13.2 V.

PRODUCT HIGHLIGHTS

1. Total harmonic distortion is 100% tested.
2. MSB trim feature allows superlinear operation.
3. The **AD1856** operates with ±5 V to ±12 V supplies.
4. Serial interface is compatible with digital filter chips.
5. 1.5 μs settling time permits 2×, 4×, and 8× oversampling.
6. No external components are required.
7. 96 dB dynamic range.
8. ±3 V or ±8 mA output capability.
9. 16-bit resolution.
10. Twos complement serial input words.
11. Low cost.
12. 16-lead plastic SOIC package.

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REVISION HISTORY

2/13—Rev. B to Rev. C

| | | | |
|---|-----------|--|----|
| Updated Format..... | Universal | Changes to Table 2..... | 5 |
| Deleted 16-Lead DIP (N) Package | Universal | Changes to Figure 2 and Table 3..... | 6 |
| Reorganized Layout..... | Universal | Deleted Figure 14 and Dual DAC, $4 \times f_s$ Oversampling Architecture Section..... | 7 |
| Changes to Features Section, General Description Section, and Product Highlights Section | 1 | Changes to Grounding Recommendations Section, Power Supplies and Decoupling Section, and Figure 3 | 9 |
| Changes to Total Harmonic Distortion Parameter and Power Supply Parameter, Table 1 | 3 | Changes to Input Data Section | 11 |
| Changes to Power Dissipation Parameter, Table 1 | 4 | Changes to Digital Filtering and Oversampling Section | 14 |
| Deleted Figure 1; Renumbered Sequentially..... | 4 | Updated Outline Dimensions..... | 15 |
| | | Changes to Ordering Guide | 15 |

SPECIFICATIONS

Typical values at $T_A = 25^\circ\text{C}$, $V_L = \pm 5\text{ V}$, and $V_S = \pm 5\text{ V}$, unless otherwise noted.

Table 1.

| Parameter | Test Conditions/Comments | Min | Typ | Max | Unit |
|---|--|---------|----------------------|---------------------|------------------|
| RESOLUTION ¹ | | | | 16 | Bits |
| DIGITAL INPUTS | | | | | |
| Input Voltage High, V_{IH} | | 0 | 2.4 | $+V_L$ | V |
| Input Voltage Low, V_{IL} | | | 0.8 | | V |
| Input Current High, I_{IH} ¹ | $V_{IH} = +V_L$ | | | 1.0 | μA |
| Input Current Low, I_{IL} ¹ | $V_{IL} = 0.4\text{ V}$ | | | -10 | μA |
| Clock Input Frequency ¹ | | 10 | | | MHz |
| ACCURACY | | | | | |
| Gain Error | | | ± 2.0 | | % |
| Bipolar Zero Error | | | ± 30 | | mV |
| Differential Linearity Error | | | ± 0.001 | | % of FSR |
| Noise at Bipolar Zero | RMS, 20 Hz to 20 kHz | | 6 | | μV |
| TOTAL HARMONIC DISTORTION | | | | | |
| 0 dB | 990.5 Hz AD1856RZ-K AD1856RZ | | 0.002 | 0.0025 ¹ | % |
| -20 dB | AD1856RZ-K AD1856RZ | | 0.002 | 0.008 ¹ | % |
| -60 dB | AD1856RZ-K AD1856RZ | | 0.018 | 0.020 ¹ | % |
| | AD1856RZ-K AD1856RZ | | 0.018 | 0.040 ¹ | % |
| | AD1856RZ-K AD1856RZ | | 1.8 | 2.0 ¹ | % |
| | AD1856RZ-K AD1856RZ | | 1.8 | 4.0 ¹ | % |
| MONOTONICITY | | | | | |
| | | | 15 | | Bits |
| DRIFT | | | | | |
| | 0°C to 70°C | | | | |
| Total Drift | | | ± 25 | | ppm of FSR/°C |
| Bipolar Zero Drift | | | ± 4 | | ppm of FSR/°C |
| SETTLING TIME | | | | | |
| Voltage Output | To $\pm 0.006\%$ of FSR 6 V step 1 LSB step | | 1.5 | | μs |
| Slew Rate | | | 1.0 | | μs |
| Current Output | 1 mA step, 10 Ω to 100 Ω load 1 k Ω load | | 9 | | V/ μs |
| | | | 350 | | ns |
| | | | 350 | | ns |
| WARM-UP TIME | | | | | |
| | | 1 | | | Minute |
| OUTPUT | | | | | |
| Voltage Output Configuration | | | ± 3 | | V |
| Bipolar Range | | ± 8 | | | mA |
| Output Current | | | 0.1 | | Ω |
| Output Impedance | | | Indefinite to ground | | |
| Short-Circuit Duration | | | | | |
| Current Output Configuration | | | ± 1.0 | | mA |
| Bipolar Range ($\pm 30\%$) | | | 1.7 | | k Ω |
| Output Impedance ($\pm 30\%$) | | | | | |
| POWER SUPPLY | | | | | |
| Voltage, $+V_L$ and $+V_S$ | $+V_S \geq +V_L$ for operation | 4.75 | 5 | 13.2 | V |
| Voltage, $-V_L$ and $-V_S$ | $-V_L \geq -V_S$ for operation | -13.2 | -5 | -4.75 | V |
| Current, +I | $+V_L$ and $+V_S = 5\text{ V}$, 10 MHz clock | | 10 | 15 ¹ | mA |
| | $+V_L$ and $+V_S = 12\text{ V}$, 10 MHz clock | | 12 | | mA |
| Current, -I | $-V_L$ and $-V_S = -5\text{ V}$, 10 MHz clock | | -12 | -15 ¹ | mA |
| | $-V_L$ and $-V_S = -12\text{ V}$, 10 MHz clock | | -15 | | mA |

| Parameter | Test Conditions/Comments | Min | Typ | Max | Unit |
|-------------------|---|-----|-----|------------------|------|
| POWER DISSIPATION | 10 MHz clock | | | | |
| | $\pm V_S$ and $\pm V_L = \pm 5\text{ V}$ | | 110 | 150 ¹ | mW |
| | $\pm V_S$ and $\pm V_L = \pm 12\text{ V}$ | | 135 | | mW |
| TEMPERATURE RANGE | | | | | |
| Specification | | 0 | | +70 | °C |
| Operational | | -25 | | +70 | °C |
| Storage | | -60 | | +100 | °C |

¹ Tested on all production units at final test.

ABSOLUTE MAXIMUM RATINGS

Table 2.

| Parameter | Rating |
|---------------------------|----------------------------|
| +V _L to DGND | 0 V to 13.2 V |
| +V _S to AGND | 0 V to 13.2 V |
| -V _L to DGND | -13.2 V to 0 V |
| -V _S to AGND | -13.2 V to 0 V |
| Digital Inputs to DGND | -0.3 V to +V _L |
| AGND to DGND | ±0.3 V |
| Short-Circuit Protection | Indefinite short to ground |
| Soldering, 10 sec | 300°C |
| Storage Temperature Range | -60°C to +100°C |

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

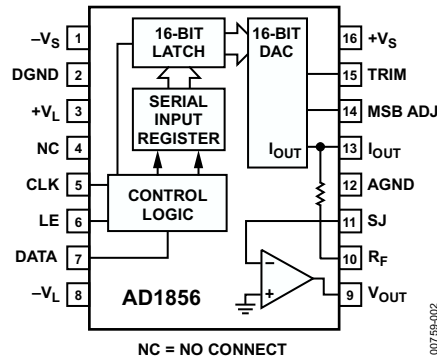


Figure 2. Pin Configuration

Table 3. Pin Function Descriptions

| Pin No. | Mnemonic | Description |
|---------|-----------|-------------------------------------|
| 1 | $-V_S$ | Analog Power Supply, Negative |
| 2 | DGND | Digital Ground |
| 3 | $+V_L$ | Logic Power Supply, Positive |
| 4 | NC | No Connection |
| 5 | CLK | Data Clock Input |
| 6 | LE | Latch Enable Input |
| 7 | DATA | Serial Data Input |
| 8 | $-V_L$ | Logic Power Supply, Negative |
| 9 | V_{OUT} | Voltage Output |
| 10 | R_F | Feedback Resistor |
| 11 | SJ | Summing Junction |
| 12 | AGND | Analog Ground |
| 13 | I_{OUT} | Current Output |
| 14 | MSB ADJ | MSB Adjustment Terminal |
| 15 | TRIM | MSB Trimming Potentiometer Terminal |
| 16 | $+V_S$ | Analog Power Supply, Positive |

TERMINOLOGY

Total Harmonic Distortion

Total harmonic distortion (THD) is defined as the ratio of the square root of the sum of the squares of the harmonic values to the value of the fundamental input frequency. THD is expressed in percent (%) or decibels (dB).

THD is a measure of the magnitude and distribution of linearity error and differential linearity error. The distribution of these errors may be different, depending on the amplitude of the output signal. Therefore, to be most useful, THD should be specified for both large and small signal amplitudes.

Settling Time

Settling time is the time required for the output to reach and remain within a specified error band about its final value, measured from the digital input transition. Settling time is the primary measure of dynamic performance.

Dynamic Range

The dynamic range specification indicates the ratio of the smallest signal that the converter can resolve to the largest signal it is able to produce. As a ratio, it is usually expressed in decibels (dB).

The theoretical dynamic range of an n-bit converter is approximately $(6 \times n)$ dB. In the case of the 16-bit AD1856, that is 96 dB. The actual dynamic range of a converter is less than the theoretical value due to limitations imposed by noise, quantization error, and other errors.

Bipolar Zero Error

Bipolar zero error is the deviation in the actual analog output from the ideal output (0 V) when the two's complement input code representing half scale (all 0s) is loaded into the input register.

Differential Linearity Error

Differential linearity error is the measure of the variation in analog value, normalized to full scale, associated with a 1 LSB change in the digital input. Monotonic behavior requires that the differential linearity error not exceed 1 LSB in the negative direction.

Monotonicity

A digital-to-analog converter is monotonic if the output either increases or remains constant as the digital input increases.

THEORY OF OPERATION

The [AD1856](#) is a complete, monolithic, 16-bit PCM audio DAC. No additional external components are required for operation. As shown in the block diagram in Figure 1, each chip contains a voltage reference, an output amplifier, a 16-bit DAC, a 16-bit input latch, and a 16-bit serial-to-parallel input register.

The voltage reference consists of a band gap circuit and buffer amplifier. This circuitry produces an output voltage that is stable over time and temperature changes.

The 16-bit digital-to-analog converter uses a combination of a segmented decoder and R-2R architectures to achieve consistent linearity and differential linearity.

The resistors that form the ladder structure are fabricated with silicon-chromium thin film. Laser trimming of these resistors further reduces linearity error, resulting in low output distortion.

The output amplifier uses both MOS and bipolar devices to produce low offset, high slew rate, and optimum settling time. When combined with the on-board feedback resistor, the output op amp can convert the output current of the [AD1856](#) to a voltage output.

The automatic test equipment digitizes 4096 samples of the output test waveform, incorporating 23 complete cycles of the sine wave. A 4096-point FFT is performed on the results of the test. Based on the first nine harmonics of the fundamental 990.5 Hz output wave, the total harmonic distortion of the device is calculated. Neither a deglitcher nor an MSB trim is used during the THD test.

The circuit design, layout, and manufacturing techniques used in the production of the AD1856 result in excellent THD performance. Figure 5 shows the typical unadjusted THD performance of the AD1856 for various amplitudes of a 1 kHz output signal. As shown in Figure 5, the AD1856 offers excellent performance, even at amplitudes as low as -60 dB. Figure 6 shows the typical THD vs. frequency performance.

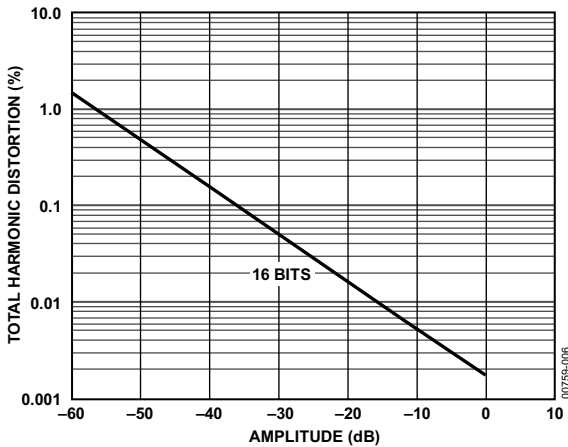


Figure 5. Typical Unadjusted THD vs. Amplitude

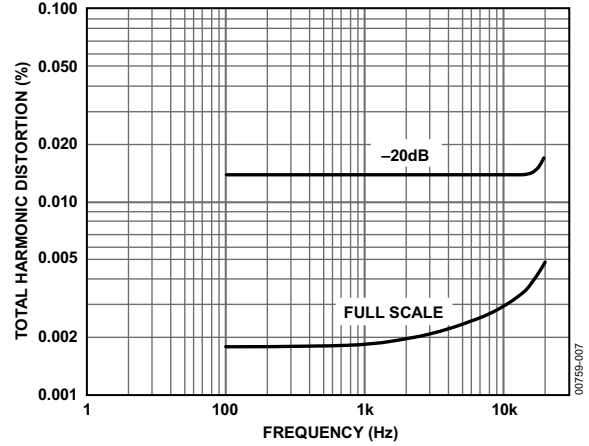


Figure 6. Typical THD vs. Frequency

OPTIONAL MSB ADJUSTMENT

Use of an optional adjustment circuit allows residual differential linearity errors around midscale to be eliminated. These errors are especially important when low amplitude signals are being reproduced. In these cases, as the signal amplitude decreases, the ratio of the midscale differential linearity error to the signal amplitude increases and THD increases.

Therefore, for best performance at low output levels, the optional MSB adjustment circuitry shown in Figure 7 can be used. This circuit allows the differential linearity error at midscale to be zeroed out. However, no adjustments are required to meet data sheet specifications.

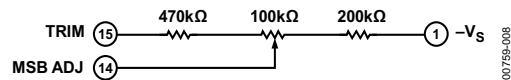


Figure 7. Optional MSB Adjustment Circuit

DIGITAL CIRCUIT CONSIDERATIONS

INPUT DATA

Data is transmitted to the [AD1856](#) in a bit stream composed of 16-bit words with a serial, MSB first format. Three signals must be present to achieve proper operation: the data, clock, and latch enable signals. Input data bits are clocked into the input register on the rising edge of the clock signal. The LSB is clocked in on the 16th clock pulse. When all data bits are loaded, a low-going latch enable pulse updates the DAC input. Figure 8 illustrates the general signal requirements for data transfer for the [AD1856](#).

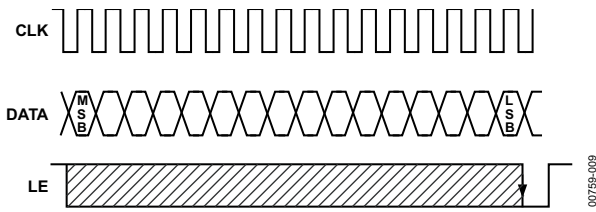


Figure 8. Signal Requirements of the [AD1856](#)

Figure 9 provides the specific timing requirements that must be met for the data transfer to be accomplished properly.

The input pins of the [AD1856](#) are both TTL and 5 V CMOS compatible, independent of the power supply voltages used.

The input requirements illustrated in Figure 8 and Figure 9 are compatible with the data outputs provided by popular DSP filter chips used in digital audio playback systems. The [AD1856](#) input clock can run at a 10 MHz rate. This clock rate allows data transfer rates for 2×, 4×, or 8× oversampling reconstruction. The Applications of the AD1856 PCM Audio DAC section provides additional guidelines for using the [AD1856](#) with various DSP filter chips.

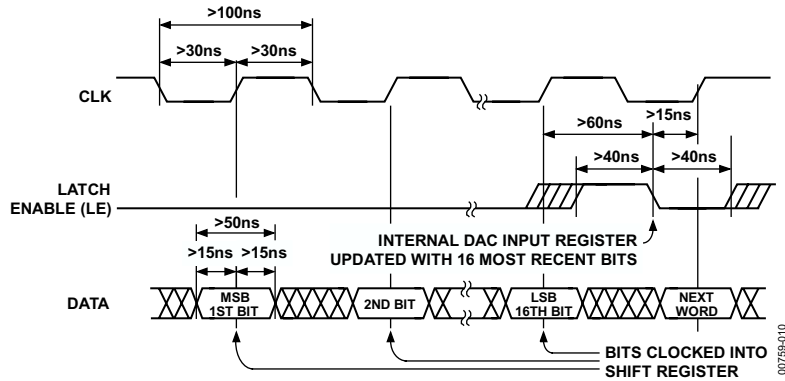


Figure 9. Timing Relationships of Input Signals

APPLICATIONS OF THE AD1856 PCM AUDIO DAC

The AD1856 is a versatile digital-to-analog converter designed for applications in consumer digital audio equipment. Portable, car, and home compact disc players, digital audio amplifiers, and DAT systems can all use the AD1856. Popular circuit architectures in these systems include stereo playback sections featuring one DAC per system, one DAC per audio channel (left/right), or even multiple DACs per channel. Furthermore, these architectures use different output reconstruction rates to accomplish these functions, including reproduction at the sample rate ($1 \times f_s$), at twice the sample rate ($2 \times f_s$), at four times the sample rate ($4 \times f_s$), and even at eight times the sample rate ($8 \times f_s$). For CD applications, f_s is 44.1 kHz; for DAT applications, f_s is 48 kHz.

ONE DAC PER SYSTEM

Figure 10 shows a circuit using one AD1856 per system to reproduce both stereo channels of a typical first-generation digital audio system. The input data is fed to the AD1856 in a format that alternates between left channel data and right channel data. The output of the AD1856 is switched between the left channel and right channel output sample-and-hold amplifiers (SHAs). The SHAs demultiplex and deglitch the output of the AD1856. The timing diagram for the control signals for this circuit is shown in Figure 11.

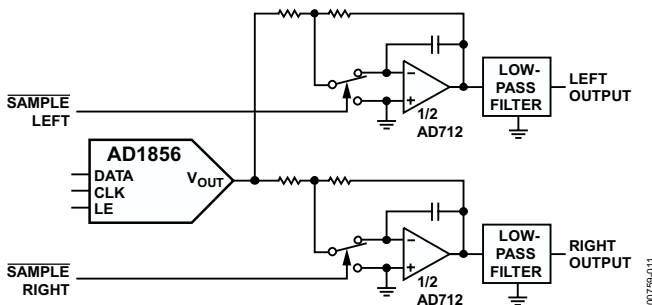


Figure 10. AD1856 in a One DAC per System Architecture

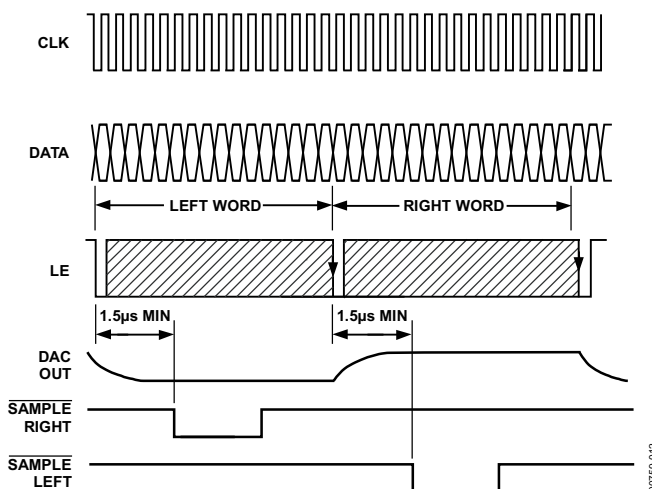


Figure 11. Control Signals for One DAC Circuit

The architecture illustrated in Figure 10 is suitable for low-end home or portable systems. However, its usefulness in mid-quality or high-quality digital audio reproduction is limited by the phase delay that is introduced in the multiplexed output. This phase delay is due to the fact that the information contained in the input bit stream represents left and right channel audio sampled simultaneously but reconstructed alternately. One solution to this problem is to incorporate a third, noninverting SHA to delay the output of one channel so that it can catch up to the other channel. This solution eliminates the phase shift by restoring simultaneous reproduction. This solution is illustrated in Figure 12.

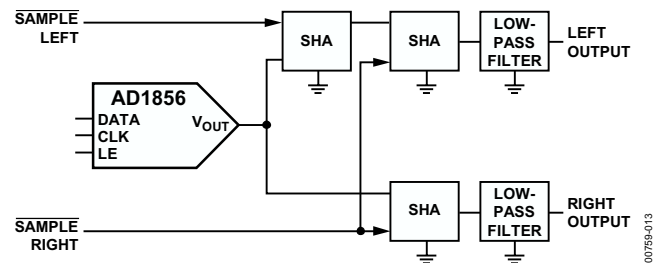


Figure 12. Third SHA Eliminates Phase Delay

ONE DAC PER CHANNEL

Another approach used to eliminate phase delay between left and right channels uses one DAC per channel. In this architecture, the input data bit streams for the left channel and the right channel are simultaneously sent and latched into each DAC. This second-generation approach, shown in Figure 13, is suitable for higher performance digital audio playback units.

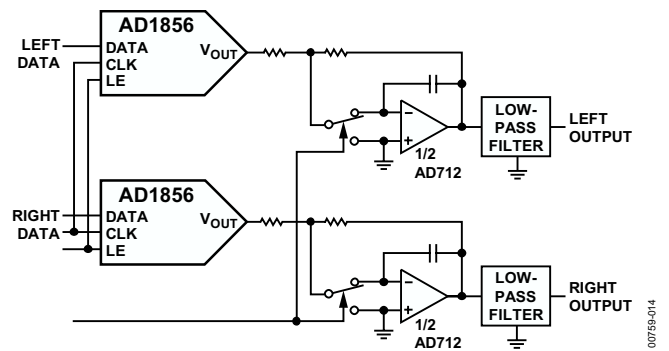


Figure 13. One DAC per Channel Architecture

TWO DACs PER CHANNEL (FOUR-DAC SYSTEM)

Another architecture uses two DACs per channel. In this scheme, shown in Figure 14, each DAC reproduces one half of the output waveform. The advantage obtained is that midscale differential linearity error no longer affects the zero-crossing points of the waveforms. These effects are shifted to the points where the output waveform crosses $\pm 3/4$ full scale. The result is that THD performance for low amplitude signals is greatly improved. Not shown in Figure 14 is a VLSI circuit, which is required to separate the incoming data into the appropriate form required by each DAC.

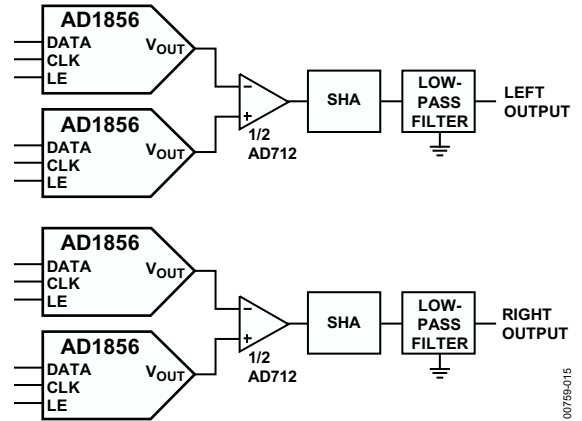


Figure 14. Two DACs per Channel Eliminate Midscale Distortion from the Zero-Crossing Points

007759-015

DIGITAL FILTERING AND OVERSAMPLING

Oversampling is a term that refers to playback techniques in which the reconstruction frequency used is an integral (2 or more) multiple of the original quantized data rate. For example, in compact disc stereo digital audio playback units, the original quantized data sample rate is 44.1 kHz. Popular oversampling rates are $2 \times f_s$ or $4 \times f_s$, yielding reconstruction rates of 88.2 kHz and 176.4 kHz, respectively.

Oversampling is used to ease the performance constraints of the low-pass filters that usually follow the reconstruction DAC. In any signal reconstructed from sampled data, undesired frequency components are introduced in the output spectrum; these components are centered at the reconstruction frequency.

When a 44.1 kHz reconstruction frequency is used, the actual frequency band of interest is 20 Hz to 20 kHz. However, a band of undesired image frequency components extends from approximately 24 kHz to 44.1 kHz; there is additional undesired component energy between 44.1 kHz and 64 kHz. These undesired components must be removed with a low-pass filter of very high order. First-generation digital audio systems often use low-pass filters of 9, 11, and even 13 poles. Linear implementations of these filters are expensive, difficult to manufacture, and can produce distortion due to varying group delay characteristics.

When a $2 \times$ reconstruction frequency (88.2 kHz) is used, the lowest undesired frequency components extend down to approximately 68 kHz. A $4 \times$ rate (176.4 kHz) has undesired components extending down to approximately 156 kHz. The filter response required to remove these frequency components can be less steep. This means that a lower order filter can be used, resulting in less distortion at lower cost. Linear filters with three or five poles are adequate and are quite common in digital audio products that use oversampling techniques.

Oversampling techniques require that the serial input data stream run at the same integral multiple of the original data rate. Therefore, although the constraints on the output low-pass filter are eased, the constraints on the serial digital input port and the settling time of the output stage are not.

The actual oversampling operation takes place in the digital filter chip, which is located upstream from the DAC. The digital filter accepts data from the media and adds the additional reconstruction points according to the algorithm and coefficients stored in the filter chip. Because the digital filters actually interpolate these additional reconstruction points, they are called interpolation filters.

ACHIEVING $8 \times f_s$ OVERSAMPLING WITH TWO AD1856 DEVICES AND THE YAMAHA YM3414

Figure 15 illustrates the combination of a Yamaha YM3414 digital filter chip and two AD1856 audio DACs. In this scheme, the use of a 16.9344 MHz clock allows an $8 \times$ oversampling rate for extremely high performance. In addition, a lower order low-pass filter can be used without sacrificing performance. The DAC input data is simultaneously transmitted to the input registers of the DACs through dedicated left and right channel output pins on the YM3414. Optional sample-and-hold signals are also provided.

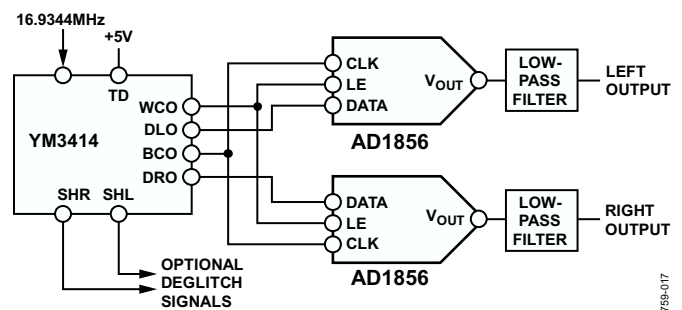
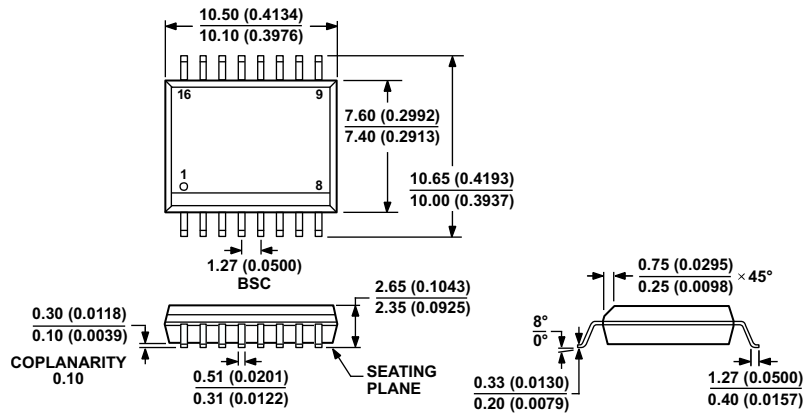


Figure 15. Yamaha YM3414 and AD1856 Interface

00759-017

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MS-013-AA
 CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS
 (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR
 REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure 16. 16-Lead Standard Small Outline Package [SOIC_W]
 Wide Body
 (RW-16)

Dimensions shown in millimeters and (inches)

03-27-2007-B

ORDERING GUIDE

| Model ¹ | Temperature Range | THD at Full-Scale Output | Package Description | Package Option |
|--------------------|-------------------|--------------------------|---------------------|----------------|
| AD1856RZ | -25°C to +70°C | 0.008% | 16-Lead SOIC_W | RW-16 |
| AD1856RZ-REEL | -25°C to +70°C | 0.008% | 16-Lead SOIC_W | RW-16 |
| AD1856RZ-REEL7 | -25°C to +70°C | 0.008% | 16-Lead SOIC_W | RW-16 |
| AD1856RZ-K | -25°C to +70°C | 0.0025% | 16-Lead SOIC_W | RW-16 |
| AD1856RZ-K-REEL7 | -25°C to +70°C | 0.0025% | 16-Lead SOIC_W | RW-16 |

¹ Z = RoHS Compliant Part.

NOTES



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