

AD5544/AD5554

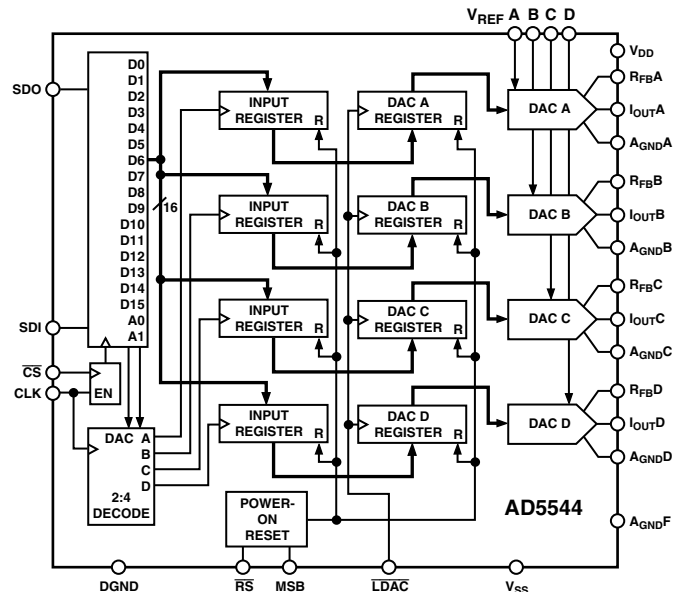
FEATURES

- AD5544 16-Bit Resolution**
- AD5554 14-Bit Resolution**
- 2 mA Full-Scale Current $\pm 20\%$, with $V_{REF} = \pm 10$ V**
- 2 μ s Settling Time**
- V_{SS} BIAS for Zero-Scale Error Reduction @ Temp**
- Midscale or Zero-Scale Reset**
- Four Separate 4Q Multiplying Reference Inputs**
- SPI-Compatible 3-Wire Interface**
- Double Buffered Registers Enable**
- Simultaneous Multichannel Change**
- Internal Power ON Reset**
- Compact SSOP-28 Package**

APPLICATIONS

- Automatic Test Equipment**
- Instrumentation**
- Digitally-Controlled Calibration**

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD5544/AD5554 quad, 16-/14-bit, current-output, digital-to-analog converters are designed to operate from a single 5 V supply.

The applied external reference input voltage (V_{REF}) determines the full-scale output current. Integrated feedback resistors (R_{FB}) provide temperature-tracking, full-scale voltage outputs when combined with an external I-to-V precision amplifier.

A doubled-buffered serial-data interface offers high-speed, 3-wire, SPI- and microcontroller-compatible inputs using serial-data-in (SDI), clock (CLK), and a chip-select (\overline{CS}). In addition, a serial-data-out pin (SDO) allows for daisy-chaining when multiple packages are used. A common level-sensitive load-DAC strobe (\overline{LDAC}) input allows simultaneous update of all DAC outputs from previously loaded input registers. Additionally, an internal power ON reset forces the output voltage to zero at system turn ON. An MSB pin allows system reset assertion (\overline{RS}) to force all registers to zero code when MSB = 0, or to half-scale code when MSB = 1.

AD5544/AD5554 are packaged in the compact SSOP-28.

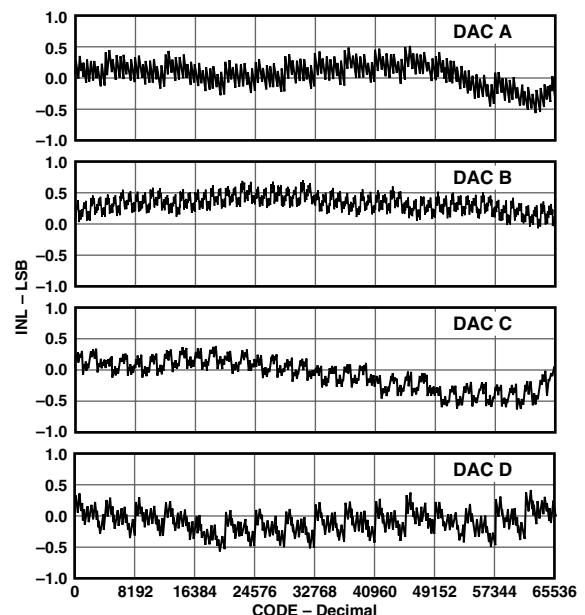


Figure 1. AD5544 INL vs. Code Plot ($T_A = 25^\circ\text{C}$)

REV. 0

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AD5544/AD5554—SPECIFICATIONS

(@ $V_{DD} = 5\text{ V} \pm 10\%$, $V_{SS} = 0\text{ V}$, $I_{OUTX} = \text{Virtual GND}$, $A_{GNDX} = 0\text{ V}$,
 $V_{REFA, B, C, D} = 10\text{ V}$, $T_A = \text{Full Operating Temperature Range}$,
 unless otherwise noted.)

| Parameter | Symbol | Condition | Min | Typ | Max | Unit |
|--|------------------------|--|------|------------|-----------|-----------------------|
| STATIC PERFORMANCE¹ | | | | | | |
| Resolution | N | 1 LSB = $V_{REF}/2^{16} = 153\ \mu\text{V}$ when $V_{REF} = 10\text{ V}$ | | | 16 | Bits |
| Relative Accuracy | INL | | | | ± 4 | LSB |
| Differential Nonlinearity | DNL | | | | ± 1.5 | LSB |
| Output Leakage Current | I_{OUTX} | Data = 0000 _H , $T_A = 25^\circ\text{C}$ | | | 10 | nA |
| | I_{OUTX} | Data = 0000 _H , $T_A = T_A \text{ Max}$ | | | 20 | nA |
| Full-Scale Gain Error | G_{FSE} | Data = FFFF _H | | ± 0.75 | ± 3 | mV |
| Full-Scale Tempco ² | TCV_{FS} | | | 1 | | ppm/ $^\circ\text{C}$ |
| Feedback Resistor | R_{FBX} | $V_{DD} = 5\text{ V}$ | 4 | 6 | 8 | k Ω |
| REFERENCE INPUT | | | | | | |
| V_{REFX} Range | V_{REFX} | | -15 | | +15 | V |
| Input Resistance | R_{REFX} | | 4 | 6 | 8 | k Ω |
| Input Resistance Match | R_{REFX} | Channel-to-Channel | | 1 | | % |
| Input Capacitance ² | C_{REFX} | | | 5 | | pF |
| ANALOG OUTPUT | | | | | | |
| Output Current | I_{OUTX} | Data = FFFF _H | 1.25 | | 2.5 | mA |
| Output Capacitance ² | C_{OUTX} | Code-Dependent | | 80 | | pF |
| LOGIC INPUTS AND OUTPUT | | | | | | |
| Logic Input Low Voltage | V_{IL} | | | | 0.8 | V |
| Logic Input High Voltage | V_{IH} | | 2.4 | | | V |
| Input Leakage Current | I_{IL} | | | | 1 | μA |
| Input Capacitance ² | C_{IL} | | | | 10 | pF |
| Logic Output Low Voltage | V_{OL} | $I_{OL} = 1.6\text{ mA}$ | | | 0.4 | V |
| Logic Output High Voltage | V_{OH} | $I_{OH} = 100\ \mu\text{A}$ | 4 | | | V |
| INTERFACE TIMING^{2, 3} | | | | | | |
| Clock Width High | t_{CH} | | 25 | | | ns |
| Clock Width Low | t_{CL} | | 25 | | | ns |
| \overline{CS} to Clock Setup | t_{CSS} | | 0 | | | ns |
| Clock to \overline{CS} Hold | t_{CSH} | | 25 | | | ns |
| Clock to SDO Prop Delay | t_{PD} | | 2 | | 20 | ns |
| Load DAC Pulsewidth | t_{LDAC} | | 25 | | | ns |
| Data Setup | t_{DS} | | 20 | | | ns |
| Data Hold | t_{DH} | | 20 | | | ns |
| Load Setup | t_{LDS} | | 5 | | | ns |
| Load Hold | t_{LDH} | | 25 | | | ns |
| SUPPLY CHARACTERISTICS | | | | | | |
| Power Supply Range | $V_{DD \text{ RANGE}}$ | | 4.5 | | 5.5 | V |
| Positive Supply Current | I_{DD} | Logic Inputs = 0 V | | 50 | 250 | μA |
| Negative Supply Current | I_{SS} | Logic Inputs = 0 V, $V_{SS} = -5\text{ V}$ | | 0.001 | 1 | μA |
| Power Dissipation | P_{DISS} | Logic Inputs = 0 V | | | 1.25 | mW |
| Power Supply Sensitivity | PSS | $\Delta V_{DD} = \pm 5\%$ | | | 0.006 | %/% |

NOTES

¹All static performance tests (except I_{OUT}) are performed in a closed-loop system using an external precision OP177 I-to-V converter amplifier. The AD5544 R_{FB} terminal is tied to the amplifier output. Typical values represent average readings measured at 25°C .

²These parameters are guaranteed by design and not subject to production testing.

³All input control signals are specified with $t_R = t_F = 2.5\text{ ns}$ (10% to 90% of 3 V) and timed from a voltage level of 1.5 V.

Specifications subject to change without notice.

(@ $V_{DD} = 5\text{ V} \pm 10\%$, $V_{SS} = -300\text{ mV}$, $I_{OUTX} = \text{Virtual GND}$, $A_{GNDX} = 0\text{ V}$,
 $V_{REFA}, B, C, D = 10\text{ V}$, $T_A = \text{full operating temperature range, unless otherwise noted.}$)

AD5544 ELECTRICAL CHARACTERISTICS

| Parameter | Symbol | Condition | Min | Typ | Max | Unit |
|---------------------------------------|---------------------|---|-----|-----|-----|------------------------------|
| AC CHARACTERISTICS¹ | | | | | | |
| Output Voltage Settling Time | t_S | To $\pm 0.1\%$ of Full Scale, Data = 0000 _H to FFFF _H to 0000 _H | | 1 | | μs |
| Output Voltage Settling Time | t_S | To $\pm 0.0015\%$ of Full Scale, Data = 0000 _H to FFFF _H to 0000 _H | | 2 | | μs |
| Reference Multiplying BW | BW -3 dB | $V_{REFX} = 100\text{ mV rms}$, Data = FFFF _H , $C_{FB} = 15\text{ pF}$ | | 2 | | MHz |
| DAC Glitch Impulse | Q | $V_{REFX} = 10\text{ V}$, Data 0000 _H to 8000 _H to 0000 _H | | 1.2 | | nV-s |
| Feedthrough Error | V_{OUTX}/V_{REFX} | Data = 0000 _H , $V_{REFX} = 100\text{ mV rms}$, $f = 100\text{ kHz}$ | | -65 | | dB |
| Crosstalk Error | V_{OUTA}/V_{REFB} | Data = 0000 _H , $V_{REFB} = 100\text{ mV rms}$, Adjacent Channel, $f = 100\text{ kHz}$ | | -90 | | dB |
| Digital Feedthrough | Q | $CS = 1$, and $f_{CLK} = 1\text{ MHz}$ | | 5 | | nV-s |
| Total Harmonic Distortion | THD | $V_{REF} = 5\text{ V p-p}$, Data = FFFF _H , $f = 1\text{ kHz}$ | | -90 | | dB |
| Output Spot Noise Voltage | e_N | $f = 1\text{ kHz}$, $BW = 1\text{ Hz}$ | | 7 | | $\text{nV}/\sqrt{\text{Hz}}$ |

NOTES

¹All ac characteristic tests are performed in a closed-loop system using an OP42 I-to-V converter amplifier.

Specifications subject to change without notice.

AD5544/AD5554—SPECIFICATIONS

AD5554 ELECTRICAL CHARACTERISTICS

(@ $V_{DD} = 5\text{ V} \pm 10\%$, $V_{SS} = 0\text{ V}$, $I_{OUTX} = \text{Virtual GND}$, $A_{GNDX} = 0\text{ V}$,
 $V_{REFA, B, C, D} = 10\text{ V}$, $T_A = \text{full operating temperature range}$,
 unless otherwise noted.)

| Parameter | Symbol | Condition | Min | Typ | Max | Unit |
|--|------------------------|--|------|---------|----------|-----------------------|
| STATIC PERFORMANCE¹ | | | | | | |
| Resolution | N | 1 LSB = $V_{REF}/2^{14} = 610\ \mu\text{V}$ when $V_{REF} = 10\text{ V}$ | | | 14 | Bits |
| Relative Accuracy | INL | | | | ± 1 | LSB |
| Differential Nonlinearity | DNL | | | | ± 1 | LSB |
| Output Leakage Current | I_{OUTX} | Data = 0000 _H , $T_A = 25^\circ\text{C}$ | | | 10 | nA |
| | I_{OUTX} | Data = 0000 _H , $T_A = T_A \text{ Max}$ | | | 20 | nA |
| Full-Scale Gain Error | G_{FSE} | Data = 3FFF _H | | ± 2 | ± 10 | mV |
| Full-Scale Tempco ² | TCV_{FS} | | | 1 | | ppm/ $^\circ\text{C}$ |
| Feedback Resistor | R_{FBX} | $V_{DD} = 5\text{ V}$ | 4 | 6 | 8 | k Ω |
| REFERENCE INPUT | | | | | | |
| V_{REFX} Range | V_{REFX} | | -15 | | +15 | V |
| Input Resistance | R_{REFX} | | 4 | 6 | 8 | k Ω |
| Input Resistance Match | R_{REFX} | Channel-to-Channel | | 1 | | % |
| Input Capacitance ² | C_{REFX} | | | 5 | | pF |
| ANALOG OUTPUT | | | | | | |
| Output Current | I_{OUTX} | Data = 3FFF _H | 1.25 | | 2.5 | mA |
| Output Capacitance ² | C_{OUTX} | Code-Dependent | | 80 | | pF |
| LOGIC INPUTS AND OUTPUT | | | | | | |
| Logic Input Low Voltage | V_{IL} | | | | 0.8 | V |
| Logic Input High Voltage | V_{IH} | | 2.4 | | | V |
| Input Leakage Current | I_{IL} | | | | 1 | μA |
| Input Capacitance ² | C_{IL} | | | | 10 | pF |
| Logic Output Low Voltage | V_{OL} | $I_{OL} = 1.6\text{ mA}$ | | | 0.4 | V |
| Logic Output High Voltage | V_{OH} | $I_{OH} = 100\ \mu\text{A}$ | 4 | | | V |
| INTERFACE TIMING^{2, 3} | | | | | | |
| Clock Width High | t_{CH} | | 25 | | | ns |
| Clock Width Low | t_{CL} | | 25 | | | ns |
| \overline{CS} to Clock Setup | t_{CSS} | | 0 | | | ns |
| Clock to \overline{CS} Hold | t_{CSH} | | 25 | | | ns |
| Clock to SDO Prop Delay | t_{PD} | | 2 | | 20 | ns |
| Load DAC Pulsewidth | t_{LDAC} | | 25 | | | ns |
| Data Setup | t_{DS} | | 20 | | | ns |
| Data Hold | t_{DH} | | 20 | | | ns |
| Load Setup | t_{LDS} | | 5 | | | ns |
| Load Hold | t_{LDH} | | 25 | | | ns |
| SUPPLY CHARACTERISTICS | | | | | | |
| Power Supply Range | $V_{DD \text{ RANGE}}$ | | 4.5 | | 5.5 | V |
| Positive Supply Current | I_{DD} | Logic Inputs = 0 V | | 50 | 250 | μA |
| Negative Supply Current | I_{SS} | Logic Inputs = 0 V, $V_{SS} = -5\text{ V}$ | | 0.001 | 1 | μA |
| Power Dissipation | P_{DISS} | Logic Inputs = 0 V | | | 1.25 | mW |
| Power Supply Sensitivity | PSS | $\Delta V_{DD} = \pm 5\%$ | | | 0.006 | %/% |

NOTES:

¹All static performance tests (except I_{OUT}) are performed in a closed-loop system using an external precision OP177 I-to-V converter amplifier. The AD5554 R_{FB} terminal is tied to the amplifier output. Typical values represent average readings measured at 25°C .

²These parameters are guaranteed by design and not subject to production testing.

³All input control signals are specified with $t_R = t_F = 2.5\text{ ns}$ (10% to 90% of 3 V) and timed from a voltage level of 1.5 V.

Specifications subject to change without notice.

(@ $V_{DD} = 5\text{ V} \pm 10\%$, $V_{SS} = -300\text{ mV}$, $I_{OUTX} = \text{Virtual GND}$, $A_{GNDX} = 0\text{ V}$, V_{REFA} ,
B, C, D = 10 V, $T_A = \text{full operating temperature range, unless otherwise noted.}$)

AD5554 ELECTRICAL CHARACTERISTICS

| Parameter | Symbol | Condition | Min Typ Max | Unit |
|---------------------------------------|---------------------|--|-------------|------------------------------|
| AC CHARACTERISTICS¹ | | | | |
| Output Voltage Settling Time | t_s | To $\pm 0.1\%$ of Full Scale, Data = 0000 _H to 3FFF _H to 0000 _H | 1 | μs |
| Output Voltage Settling Time | t_s | To $\pm 0.0015\%$ of Full Scale, Data = 0000 _H to 3FFF _H to 0000 _H | 2 | μs |
| Reference Multiplying BW | BW -3 dB | $V_{REFX} = 100\text{ mV rms}$, Data = 3FFF _H , $C_{FB} = 15\text{ pF}$ | 2 | MHz |
| DAC Glitch Impulse | Q | $V_{REFX} = 10\text{ V}$, Data 0000 _H to 2000 _H to 0000 _H | 1.2 | nV-s |
| Feedthrough Error | V_{OUTX}/V_{REFX} | Data = 0000 _H , $V_{REFX} = 100\text{ mV rms}$, $f = 100\text{ kHz}$ | -65 | dB |
| Crosstalk Error | V_{OUTA}/V_{REFB} | Data = 0000 _H , $V_{REFB} = 100\text{ mV rms}$, Adjacent Channel, $f = 100\text{ kHz}$ | -90 | dB |
| Digital Feedthrough | Q | $\overline{CS} = 1$, and $f_{CLK} = 1\text{ MHz}$ | 5 | nV-s |
| Total Harmonic Distortion | THD | $V_{REF} = 5\text{ V p-p}$, Data = 3FFF _H , $f = 1\text{ kHz}$ | -90 | dB |
| Output Spot Noise Voltage | e_N | $f = 1\text{ kHz}$, BW = 1 Hz | 7 | $\text{nV}/\sqrt{\text{Hz}}$ |

NOTES:

¹All ac characteristic tests are performed in a closed-loop system using an OP42 I-to-V converter amplifier.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

| | |
|--|---------------------------------------|
| V_{DD} to GND | -0.3 V, +8 V |
| V_{SS} to GND | +0.3 V, -7 V |
| V_{REF} to GND | -18 V, +18 V |
| Logic Inputs and Output to GND | -0.3 V, +8 V |
| $V(I_{OUT})$ to GND | -0.3 V, $V_{DD} + 0.3\text{ V}$ |
| A_{GNDX} to DGND | -0.3 V, +0.3 V |
| Input Current to Any Pin Except Supplies | $\pm 50\text{ mA}$ |
| Package Power Dissipation | $(T_J \text{ MAX} - T_A)/\theta_{JA}$ |
| Thermal Resistance θ_{JA} | |
| 28-Lead Shrink Surface-Mount (RS-28) | 100°C/W |
| Maximum Junction Temperature ($T_J \text{ MAX}$) | 150°C |

Operating Temperature Range

Model A -40°C to +85°C

Storage Temperature Range -65°C to +150°C

Lead Temperature:

RS-28 (Vapor Phase, 60 secs) 215°C

RS-28 (Infrared, 15 secs) 220°C

*Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ORDERING GUIDE

| Model | RES Bit | INL LSB | DNL LSB | Temperature Range | Package Description | Package Option |
|-----------|---------|---------|-----------|-------------------|---------------------|----------------|
| AD5544ARS | 16 | ± 4 | ± 1.5 | -40/+85°C | SSOP-28 | RS-28 |
| AD5554BRS | 14 | ± 1 | ± 1 | -40/+85°C | SSOP-28 | RS-28 |

The AD5544/AD5554 contain 4196 transistors. The die size is 122 mil \times 204 mil.

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD5544/AD5554 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high-energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



AD5544/AD5554

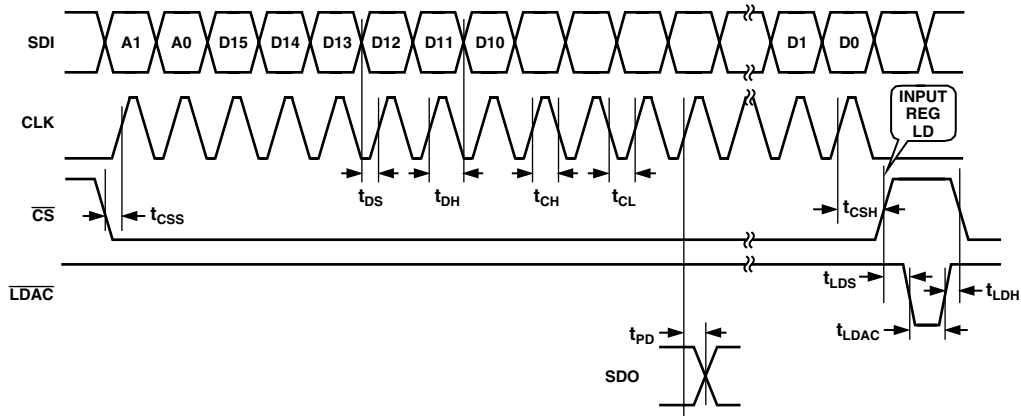


Figure 2. AD5544 Timing Diagram

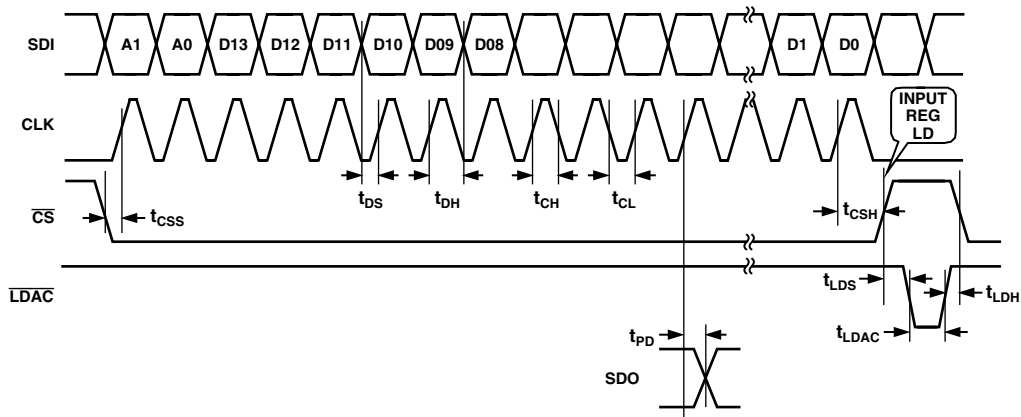


Figure 3. AD5554 Timing Diagram

Table I. AD5544 Control-Logic Truth Table

| \overline{CS} | CLK | \overline{LDAC} | \overline{RS} | MSB | Serial Shift Register Function | Input Register Function | DAC Register |
|-----------------|-------------|-------------------|-----------------|-----|--------------------------------------|---|----------------------------------|
| H | X | H | H | X | No Effect | Latched | Latched |
| L | L | H | H | X | No Effect | Latched | Latched |
| L | $\uparrow+$ | H | H | X | Shift-Register-Data Advanced One Bit | Latched | Latched |
| L | H | H | H | X | No Effect | Latched | Latched |
| $\uparrow+$ | L | H | H | X | No Effect | Selected DAC Updated with Current SR Contents | Latched |
| H | X | L | H | X | No Effect | Latched | Transparent |
| H | X | H | H | X | No Effect | Latched | Latched |
| H | X | $\uparrow+$ | H | X | No Effect | Latched | Latched |
| H | X | H | L | 0 | No Effect | Latched Data = 0000 _H | Latched Data = 0000 _H |
| H | X | H | L | H | No Effect | Latched Data = 8000 _H | Latched Data = 8000 _H |

Table II. AD5554 Control-Logic Truth Table

| \overline{CS} | CLK | \overline{LDAC} | \overline{RS} | MSB | Serial Shift Register Function | Input Register Function | DAC Register |
|-----------------|-------------|-------------------|-----------------|-----|--------------------------------------|---|----------------------------------|
| H | X | H | H | X | No Effect | Latched | Latched |
| L | L | H | H | X | No Effect | Latched | Latched |
| L | $\uparrow+$ | H | H | X | Shift-Register-Data Advanced One Bit | Latched | Latched |
| L | H | H | H | X | No Effect | Latched | Latched |
| $\uparrow+$ | L | H | H | X | No Effect | Selected DAC Updated with Current SR Contents | Latched |
| H | X | L | H | X | No Effect | Latched | Transparent |
| H | X | H | H | X | No Effect | Latched | Latched |
| H | X | $\uparrow+$ | H | X | No Effect | Latched | Latched |
| H | X | H | L | 0 | No Effect | Latched Data = 0000 _H | Latched Data = 0000 _H |
| H | X | H | L | H | No Effect | Latched Data = 2000 _H | Latched Data = 2000 _H |

NOTES

1. SR = Shift Register.
2. $\uparrow+$ positive logic transition; X = Don't Care.
3. At power ON both the Input Register and the DAC Register are loaded with all zeros.
4. For AD5544, data appears at the SDO Pin 19 clock pulses after input at the SDI pin.
5. For AD5554, data appears at the SDO Pin 17 clock pulses after input at the SDI pin.

Table III. AD5544 Serial Input Register Data Format, Data Is Loaded in the MSB-First Format

| | MSB | | | | | | | | | | | | | | | | | LSB |
|--------------|-----|-----|-----|-----|-----|-----|-----|-----|----|----|----|----|----|----|----|----|----|-----|
| Bit Position | B17 | B16 | B15 | B14 | B13 | B12 | B11 | B10 | B9 | B8 | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
| Data Word | A1 | A0 | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |

NOTE

Only the last 18 bits of data clocked into the serial register (Address + Data) are inspected when the \overline{CS} line's positive edge returns to logic high. At this point an internally generated load strobe transfers the serial register data contents (Bits D15–D0) to the decoded DAC-Input-Register address determined by bits A1 and A0. Any extra bits clocked into the AD5544 shift register are ignored, only the last 18 bits clocked in are used. If double-buffered data is not needed, the \overline{LDAC} pin can be tied logic low to disable the DAC Registers.

Table IV. AD5554 Serial Input Register Data Format, Data Is Loaded in the MSB-First Format

| | MSB | | | | | | | | | | | | | | | | LSB |
|--------------|-----|-----|-----|-----|-----|-----|----|----|----|----|----|----|----|----|----|----|-----|
| Bit Position | B15 | B14 | B13 | B12 | B11 | B10 | B9 | B8 | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 | |
| Data Word | A1 | A0 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | |

NOTE

Only the last 16 bits of data clocked into the serial register (Address + Data) are inspected when the \overline{CS} line's positive edge returns to logic high. At this point an internally generated load strobe transfers the serial register data contents (Bits D13–D0) to the decoded DAC-Input-Register address determined by bits A1 and A0. Any extra bits clocked into the AD5554 shift register are ignored, only the last 16 bits clocked in are used. If double-buffered data is not needed, the \overline{LDAC} pin can be tied logic low to disable the DAC Registers.

Table V. Address Decode

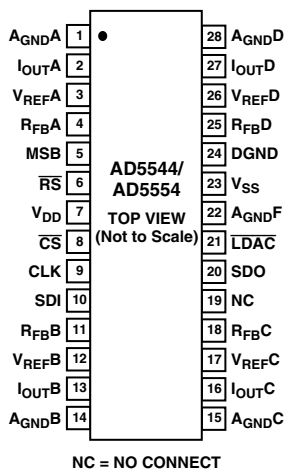
| A1 | A0 | DAC Decoded |
|----|----|-------------|
| 0 | 0 | DAC A |
| 0 | 1 | DAC B |
| 1 | 0 | DAC C |
| 1 | 1 | DAC D |

AD5544/AD5554

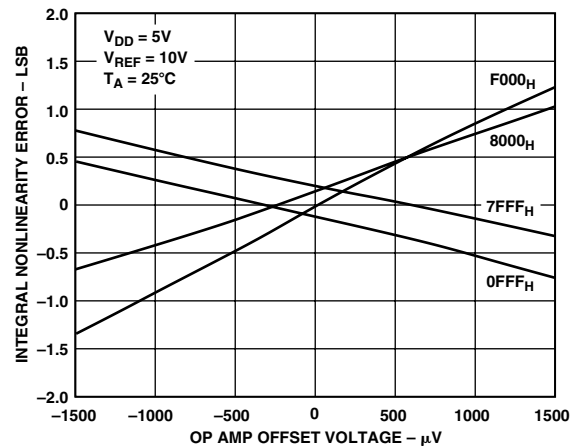
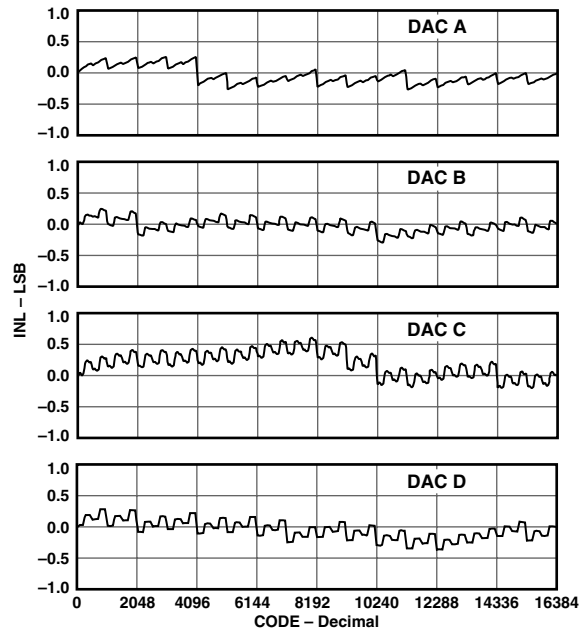
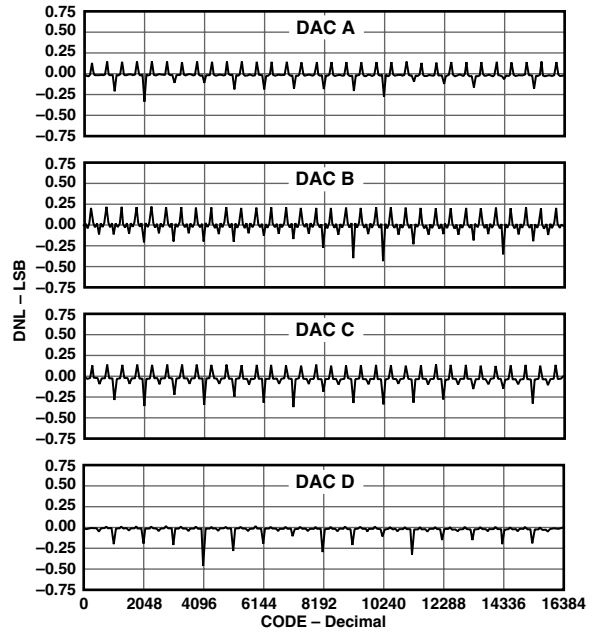
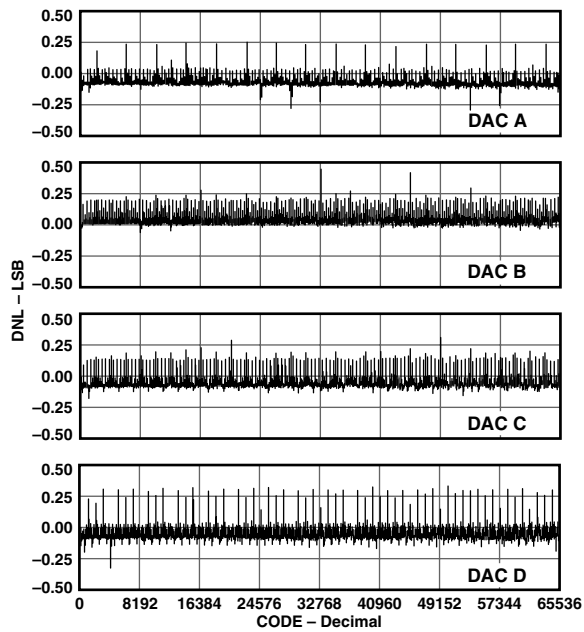
AD5544/AD5554 PIN FUNCTION DESCRIPTIONS

| Pin # | Name | Function |
|-------|-------------------|--|
| 1 | AGNDA | DAC A Analog Ground. |
| 2 | IOUTA | DAC A Current Output. |
| 3 | VREFA | DAC A Reference Voltage Input Terminal. Establishes DAC A full-scale output voltage. Pin can be tied to V _{DD} pin. |
| 4 | RFB A | Establish Voltage Output for DAC A by Connecting to External Amplifier Output. |
| 5 | MSB | MSB Bit Set Pin During a Reset Pulse (\overline{RS}) or at System Power ON if Tied to Ground or V _{DD} . |
| 6 | \overline{RS} | Reset Pin, Active Low Input. Input registers and DAC registers are set to all zeros or half-scale code (8000 _H for AD5544 and 2000 _H for AD5554) determined by the voltage on the MSB pin. Register Data = 0000 _H when MSB = 0. Register Data = 8000 _H for AD5544 and 2000 _H for AD5554 when MSB = 1. |
| 7 | V _{DD} | Positive Power Supply Input. Specified range of operation 5 V ± 10%. |
| 8 | \overline{CS} | Chip Select, Active Low Input. Disables shift register loading when high. Transfers serial register data to the Input Register when $\overline{CS}/\overline{LDAC}$ returns High. Does not effect \overline{LDAC} operation. |
| 9 | CLK | Clock Input, Positive Edge Clocks Data into Shift Register. |
| 10 | SDI | Serial Data Input, Input Data Loads Directly into the Shift Register. |
| 11 | RFB B | Establish Voltage Output for DAC B by Connecting to External Amplifier Output. |
| 12 | VREFB | DAC B Reference Voltage Input Terminal. Establishes DAC B full-scale output voltage. Pin can be tied to V _{DD} pin. |
| 13 | IOUTB | DAC B Current Output. |
| 14 | AGNDB | DAC B Analog Ground. |
| 15 | AGNDC | DAC C Analog Ground. |
| 16 | IOUTC | DAC C Current Output. |
| 17 | VREFC | DAC C Reference Voltage Input Terminal. Establishes DAC C full-scale output voltage. Pin can be tied to V _{DD} pin. |
| 18 | RFB C | Establish voltage output for DAC C by connecting to external amplifier output. |
| 19 | NC | No Connect. Leave pin unconnected. |
| 20 | SDO | Serial Data Output, input data loads directly into the shift register. Data appears at SDO, 19 clock pulses for AD5544 and 17 clock pulses for AD5554 after input at the SDI pin. |
| 21 | \overline{LDAC} | Load DAC Register Strobe, Level Sensitive Active Low. Transfers all Input Register data to DAC registers. Asynchronous active low input. See Control Logic Truth Table for operation. |
| 22 | AGNDF | High Current Analog Force Ground. |
| 23 | V _{SS} | Negative Bias Power Supply Input. Specified range of operation -0.3 V to -5.5 V. |
| 24 | DGND | Digital Ground Pin. |
| 25 | RFB D | Establish Voltage Output for DAC D by Connecting to External Amplifier Output. |
| 26 | VREFD | DAC D Reference Voltage Input Terminal. Establishes DAC D full-scale output voltage. Pin can be tied to V _{DD} pin. |
| 27 | IOUTD | DAC D Current Output. |
| 28 | AGNDD | DAC D Analog Ground. |

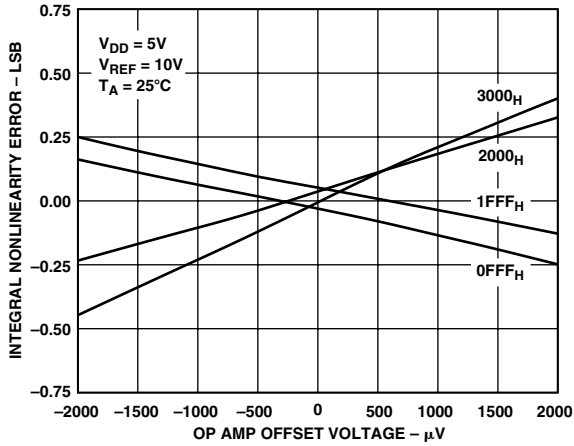
AD5544/AD5554 PIN CONFIGURATION



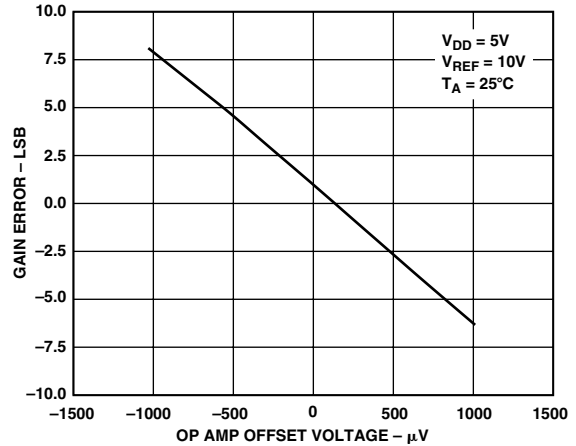
Typical Performance Characteristics—AD5544/AD5554



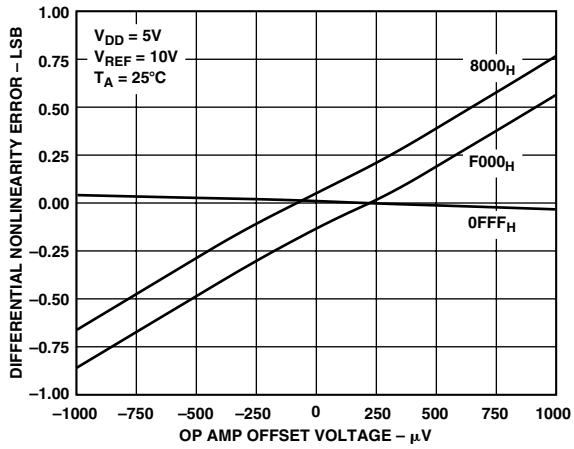
AD5544/AD5554



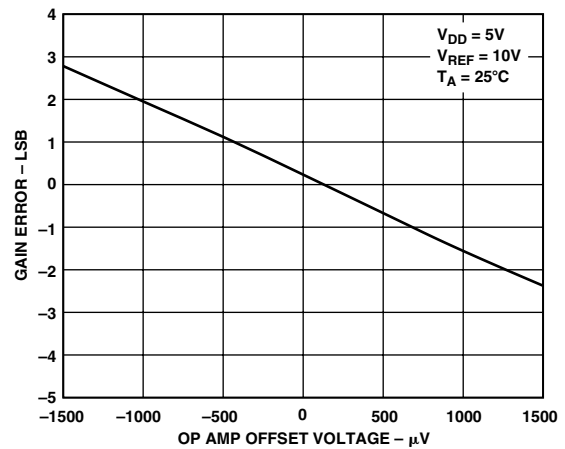
TPC 5. AD5544 Integral Nonlinearity Error vs. Op Amp Offset



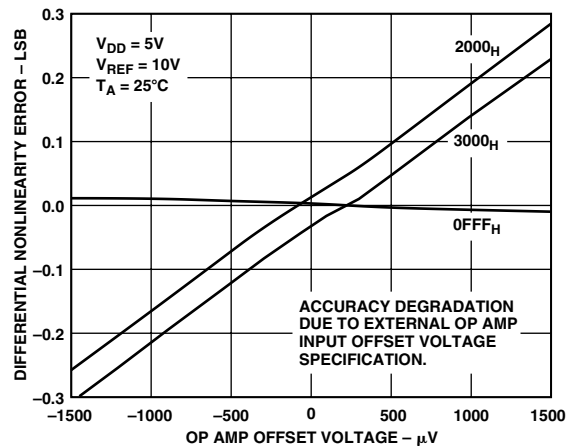
TPC 8. AD5544 Gain Error vs. Op Amp Offset



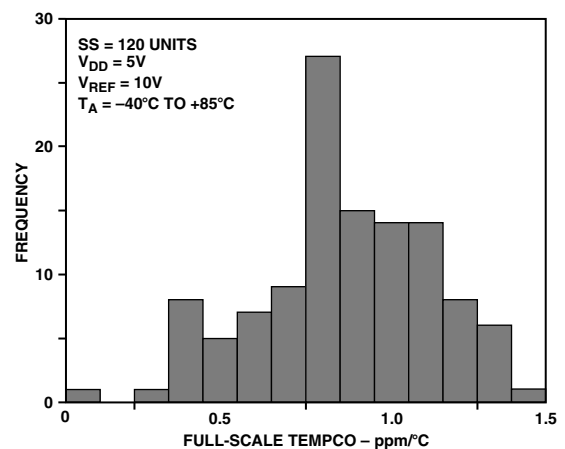
TPC 6. AD5544 Differential Nonlinearity Error vs. Op Amp Offset



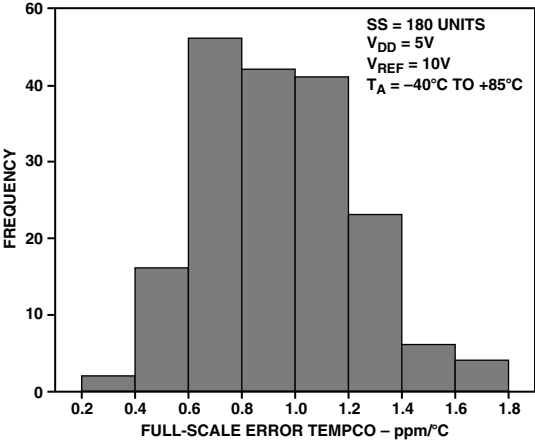
TPC 9. AD5554 Gain Error vs. Op Amp Offset



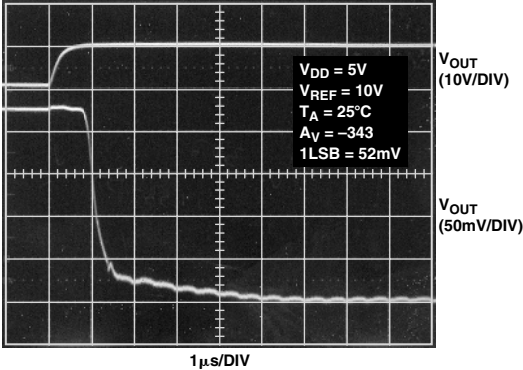
TPC 7. AD5554 Differential Nonlinearity Error vs. Op Amp Offset



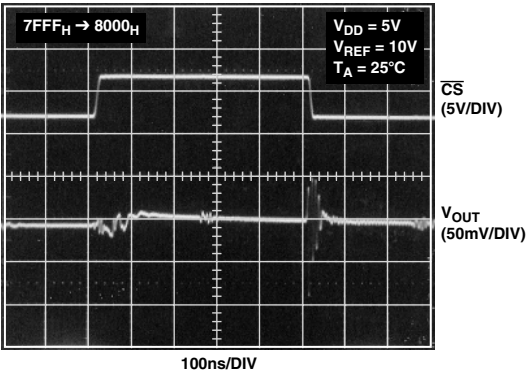
TPC 10. AD5544 Full-Scale Tempco (ppm/°C)



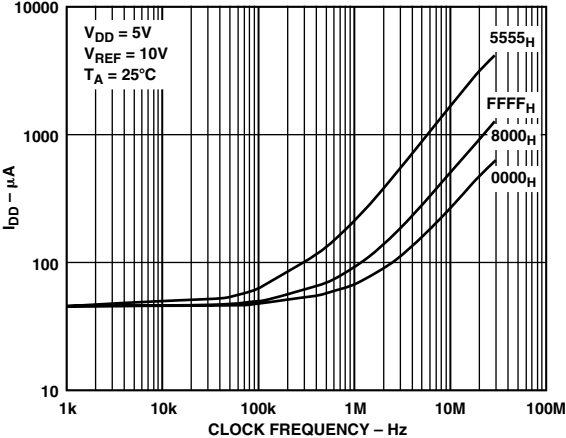
TPC 11. AD5544 Full-Scale Tempco (ppm/°C)



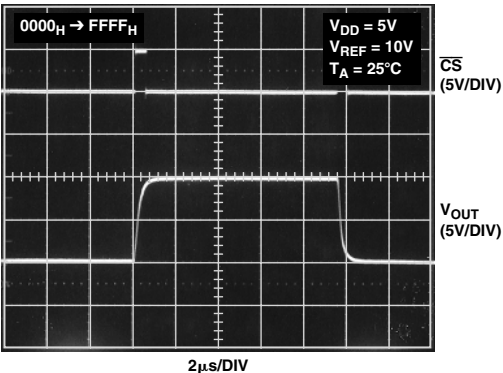
TPC 14. AD5544 Small Signal Settling Time



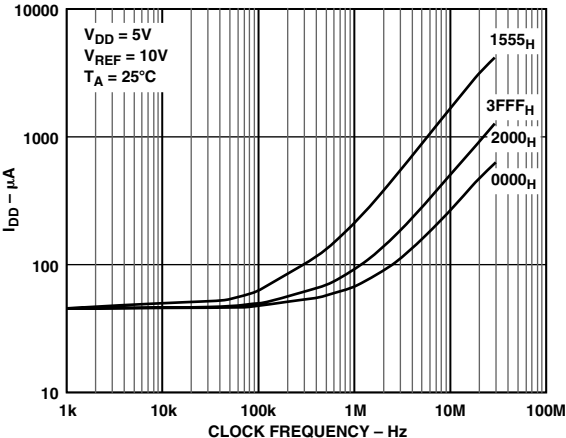
TPC 12. AD5544 Midscale Transition



TPC 15. AD5544 Power Supply Current vs. Clock Frequency

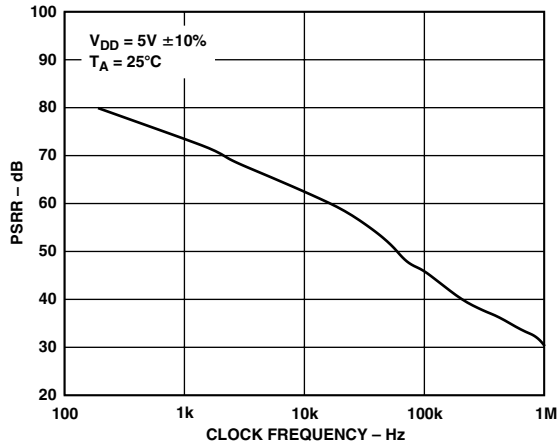


TPC 13. AD5544 Large Signal Settling Time

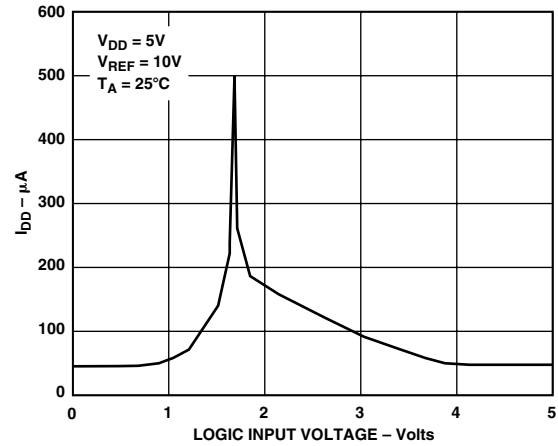


TPC 16. AD5544 Power Supply Current vs. Clock Frequency

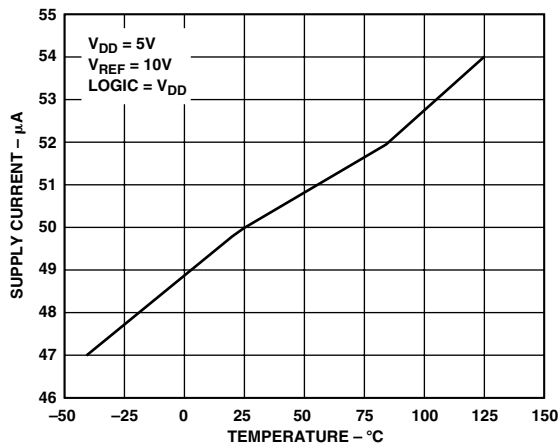
AD5544/AD5554



TPC 17. AD5544/AD5554 Power Supply Rejection vs. Frequency



TPC 19. AD5544/AD5554 Power Supply Current vs. Logic Input Voltage



TPC 18. AD5544/AD5554 Power Supply Current vs. Temperature

CIRCUIT OPERATION

The AD5544 and AD5554 contain four, 16-bit and 14-bit, current-output, digital-to-analog converters respectively. Each DAC has its own independent multiplying reference input. Both AD5544/AD5554 use 3-wire SPI compatible serial data interface, with a configurable asynchronous $\overline{\text{RS}}$ pin for half-scale ($\text{MSB} = 1$) or zero-scale ($\text{MSB} = 0$) preset. In addition, an $\overline{\text{LDAC}}$ strobe enables four channel simultaneous updates for hardware synchronized output voltage changes.

D/A Converter Section

Each part contains four current-steering R-2R ladder DACs. Figure 4 shows a typical equivalent DAC. Each DAC contains a matching feedback resistor for use with an external I-to-V converter amplifier. The R_{FBX} pin is connected to the output of the external amplifier. The I_{OUTX} terminal is connected to the inverting input of the external amplifier. The AGNDX pin should be Kelvin-connected to the load point in the circuit requiring the full 16-bit accuracy. These DACs are designed to operate

with both negative or positive reference voltages. The V_{DD} power pin is only used by the logic to drive the DAC switches ON and OFF. Note that a matching switch is used in series with the internal $5\text{ k}\Omega$ feedback resistor. If users are attempting to measure the value of R_{FB} , power must be applied to V_{DD} in order to achieve continuity. An additional V_{SS} bias pin is used to guard the substrate during high temperature applications to minimize zero-scale leakage currents that double every 10°C . The DAC output voltage is determined by V_{REF} and the digital data (D) as:

$$V_{\text{OUT}} = -V_{\text{REF}} \times \frac{\text{D}}{65536} \quad (\text{For AD5544}) \quad (\text{Equation 1})$$

$$V_{\text{OUT}} = -V_{\text{REF}} \times \frac{\text{D}}{16384} \quad (\text{For AD5554}) \quad (\text{Equation 2})$$

Note that the output polarity is opposite to the V_{REF} polarity for dc reference voltages.

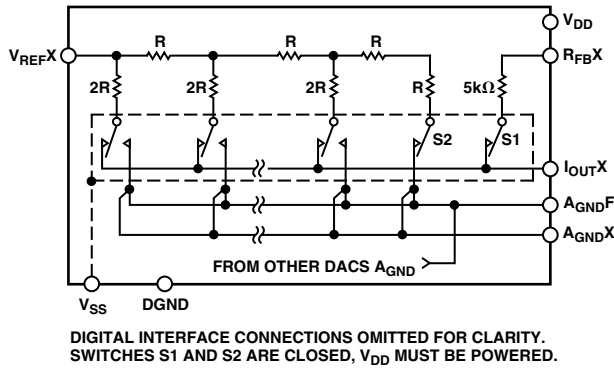


Figure 4. Typical Equivalent DAC Channel

These DACs are also designed to accommodate ac reference input signals. Both AD5544/AD5554 will accommodate input reference voltages in the range of -12 V to $+12\text{ V}$. The reference voltage inputs exhibit a constant nominal input resistance of $5\text{ k}\Omega$, $\pm 30\%$. On the other hand, the DAC outputs I_{OUTA} , B, C, D are code-dependent and produce various output resistances and capacitances. The choice of external amplifier should take into account the variation in impedance generated by the AD5544/AD5554 on the amplifiers' inverting input node. The feedback resistance, in parallel with the DAC ladder resistance, dominates output voltage noise. For multiplying mode applications, an external feedback compensation capacitor (C_{FB}) may be needed to provide a critically damped output response for step changes in reference input voltages. Figures 5 and 6 show the gain vs. frequency performance at various attenuation settings using a 23 pF external feedback capacitor connected across the I_{OUTX} and R_{FBX} terminals for AD5544 and AD5554 respectively. In order to maintain good analog performance, power supply bypassing of $0.01\text{ }\mu\text{F}$, in parallel with $1\text{ }\mu\text{F}$, is recommended. Under these conditions, clean power supply with low ripple voltage capability should be used. Switching power supplies is usually not suitable for this application due to the higher ripple voltage and PSS frequency-dependent characteristics. It is best to derive the AD5544/AD5554's 5 V supply from the systems' analog supply voltages. (Do not use the digital 5 V supply.) See Figure 7.

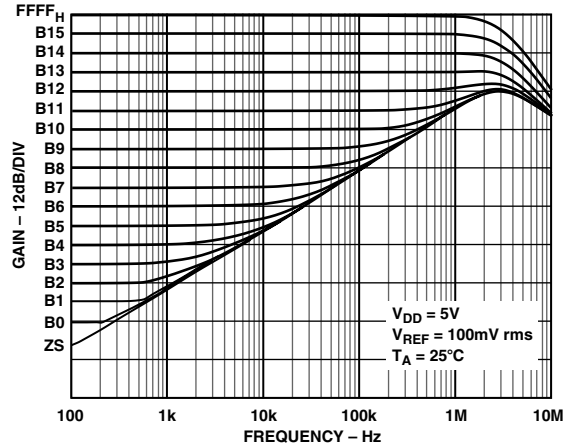


Figure 5. AD5544 Reference Multiplying Bandwidth vs. Code

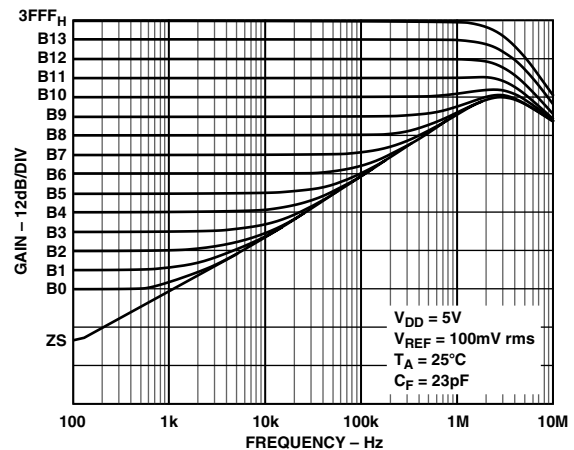


Figure 6. AD5554 Reference Multiplying Bandwidth vs. Code

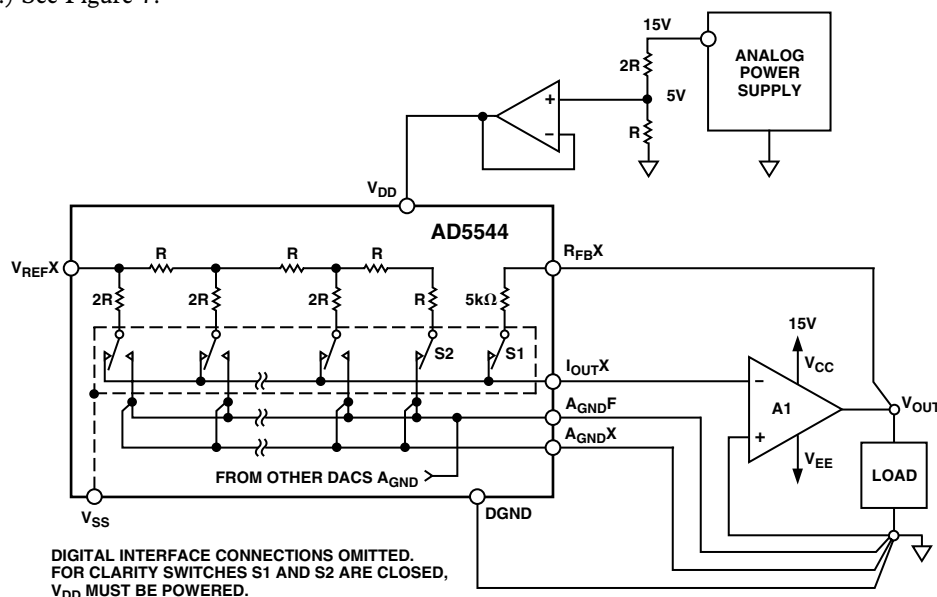


Figure 7. Recommended Kelvin-Sensed Hookup

AD5544/AD5554

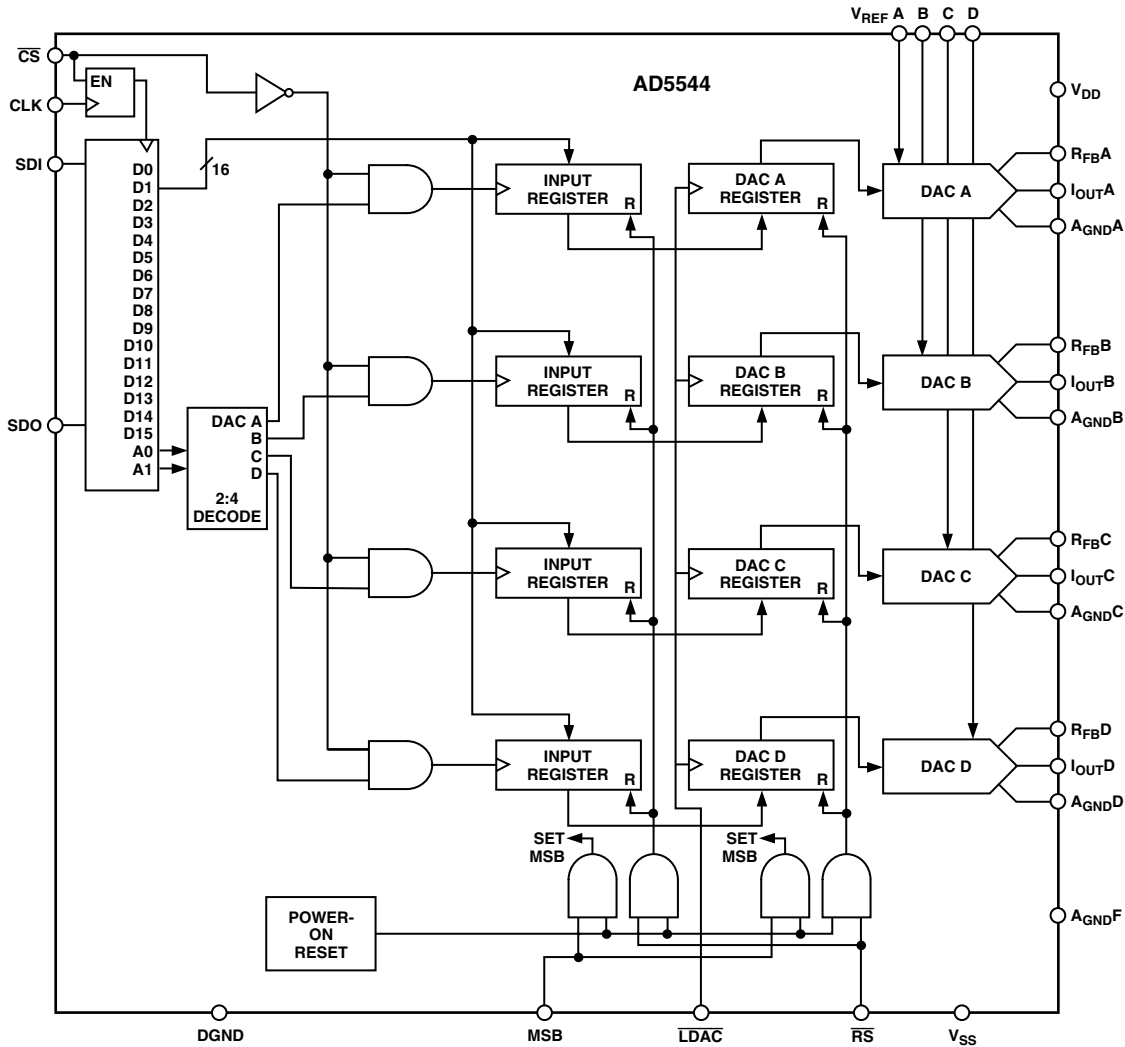


Figure 8. System Level Digital Interfacing

SERIAL DATA INTERFACE

The AD5544/AD5554 uses a 3-wire (\overline{CS} , SDI, CLK) SPI compatible serial data interface. Serial data of AD5544 and AD5554 is clocked into the serial input register in an 18-bit and 16-bit data-word format respectively. MSB bits are loaded first. Table II defines the 18 data-word bits for AD5544. Table III defines the 16 data-word bits for AD5554. Data is placed on the SDI pin, and clocked into the register on the positive clock edge of CLK subject to the data setup and data hold time requirements specified in the Interface Timing Specifications. Data can only be clocked in while the \overline{CS} chip select pin is active low. For AD5544, only the last 18 bits clocked into the serial register will be interrogated when the \overline{CS} pin returns to the logic high state, extra data bits are ignored. For AD5554, only the last 16 bits clocked into the serial register will be interrogated when the \overline{CS} pin returns to the logic high state. Since most microcontrollers output serial data in 8-bit bytes, three right-justified data bytes can be written to the AD5544. Keeping the \overline{CS} line low between the first, second, and third byte transfers will result in a successful serial register update. Similarly, two right-justified data bytes

can be written to the AD5554. Keeping the \overline{CS} line low between the first and second byte transfer will result in a successful serial register update.

Once the data is properly aligned in the shift register, the positive edge of the \overline{CS} initiates the transfer of new data to the target DAC register, determined by the decoding of address bits A1 and A0. For AD5544, Tables I, III, V, and Figure 2 define the characteristics of the software serial interface. For AD5554, Tables II, IV, V, and Figure 3 define the characteristics of the software serial interface. Figures 8 and 9 show the equivalent logic interface for the key digital control pins for AD5544. AD5554 has similar configuration, except with 14 data bits.

Two additional pins \overline{RS} and MSB provide hardware control over the preset function and DAC Register loading. If these functions are not needed, the \overline{RS} pin can be tied to logic high. The asynchronous input \overline{RS} pin forces all input and DAC registers to either the zero-code state (MSB = 0), or the half-scale state (MSB = 1)

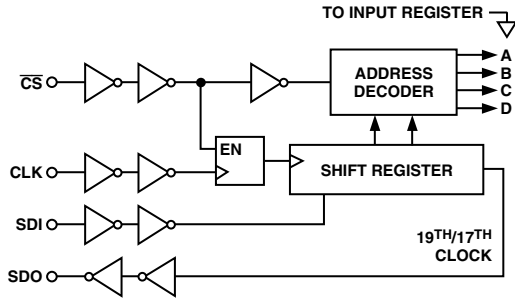


Figure 9. AD5544/AD5554 Equivalent Logic Interface

POWER-ON RESET

When the V_{DD} power supply is turned ON, an internal reset strobe forces all the Input and DAC registers to the zero-code state or half-scale, depending on the MSB pin voltage. The V_{DD} power supply should have a smooth positive ramp without drooping in order to have consistent results, especially in the region of $V_{DD} = 1.5\text{ V}$ to 2.3 V . The V_{SS} supply has no effect on the power-ON reset performance. The DAC register data will stay at zero or half-scale setting until a valid serial register data load takes place.

ESD Protection Circuits

All logic-input pins contain back-biased ESD protection Zeners connected to ground (DGND) and V_{DD} as shown in Figure 9.

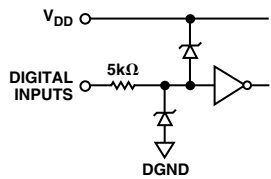


Figure 10. Equivalent ESD Protection Circuits

PCB LAYOUT

In PCB layout, all analog ground, A_{GNDX} , should be tied together. Amplifiers suitable for I-to-V conversion include:

- High Accuracy: OP97, OP297
- Speed and Accuracy: OP42
- $\pm 5\text{ V}$ Applications: OP162/OP262/OP462, OP184/OP284/OP484

APPLICATIONS

The AD5544/AD5554 are inherently 2-quadrant multiplying D/A converters. That is, they can be easily set up for unipolar output operation. The full-scale output polarity is the inverse of the reference-input voltage.

In some applications it may be necessary to generate the full 4-quadrant multiplying capability or a bipolar output swing. This is easily accomplished using an additional external amplifier (A2) configured as a summing amplifier (see Figure 11). In this circuit the first and second amplifiers (A1 and A2) provide a total gain-of-2 which increases the output voltage span to 20 V. Biasing the external amplifier with a 10 V offset from the reference voltage results in a full 4-quadrant multiplying circuit. The transfer equation of this circuit shows that both negative and positive output voltages are created as the input data (D) is incremented from code zero ($V_{OUT} = -10\text{ V}$) to midscale ($V_{OUT} = 0\text{ V}$) to full-scale ($V_{OUT} = 10\text{ V}$).

$$V_{OUT} = \left(\frac{D}{32768} - 1 \right) \times V_{REF} \quad (\text{For AD5544}) \quad (\text{Equation 3})$$

$$V_{OUT} = \left(\frac{D}{8192} - 1 \right) \times V_{REF} \quad (\text{For AD5554}) \quad (\text{Equation 4})$$

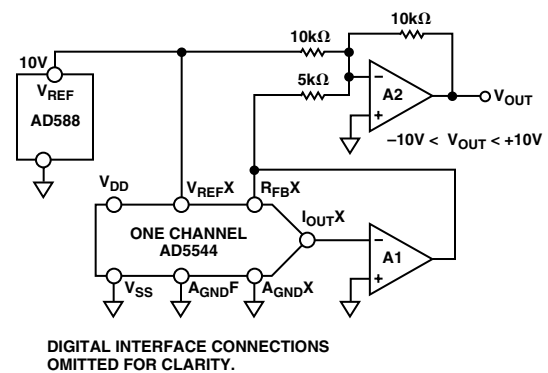


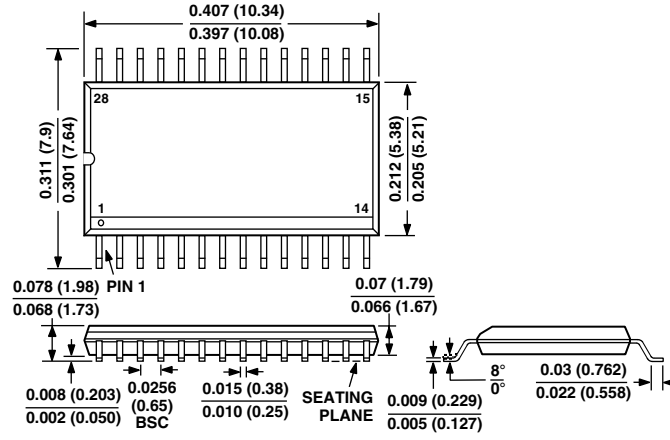
Figure 11. Four-Quadrant Multiplying Application Circuit

AD5544/AD5554

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

28-Lead SSOP (RS-28)



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