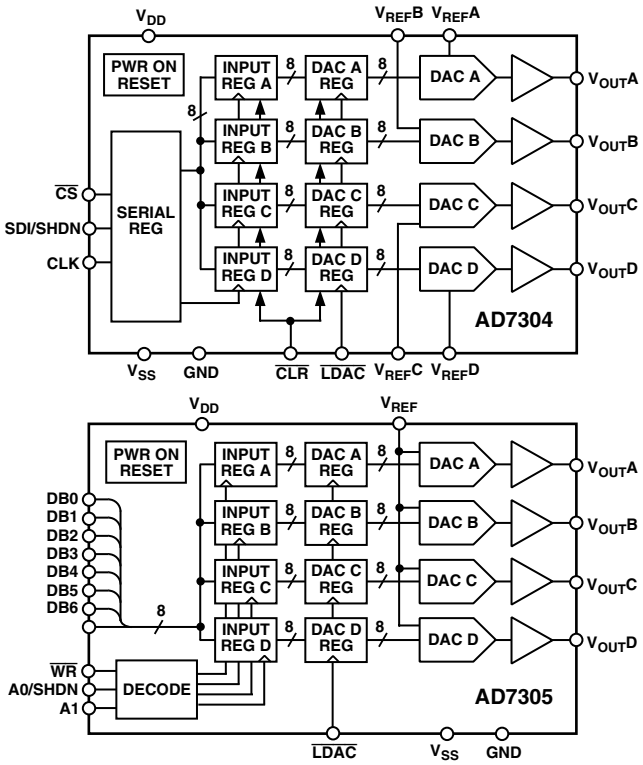
+3 V/+5 V, Rail-to-Rail Quad, 8-Bit DAC

AD7304/AD7305*

FEATURES
Four 8-Bit DACs in One Package
+3 V, +5 V and ±5 V Operation
Rail-to-Rail REF-Input to Voltage Output Swing
2.6 MHz Reference Multiplying Bandwidth
Compact 1.1 mm Height TSSOP 16-/20-Lead Package
Internal Power ON Reset
SPI Serial Interface Compatible—AD7304
Fast Parallel Interface—AD7305
40 μA Power Shutdown

APPLICATIONS
Automotive Output Span Voltage
Instrumentation, Digitally Controlled Calibration
Pin-Compatible AD7226 Replacement when V_{DD} < 5.5 V

FUNCTIONAL BLOCK DIAGRAMS



GENERAL DESCRIPTION

The AD7304/AD7305 are quad, 8-bit DACs that operate from a single +3 V to +5 V supply or ±5 V supplies. The AD7304 has a serial interface, while the AD7305 has a parallel interface. Internal precision buffers swing rail-to-rail. The reference input range includes both supply rails allowing for positive or negative full-scale output voltages. Operation is guaranteed over the supply voltage range of +2.7 V to +5.5 V, consuming less than 9 mW from a +3 V supply.

The full-scale voltage output is determined by the external reference input voltage applied. The rail-to-rail V_{REF} input to DAC V_{OUT} allows for a full-scale voltage set equal the positive supply V_{DD}, the negative supply V_{SS} or any value in between.

The AD7304's doubled-buffered serial-data interface offers high speed, three-wire, SPI and microcontroller compatible inputs using data in (SDI), clock (CLK) and chip select ($\overline{CS}$) pins. Additionally, an internal power-on reset sets the output to zero scale.

The parallel input AD7305 uses a standard address decode along with the $\overline{WR}$ control line to load data into the input registers. The double buffered architecture allows all four input registers to be preloaded with new values, followed by a $\overline{LDAC}$ control strobe which copies all the new data into the DAC registers thereby updating the analog output values. When operating from less than +5.5 V, the AD7305 is pin-compatible with the popular industry standard AD7226.

An internal power ON reset places both parts in the zero-scale state at turn ON. A 40 μA power shutdown (SHDN) feature is activated on both parts by tristating the SDI/SHDN pin on the AD7304, and tristating the A0/SHDN address pin on the AD7305.

The AD7304/AD7305 are specified over the extended industrial (–40°C to +85°C), and the automotive (–40°C to +125°C) temperature ranges. AD7304s are available in 16-lead plastic DIP (N-16), and wide-body SOL-16 (R-16) packages. The parallel input AD7305 is available in the 20-lead plastic DIP (N-20), and the SOL-20 (R-20) surface mount package. For ultracompact applications the thin 1.1 mm TSSOP-16 (RU-16) package will be available for the AD7304, while the TSSOP-20 (RU-20) will house the AD7305.

*Protected under Patent Number 5684481.

REV. A

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AD7304/AD7305–SPECIFICATIONS (@ V_{DD} = +3 V or +5 V, V_{SS} = 0 V; or V_{DD} = +5 V and V_{SS} = –5 V, $V_{SS} \le V_{REF} \le V_{DD}$, –40°C < T_A < +85°C/+125°C, unless otherwise noted.)

Parameter	Symbol	Condition	3 V ± 10%	5 V ± 10%	±5 V ± 10%	Units
STATIC PERFORMANCE						
Resolution[1]	N		8	8	8	Bits
Integral Nonlinearity[2]	INL		±1	±1	±1	LSB max
Differential Nonlinearity	DNL	Monotonic, All Codes 0 to FF_H	±1	±1	±1	LSB max
Zero-Scale Error	V_{ZSE}	Data = 00_H	15	15	±15	mV max
Full-Scale Voltage Error	V_{FSE}	Data = FF_H	±4	±4	±4	LSB max
Full-Scale Tempco[3]	TCV_{FS}		5	5	5	ppm/°C typ[4]
REFERENCE INPUT						
V_{REFIN} Range	V_{REFIN}		V_{SS}/V_{DD}	V_{SS}/V_{DD}	V_{SS}/V_{DD}	V min/max
Input Resistance (AD7304)	R_{REFIN}	Code = 55_H	28	28	28	kΩ typ
Input Resistance (AD7305)	R_{REFIN}	All DACs at Code = 55_H	7.5	7.5	7.5	kΩ typ
Input Capacitance[3]	C_{REFIN}		5	5	5	pF typ
ANALOG OUTPUTS						
Output Voltage Range	V_{OUT}		V_{SS}/V_{DD}	V_{SS}/V_{DD}	V_{SS}/V_{DD}	V min/max
Output Current Drive	I_{OUT}	Code = 80_H, ΔV_{OUT} < 1 LSB	±3	±3	±3	mA typ
Shutdown Resistance	R_{OUT}	DAC Outputs Placed in Shutdown State	120	120	120	kΩ typ
Capacitive Load[3]	C_L	No Oscillation	200	200	200	pF typ
LOGIC INPUTS						
Logic Input Low Voltage	V_{IL}		0.6	0.8	0.8	V min
Logic Input High Voltage	V_{IH}		2.1	2.4	2.4	V max
Input Leakage Current[5]	I_{IL}		±10	±10	±10	µA max
Input Capacitance[3]	C_{IL}		8	8	8	pF max
AC CHARACTERISTICS[3]						
Output Slew Rate	SR	Code = 00_H to FF_H to 00_H	1/2.7	1/3.6	1/3.6	V/µs min/typ
Reference Multiplying	BW	Small Signal, V_{SS} = –5 V			2.6	MHz typ
Total Harmonic Distortion	THD	V_{REF} = 4 V p-p, V_{SS} = –5 V, f = 1 kHz			0.025	%
Settling Time[6]	t_S	To ±0.1% of Full Scale	1.1/2	1.0/2	1.0/2	µs typ/max
Shutdown Recovery Time	t_{SDR}	To ±0.1% of Full Scale	2	2	2	µs max
Time to Shutdown	t_{SDN}		15	15	15	µs typ
DAC Glitch	Q		15	15	15	nVs typ
Digital Feedthrough	Q		2	2	2	nVs typ
Feedthrough	V_{OUT}/V_{REF}	Code = 00_H, V_{REF} =1 V p-p, f = 100 kHz			–65	dB
SUPPLY CHARACTERISTICS						
Positive Supply Current	I_{DD}	V_{LOGIC} = 0 V or V_{DD}, No Load	6	6	6	mA max
Negative Supply Current	I_{SS}	V_{SS} = –5 V			6	mA max
Power Dissipation	P_{DISS}	V_{LOGIC} = 0 V or V_{DD}, No Load	15	30	60	mW max
Power Down	I_{DD_SD}	SDI/SHDN = Floating	40	40	40	µA typ
Power Supply Sensitivity	PSS	ΔV_{DD} = ±10%	0.004	0.004	0.004	%/%

NOTES
[1]One LSB = $V_{REF}/256$.
[2]The first three codes (00_H, 01_H, 10_H) are excluded from the integral nonlinearity error measurement in single supply operation +3 V or +5 V.
[3]These parameters are guaranteed by design and not subject to production testing.
[4]Typicals represent average readings measured at +25°C.
[5]SDI/SHDN and A0/SHDN pins have 30 µA maximum I_{IL} input leakage current.
[6]The settling time specification does not apply for negative going transitions within the last 3 LSBs of ground in single supply operation.

Specifications subject to change without notice.

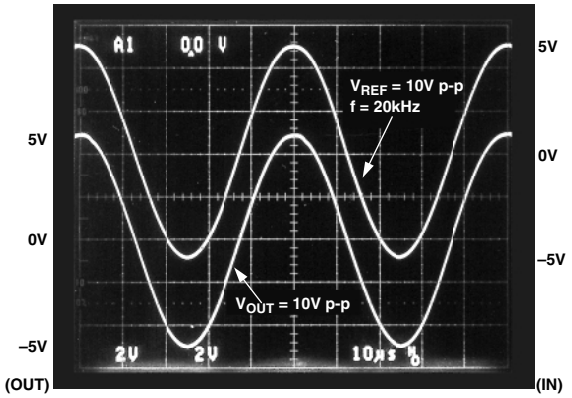


Figure 1. AD7304/AD7305 Rail-to-Rail Reference Input to Output at 20 kHz

TIMING SPECIFICATIONS (@ V_{DD} = +3 V or +5 V, V_{SS} = 0 V; or V_{DD} = +5 V and V_{SS} = –5 V, $V_{SS} \le V_{REF} \le V_{DD}$, –40°C < T_A < +85°C/125°C, unless otherwise noted.)

Parameter	Symbol	3 V ± 10%	5 V ± 10%	±5 V ± 10%	Units
INTERFACE TIMING SPECIFICATIONS[1, 2]					
AD7304 Only					
Clock Width High	t_{CH}	70	55	55	ns min
Clock Width Low	t_{CL}	70	55	55	ns min
Data Setup	t_{DS}	50	40	40	ns min
Data Hold	t_{DH}	30	20	20	ns min
Load Pulsewidth	t_{LDW}	70	60	60	ns min
Load Setup	t_{LD1}	40	30	30	ns min
Load Hold	t_{LD2}	40	30	30	ns min
Clear Pulsewidth	t_{CLWR}	60	60	60	ns min
Select	t_{CSS}	30	20	20	ns min
Deselect	t_{CSH}	60	40	40	ns min
AD7305 Only					
Data Setup	t_{DS}	60	40	40	ns min
Data Hold	t_{DH}	30	20	20	ns min
Address Setup	t_{AS}	60	40	40	ns min
Address Hold	t_{AH}	30	20	20	ns min
Write Width	t_{WR}	60	50	50	ns min
Load Pulsewidth	t_{LDW}	60	50	50	ns min
Load Setup	t_{LS}	60	40	40	ns min
Load Hold	t_{LH}	30	20	20	ns min

NOTES
[1]These parameters are guaranteed by design and not subject to production testing.
[2]All input control signals are specified with $t_R = t_F$ = 2 ns (10% to 90% of V_{DD}) and timed from a voltage level of 1.6 V.

ABSOLUTE MAXIMUM RATINGS*

V_{DD} to GND ..... –0.3 V, +8 V
V_{SS} to GND ..... +0.3 V, –8 V
V_{REFX} to GND ..... V_{SS}, V_{DD}
Logic Inputs to GND ..... –0.3 V, V_{DD} + 0.3 V
V_{OUTX} to GND ..... –0.3 V, V_{DD} + 0.3 V
I_{OUT} Short Circuit to GND ..... 50 mA
Package Power Dissipation ..... $(T_{J\,MAX}–T_A)/\theta_{JA}$
Thermal Resistance θ_{JA}
16-Lead Plastic DIP Package (N-16) ..... 103°C/W
16-Lead SOIC Package (R-16) ..... 73°C/W
TSSOP-16 Package (RU-16) ..... 180°C/W
20-Lead Plastic DIP Package (N-20) ..... 120°C/W
20-Lead SOIC Package (R-20) ..... 74°C/W
TSSOP-20 Package (RU-20) ..... 155°C/W
Maximum Junction Temperature ($T_{J\,MAX}$) ..... +150°C
Operating Temperature Range ..... –40°C to +85°C
Storage Temperature Range ..... –65°C to +150°C
Lead Temperature
N-16 and N-20 (Soldering, 10 secs) ..... +300°C
R-16, R-20, RU-16, RU-20 (Vapor Phase, 60 secs) ..+215°C
R-16, R-20, RU-16, RU-20 (Infrared, 15 secs) ....+220°C

*Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Options
AD7304BN	–40°C/+85°C	16-Lead P-DIP	N-16
AD7304BR	–40°C/+85°C	16-Lead SOIC	R-16
AD7304YR	–40°C/+125°C	16-Lead SOIC	R-16
AD7304BRU	–40°C/+85°C	TSSOP-16	RU-16
AD7305BN	–40°C/+85°C	20-Lead P-DIP	N-20
AD7305BR	–40°C/+85°C	20-Lead SOIC	R-20
AD7305YR	–40°C/+125°C	20-Lead SOIC	R-20
AD7305BRU	–40°C/+85°C	TSSOP-20	RU-20

The AD7304/AD7305 contains 2759 transistors. Die size: 103 mil × 102 mil, 10,506 sq mil.

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD7304/AD7305 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

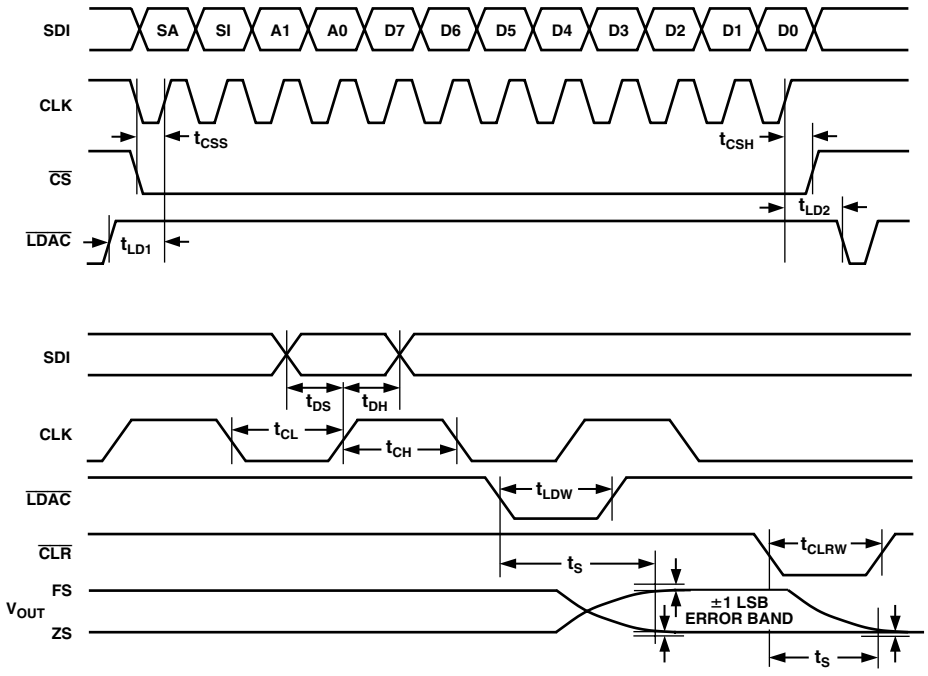


Figure 2. AD7304 Timing Diagram

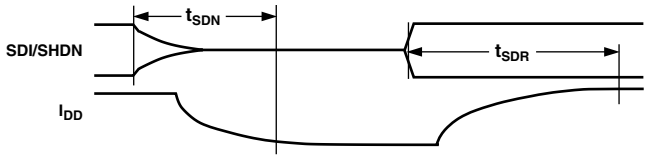


Figure 3. AD7304 Timing Diagram

Table I. AD7304 Control Logic Truth Table

$\overline{CS}$	CLK	$\overline{LDAC}$	$\overline{CLR}$	Serial Shift Register Function	Input REG Function	DAC Register Function
H	X	H	H	No Effect	No Effect	No Effect
L	↑+	H	H	Data Advanced 1 Bit	No Effect	No Effect
↑+	L	H	H	No Effect	Updated with SR Contents[2]	No Effect
H	X	L	H	No Effect	Latched with SR Contents[2]	All Input Register Contents Transferred[3]
H	X	H	↓–	No Effect	Loaded with 00_H	Loaded with 00_H
H	X	H	↑+	No Effect	Latched with 00_H	Latched with 00_H

NOTES
[1]↑+ positive logic transition; ↓– negative logic transition; X Don't Care.
[2]One Input Register receives the data bits D7–D0 decoded from the SR address bits (A1, A0); where REG A = (0, 0); B = (0, 1); C = (1, 0); D = (1, 1).
[3]$\overline{LDAC}$ is a level-sensitive input.

Table II. AD7304 Serial Input Register Data Format, Data Is Loaded in the MSB-First Format

	MSB B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	LSB B0
AD7304	SAC	SDC	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0

If B11 (SAC), *Shutdown All Channels*, is set to logic LOW, all DACs are placed in a power shutdown mode, all output voltages become high resistance. If B10 (SDC), *Shutdown Decoded Channel*, is set to logic LOW, only the DAC decoded by address bits A1 and A0 is placed in the shutdown mode.

Table III. AD7305 Control Logic Truth Table

$\overline{WR}$	A1	A0	$\overline{LDAC}$	Input Register Function	DAC Register Function
L	L	L	H	REG A Loaded with DB0–DB7	Latched with Previous Contents, No Change
↑+	L	L	H	REG A Latched with DB0–DB7	Latched with Previous Contents, No Change
L	L	H	H	REG B Loaded with DB0–DB7	Latched with Previous Contents, No Change
↑+	L	H	H	REG B Latched with DB0–DB7	Latched with Previous Contents, No Change
L	H	L	H	REG C Loaded with DB0–DB7	Latched with Previous Contents, No Change
↑+	H	L	H	REG C Latched with DB0–DB7	Latched with Previous Contents, No Change
L	H	H	H	REG D Loaded with DB0–DB7	Latched with Previous Contents, No Change
↑+	H	H	H	REG D Latched with DB0–DB7	Latched with Previous Contents, No Change
H	X	X	L	No Effect	All Input Register Contents Loaded, Register Transparent
L	X	X	L	Input REG x Transparent to DB0–DB7	Register Transparent
H	X	X	↑+	No Effect	All Input Register Contents Latched
H	X	X	H	No Effect, Device Not Selected	No Effect, Device Not Selected

NOTES
[1]↑+ positive logic transition; ↓– negative logic transition; X Don't Care.
[2]$\overline{LDAC}$ is a level sensitive input.

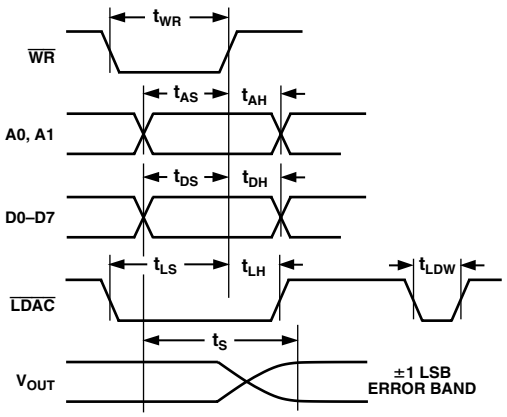


Figure 4. AD7305 Timing Diagram

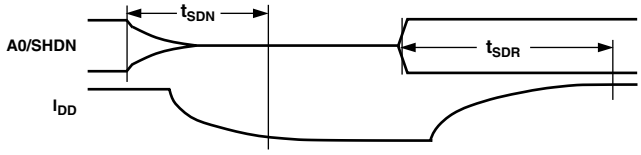
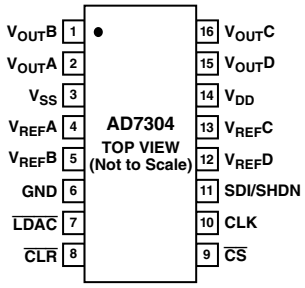
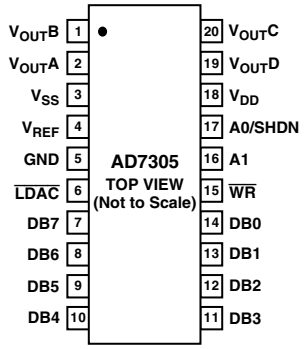


Figure 5. AD7305 Timing Diagram

PIN CONFIGURATIONS





AD7304 PIN FUNCTION DESCRIPTIONS

Pin #	Name	Function
1	$V_{OUT}B$	Channel B rail-to-rail buffered DAC voltage output. Full scale set by reference voltage applied to $V_{REF}B$ pin. Output is open circuit when SHDN is enabled.
2	$V_{OUT}A$	Channel A rail-to-rail buffered DAC voltage output. Full scale set by reference voltage applied to $V_{REF}A$ pin. Output is open circuit when SHDN is enabled.
3	V_{SS}	Negative Power Supply Input. Specified range of operation 0 V to –5.5 V.
4	$V_{REF}A$	Channel A Reference Input. Establishes $V_{OUT}A$ full-scale voltage. Specified range of operation $V_{SS} < V_{REF}A < V_{DD}$.
5	$V_{REF}B$	Channel B Reference Input. Establishes $V_{OUT}B$ full-scale voltage. Specified range of operation $V_{SS} < V_{REF}B < V_{DD}$.
6	GND	Common Analog and Digital Ground.
7	$\overline{LDAC}$	Load DAC register strobe, active low. Transfers all four Input Register data into their DAC registers. Asynchronous active low input. DAC Register is transparent when $\overline{LDAC}$ = 0. See Control Logic Truth Table for operation.
8	$\overline{CLR}$	Clears all Input and DAC registers to the zero condition. Asynchronous active low input. The serial register is not effected.
9	$\overline{CS}$	Chip Select, Active Low Input. Disables shift register loading when high. Transfers Serial Input Register Data to the decoded Input Register when $\overline{CS}$ returns HIGH. Does not effect $\overline{LDAC}$ operation.
10	CLK	Clock input, positive edge clocks data into shift register. Disabled by chip select $\overline{CS}$.
11	SDI/SHDN	Serial Data-Input loads directly into the shift register, MSB first. Hardware shutdown (SHDN) control input, active when pin is left floating by a three-state logic driver. Does not effect DAC register contents as long as power is present on V_{DD}.
12	$V_{REF}D$	Channel D Reference Input. Establishes $V_{OUT}D$ full-scale voltage. Specified range of operation $V_{SS} < V_{REF}D < V_{DD}$.
13	$V_{REF}C$	Channel C Reference Input. Establishes $V_{OUT}C$ full-scale voltage. Specified range of operation $V_{SS} < V_{REF}C < V_{DD}$.
14	V_{DD}	Positive power supply input. Specified range of operation +2.7 V to +5.5 V.
15	$V_{OUT}D$	Channel D rail-to-rail buffered DAC voltage output. Full-scale set by reference voltage applied to $V_{REF}D$ pin. Output is open circuit when SHDN is enabled.
16	$V_{OUT}C$	Channel C rail-to-rail buffered DAC voltage output. Full-scale set by reference voltage applied to $V_{REF}C$ pin. Output is open circuit when SHDN is enabled.

AD7305 PIN FUNCTION DESCRIPTIONS

Pin #	Name	Function
1	$V_{OUT}B$	Channel B rail-to-rail buffered DAC voltage output. Full scale set by reference voltage applied to $V_{REF}B$ pin. Output is open circuit when SHDN is enabled.
2	$V_{OUT}A$	Channel A rail-to-rail buffered DAC voltage output. Full scale set by reference voltage applied to $V_{REF}A$ pin. Output is open circuit when SHDN is enabled.
3	V_{SS}	Negative Power Supply Input. Specified range of operation 0 V to –5.5 V.
4	V_{REF}	Channel B Reference Input. Establishes V_{OUT} full-scale voltage. Specified range of operation $V_{SS} < V_{REF} < V_{DD}$.
5	GND	Common Analog and Digital Ground.
6	$\overline{LDAC}$	Load DAC register strobe, active low. Transfers all four Input Register data into their DAC registers. Asynchronous active low input. DAC Register is transparent when $\overline{LDAC}$ = 0. See Control Logic Truth Table for operation.
7	DB7	MSB Digital Input Data Bit.
8	DB6	Data Bit 6.
9	DB5	Data Bit 5.
10	DB4	Data Bit 4.
11	DB3	Data Bit 3.
12	DB2	Data Bit 2.
13	DB1	Data Bit 1.
14	DB0	LSB Digital Input Data Bit.
15	$\overline{WR}$	Write data into Input Register control line, active low. See Control Logic Truth Table for operation.
16	A1	Address Bit 1.
17	A0/SHDN	Address Bit 0/Hardware shutdown (SHDN) control input, active when pin is left floating by a three-state logic driver. Does not effect DAC register contents as long as power is present on V_{DD}.
18	V_{DD}	Positive Power Supply Input. Specified range of operation +2.7 V to +5.5 V.
19	$V_{OUT}D$	Channel D rail-to-rail buffered DAC voltage output. Full scale set by reference voltage applied to $V_{REF}D$ pin. Output is open circuit when SHDN is enabled.
20	$V_{OUT}C$	Channel C rail-to-rail buffered DAC voltage output. Full scale set by reference voltage applied to $V_{REF}C$ pin. Output is open circuit when SHDN is enabled.

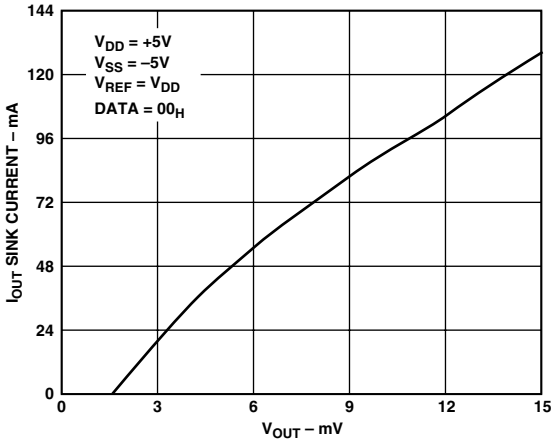


Figure 6. I_{OUT}SINK vs. V_{OUT} Rail-to-Rail Performance

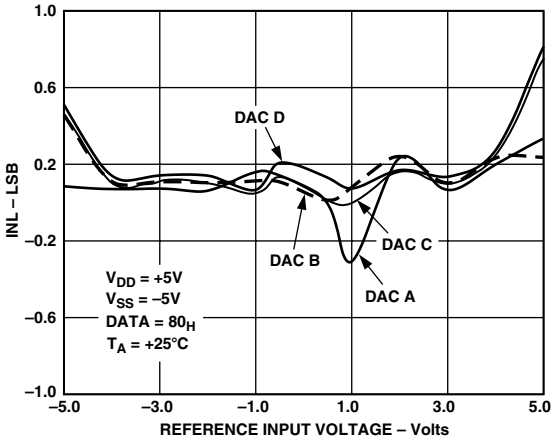


Figure 9. INL vs. Reference Input Voltage

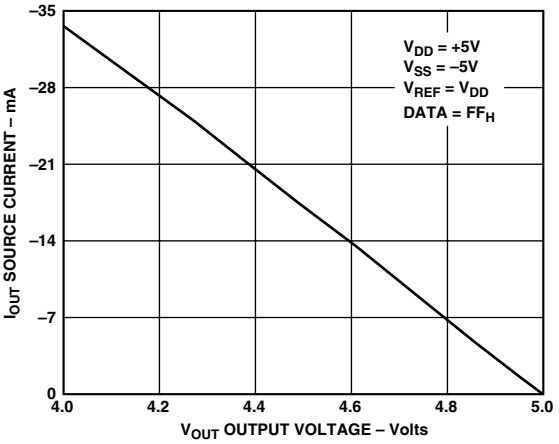


Figure 7. I_{OUT}SOURCE vs. V_{OUT} Rail-to-Rail Performance

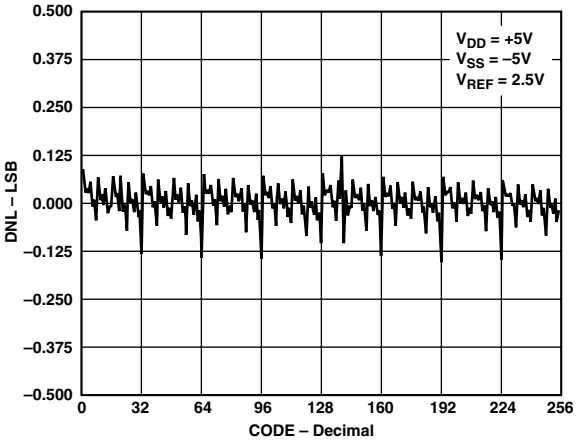


Figure 10. DNL vs. Code

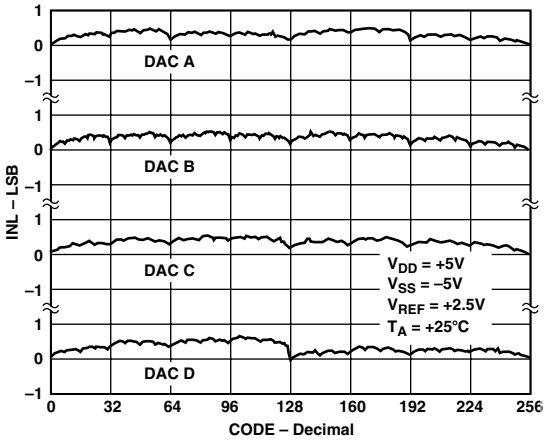


Figure 8. INL vs. Code, All DAC Channels

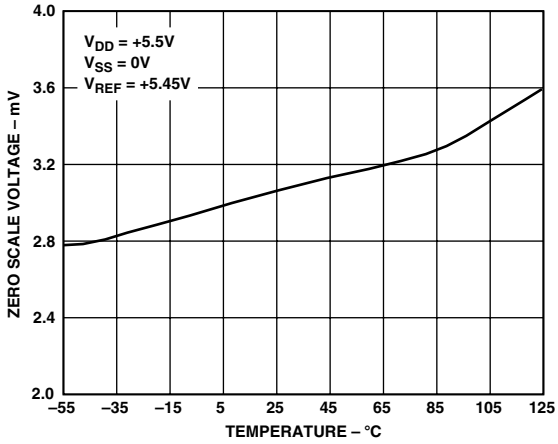


Figure 11. Zero Scale Voltage vs. Temperature

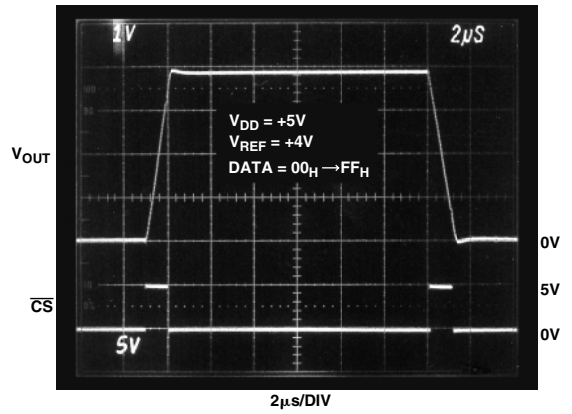


Figure 12. Large-Signal Settling Time

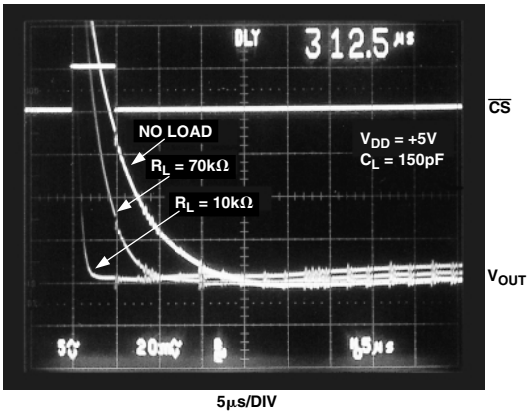


Figure 15. Time to Shutdown

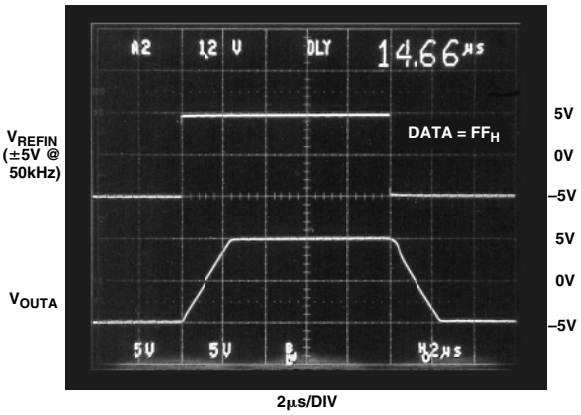


Figure 13. Multiplying Mode Step Response and Output Slew Rate

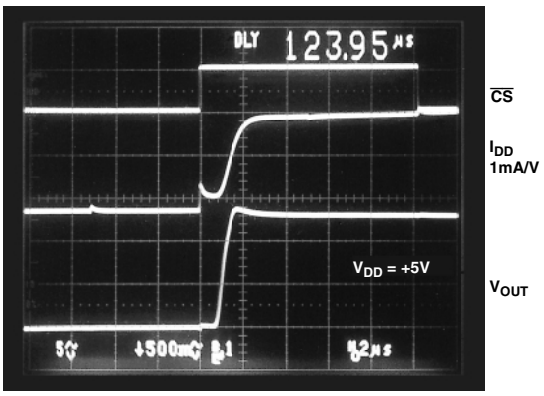


Figure 16. Shutdown Recovery Time (Wakeup)

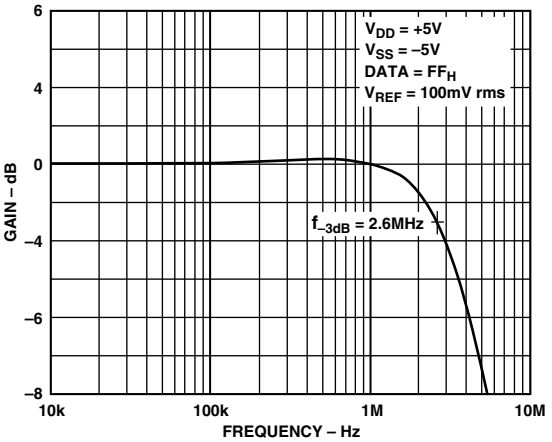


Figure 14. Multiplying Mode Gain vs. Frequency

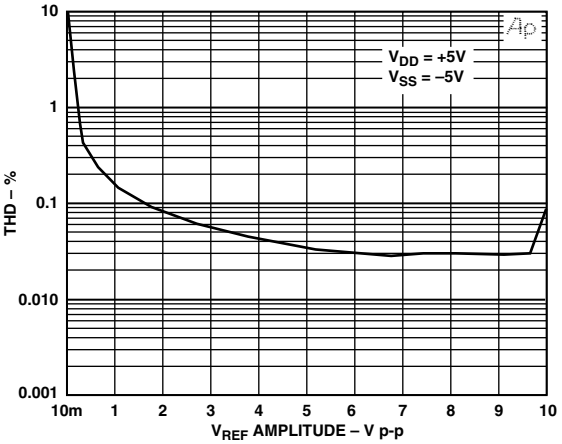


Figure 17. THD vs. Reference Input Amplitude

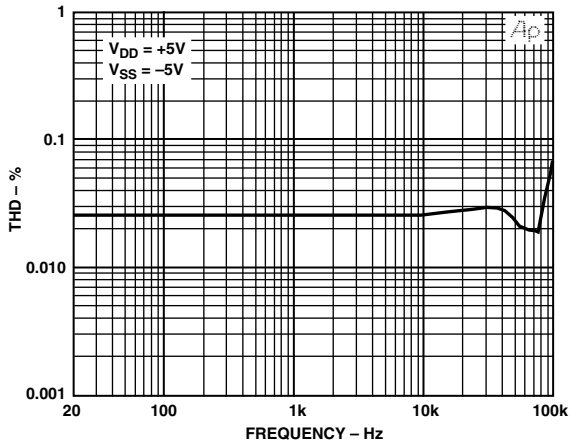


Figure 18. THD vs. Frequency

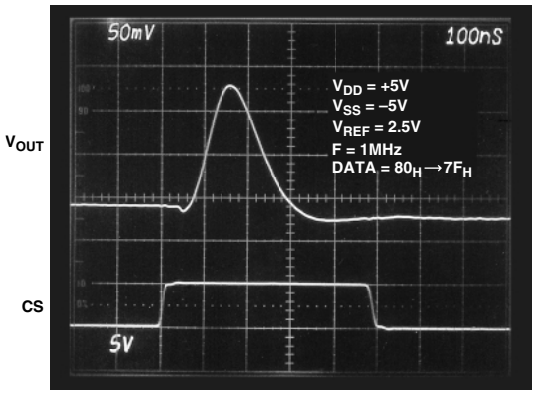


Figure 21. Midscale Transition Glitch

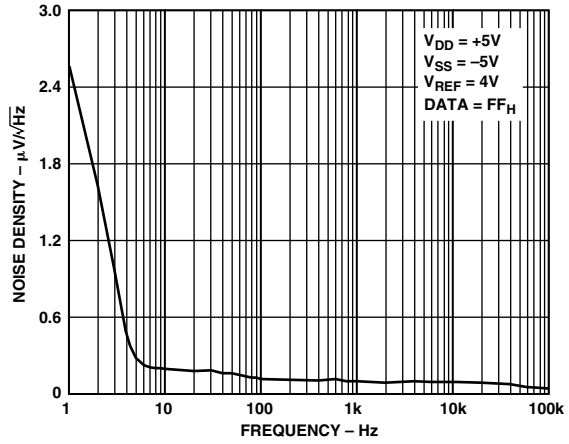


Figure 19. Output Noise Voltage Density vs. Frequency

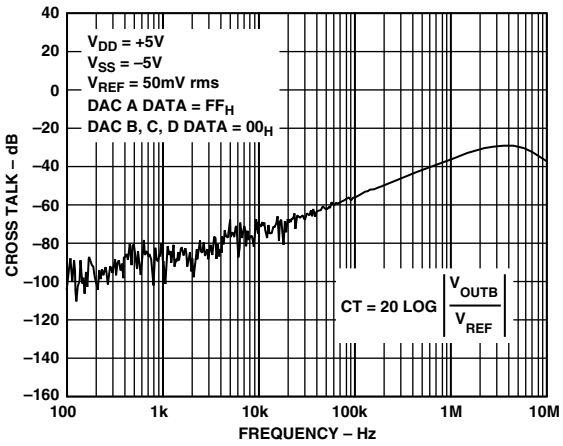


Figure 22. Crosstalk vs. Frequency

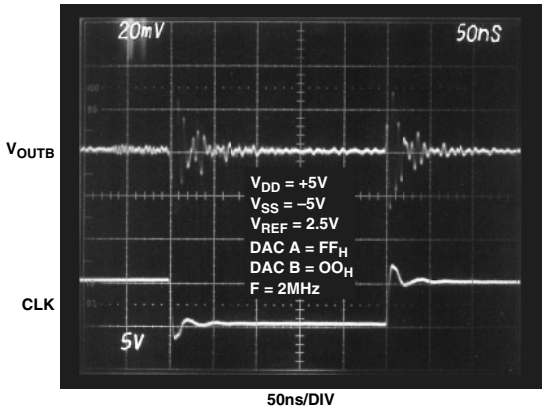


Figure 20. Digital Feedthrough

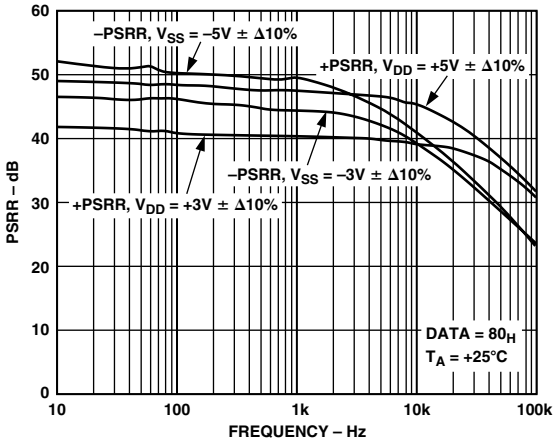


Figure 23. Power Supply Rejection vs. Frequency

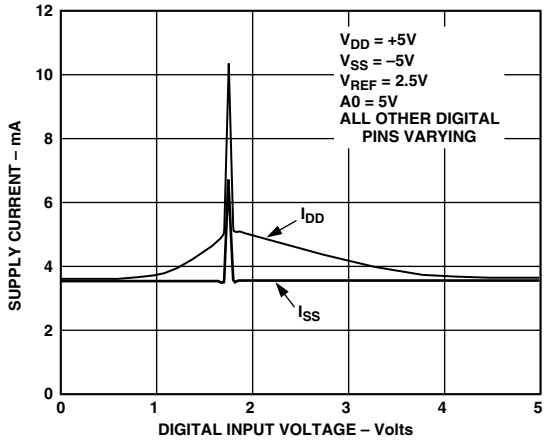


Figure 24. Supply Current vs. Digital Input Voltage

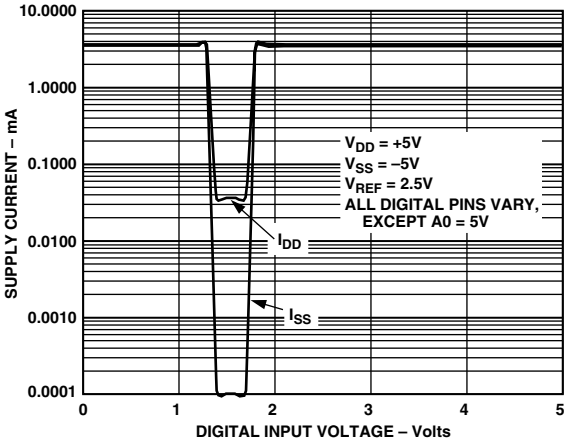


Figure 25. Shutdown Supply Current vs. Digital Input Voltage (A0 Only)

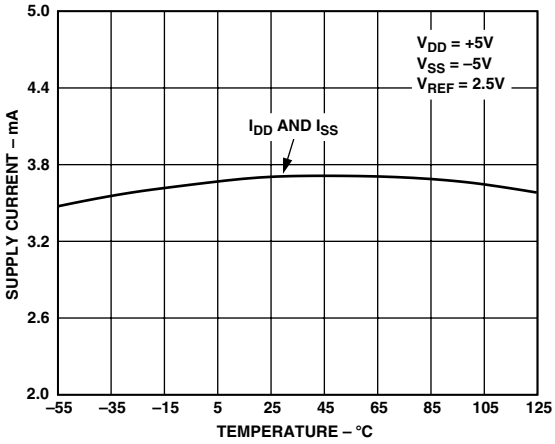


Figure 26. Supply Current vs. Temperature

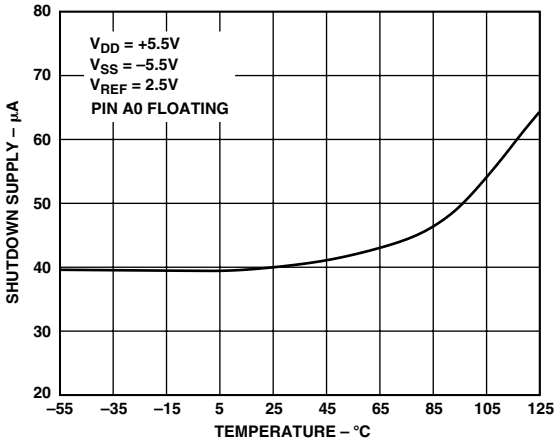


Figure 27. Shutdown Supply Current vs. Temperature

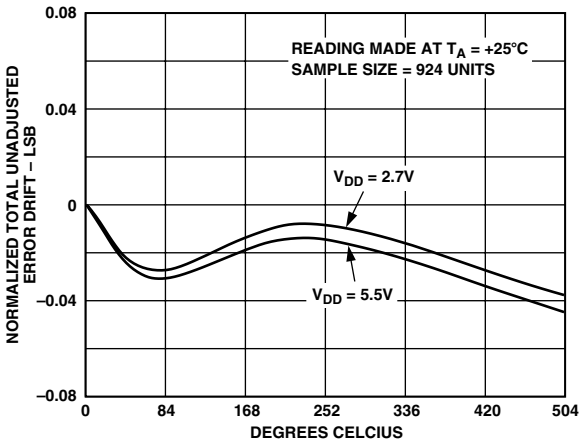


Figure 28. Normalized TUE Drift Accelerated by Burn-In Hours of Operation @ 150°C

CIRCUIT OPERATION

The AD7304/AD7305 are a set of four-channel, 8-bit, voltage-output, digital-to-analog converters differing primarily in digital logic interface and number of reference inputs. Both parts share the same internal DAC design and true rail-to-rail output buffers. The AD7304 contains four independent multiplying reference inputs, while the AD7305 has one common reference input. The AD7304 uses a 3-wire SPI compatible serial data interface, while the AD7305 offers a 8-bit parallel data interface.

D/A Converter Section

Each part contains four voltage-switched R-2R ladder DACs. Figure A shows a typical equivalent DAC. These DACs are designed to operate both single-supply or dual supply, depending on whether the user supplies a negative voltage on the V_{SS} pin. In a single-supply application the V_{SS} is tied to ground. In either mode the DAC output voltage is determined by the V_{REF} input voltage and the digital data (D) loaded into the corresponding DAC register according to Equation 1.

$$V_{OUT} = V_{REF} \times D/256 \quad (1)$$

Note that the output full-scale polarity is the same as the V_{REF} polarity for dc reference voltages.

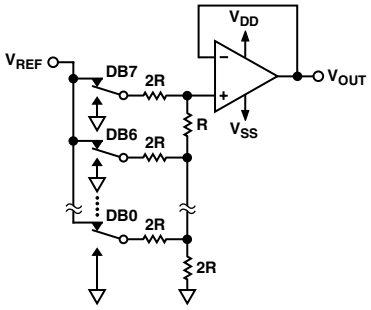


Figure 29. Typical Equivalent DAC Channel

These DACs are also designed to accommodate ac reference input signals. As long as the ac signals are maintained between $V_{SS} < V_{REF} < V_{DD}$, the user can expect 50 kHz of full-power multiplying bandwidth performance. In order to use negative input reference voltages, the V_{SS} pin must be biased with a negative voltage of equal or greater magnitude than the reference voltage.

The reference inputs are code-dependent, exhibiting worst case minimum resistance values specified in the parametric specification table. The DAC outputs V_{OUT}A, B, C, D are each capable of driving 2 kΩ loads in parallel with up to 500 pF loads. Output source and sink current is shown in Figures 6 and 7. The output slew rate is nominally 3.6 V/μs while operating from ±5 V supplies. The low output impedance of the buffers minimizes crosstalk between analog input channels. At 100 kHz, 65 dB of channel-to-channel isolation exists (Figure 22). Output voltage noise is plotted in Figure 19. In order to maintain good analog performance, power supply bypassing of 0.01 μF in parallel with 1 μF is recommended. The true rail-to-rail capability of the AD7304/AD7305 allows the user to connect the reference inputs directly to the same supply as the V_{DD} or V_{SS} pin (Figure 30). Under these conditions clean power supply voltages (low ripple, avoid switching supplies) appropriate for the application should be used.

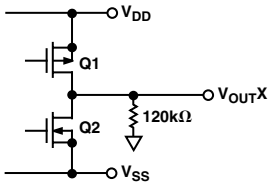


Figure 30. Equivalent DAC Amplifier Output Circuit

AD7304 SERIAL DATA INTERFACE

The AD7304 uses a 3-wire ($\overline{CS}$, SDI, CLK) SPI compatible serial data interface. New serial data is clocked into the serial input register in a 12-bit data-word format. MSB bits are loaded first. Table II defines the 12 data-word bits. Data is placed on the SDI/SHDN pin and clocked into the register on the positive clock edge of CLK subject to the data setup and data hold time requirements specified in the TIMING SPECIFICATIONS. Data can only be clocked in while the $\overline{CS}$ chip select pin is active low. Only the last 12-bits clocked into the serial register will be interrogated when the $\overline{CS}$ pin returns to the logic high state, extra data bits are ignored. Since most microcontrollers output serial data in 8-bit bytes, two right justified data bytes can be written to the AD7304. Keeping the $\overline{CS}$ line low between the first and second byte transfer will result in a successful serial register update.

Once the data is properly aligned in the shift register the positive edge of the $\overline{CS}$ initiates either the transfer of new data to the target DAC register, determined by the decoding of address bits A1 and A0, or the shutdown features will be activated based on the SAC or SDC bits. When either SAC or SDC pins are set (Logic = 0) the loading of new data determined by Bits B9 to B0 are still loaded, but the results do not appear on the buffer outputs until the device is brought out of the shutdown state. The selected DAC output voltages become high impedance with a nominal resistance of 120 kΩ to ground, Figure 30. If both SAC and SDC pins are set, all channels are still placed in the shutdown mode. When the AD7304 has been programmed into the power shutdown state, the present DAC register data is maintained as long as V_{DD} remains greater than 2.7 volts. The remaining characteristics of the software serial interface are defined by Tables I, II and Figure 3 timing diagram.

Two additional pins $\overline{CLR}$ and $\overline{LDAC}$ on the AD7304 provide hardware control over the clear function and the DAC Register loading. If these functions are not needed the $\overline{CLR}$ pin can be tied to logic high, and the $\overline{LDAC}$ pin can be tied to logic low. The asynchronous input $\overline{CLR}$ pin forces all input and DAC registers to the zero-code state. The asynchronous $\overline{LDAC}$ pin can be strobed to active low when all DAC Registers need to be updated simultaneously from their respective Input Registers. The $\overline{LDAC}$ pin places the DAC Register in a transparent mode while in the logic low state.

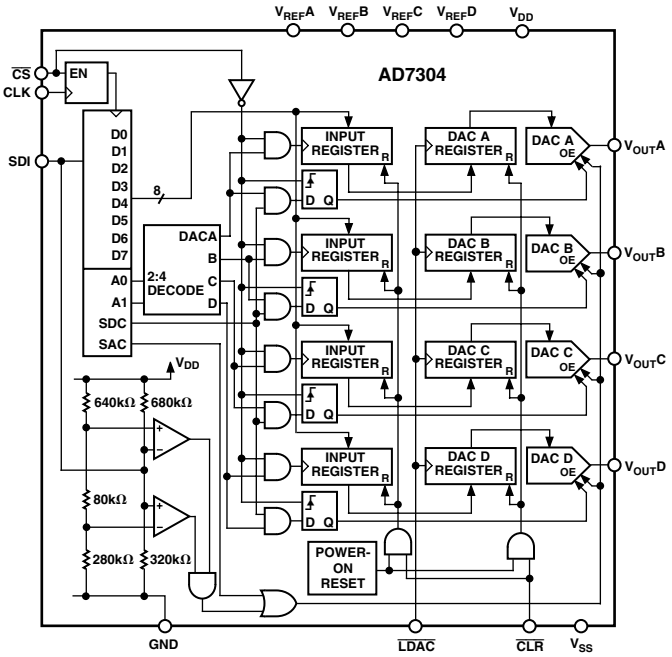


Figure 31. AD7304 Equivalent Logic Interface

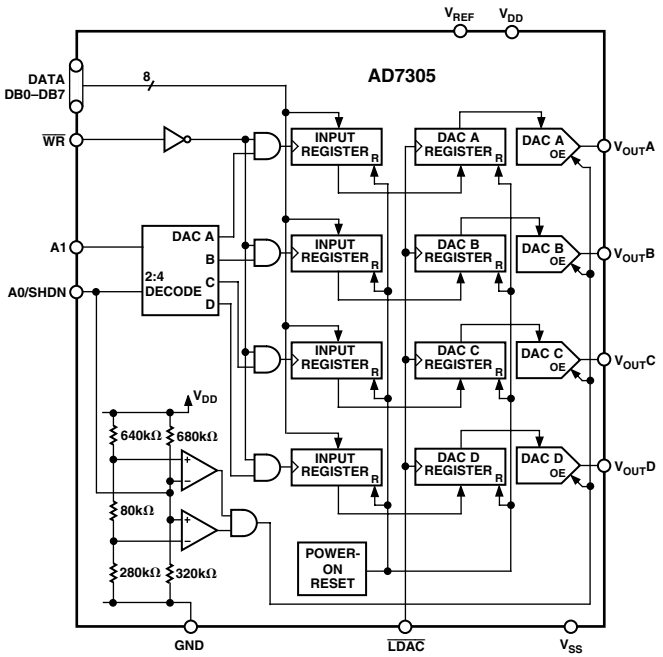


Figure 32. AD7305 Equivalent Logic Interface

AD7304 Hardware Shutdown SHDN

If a three-state driver is used on the SDI/SHDN pin, the AD7304 can be placed into a power shutdown mode when the SDI/SHDN pin is placed in a high impedance state. For proper operation no other termination voltages should be present on this pin. An internal window comparator will detect when the logic voltage on the SHDN pin is between 28% and 36% of V_{DD}. A high impedance internal bias generator provides this voltage on the SHDN pin. The four DAC output voltages become high impedance with a nominal resistance of 120 kΩ to ground. See Figure 30 for an equivalent circuit.

AD7304/AD7305 POWER ON RESET

When the V_{DD} power supply is turned on, an internal reset strobe forces all the Input and DAC registers to the zero-code state. The V_{DD} power supply should have a monotonically increasing ramp in order to have consistent results, especially in the region of V_{DD} = 1.5 V to 2.3 V. The V_{SS} supply has no effect on the power ON reset performance. The DAC register data will stay at zero until a valid serial register software load takes place. In the case of the double buffered AD7305 the output DAC register can only be changed once the $\overline{LDAC}$ strobe is initiated.

AD7305 PARALLEL DATA INTERFACE

The AD7305 has an 8-bit parallel interface DB7 = MSB, DB0 = LSB. Two address Bits A1 and A0 are decoded when an active low write strobe is placed on the $\overline{WR}$ pin, see Table III. The $\overline{WR}$ is a level-sensitive input pin, therefore the data setup and data hold times defined in the TIMING SPECIFICATIONS need to be adhered to.

The $\overline{LDAC}$ pin provides the capability of simultaneously updating all DAC registers with new data from the Input Registers at the same time. This will result in the analog outputs all changing to their new values at the same time. The $\overline{LDAC}$ pin is a level-sensitive input. If the simultaneous update feature is not required the $\overline{LDAC}$ pin can be tied to logic low. When the $\overline{LDAC}$ is tied to logic low, the DAC Registers become transparent and the Input Register data determines the DAC output voltage. See Figure 32 for an equivalent interface logic diagram.

AD7226 Pin Compatibility

By tying the $\overline{LDAC}$ pin to ground, the AD7305 has the same pin out and functionality as the AD7226, with the exception of a lower power supply operating voltage.

AD7305 Hardware Shutdown SHDN

If a three state driver is used on the A0/SHDN pin, the AD7305 can be placed into a power shutdown mode when the A0/SHDN pin is placed in a high impedance state. For proper operation no other termination voltages should be present on this pin. An internal window comparator will detect when the logic voltage on the SHDN pin is between 28% and 36% of V_{DD}. A high impedance internal bias generator provides this voltage on the SHDN pin. The four DAC output voltages become high impedance with a nominal resistance of 120 kΩ to ground.

ESD Protection Circuits

All logic input pins contain back-biased ESD protection Zeners connected to ground (GND). The V_{REF} pins also contain a back-biased ESD protection Zener connected to V_{DD} (see Figure 33).

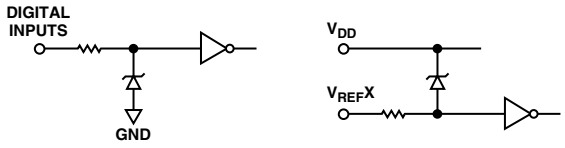


Figure 33. Equivalent ESD Protection Circuits

APPLICATIONS

The AD7304/AD7305 is inherently a 2-quadrant multiplying D/A converter. That is, it can easily be set up for unipolar output operation. The full-scale output polarity is the same as the reference input voltage polarity.

In some applications it may be necessary to generate the full 4-quadrant multiplying capability or a bipolar output swing. This is easily accomplished using an external true rail-to-rail op amp, such as the OP295. Connecting the external amplifier with two equal value resistors as shown in Figure 34 results in a full 4-quadrant multiplying circuit. In this circuit the amplifier provides a gain of two, which increases the output span magnitude to 10 volts. The transfer equation of this circuit shows that both negative and positive output voltages are created as the input data (D) is incremented from code zero (V_{OUT} = –5 V) to midscale (V_{OUT} = 0 V) to full scale (V_{OUT} = +5 V).

$$V_{OUT} = (D/128 - 1) \times V_{REF} \quad (2)$$

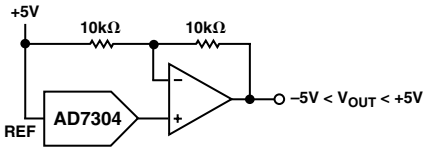
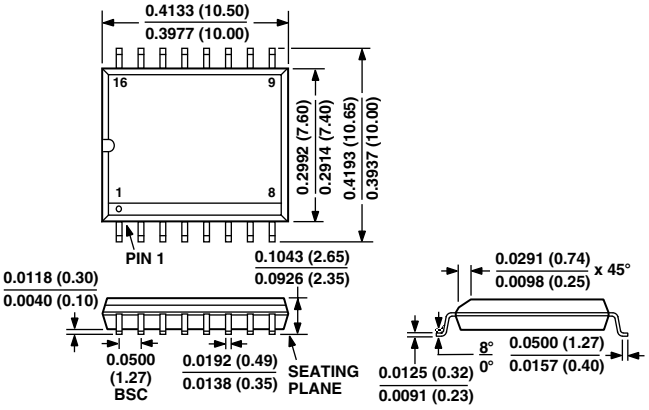


Figure 34. Four-Quadrant Multiplying Application Circuit

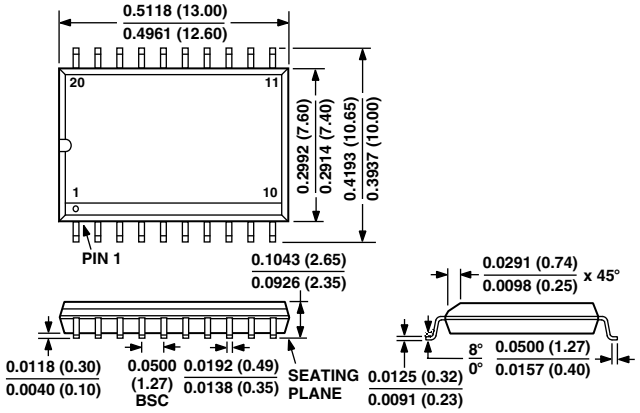
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

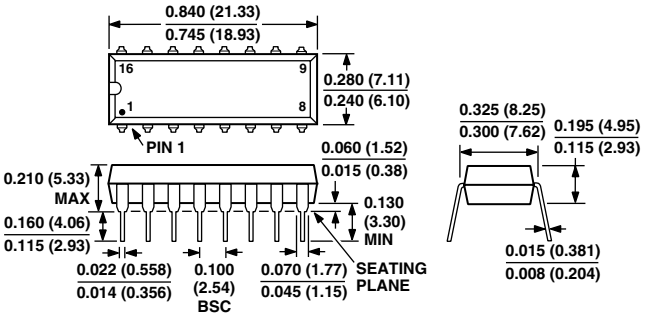
16-Lead Wide SOIC (R-16)



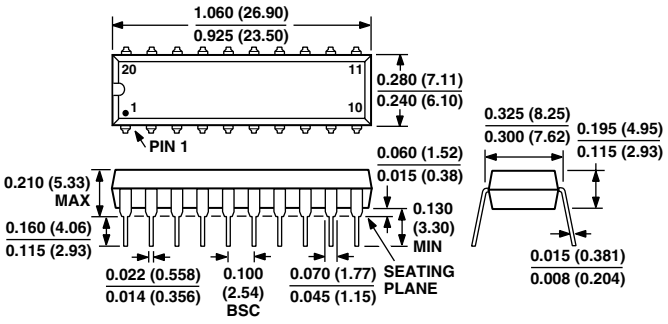
20-Lead SOIC (R-20)



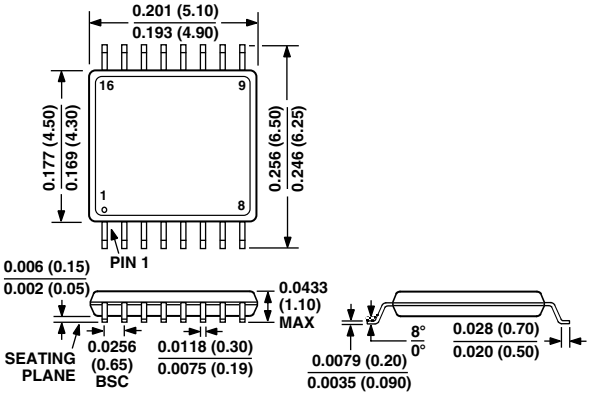
16-Lead Plastic DIP (N-16)



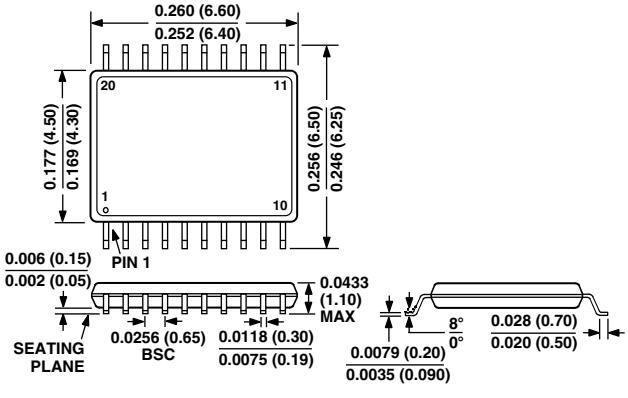
20-Lead Plastic DIP (N-20)



16-Lead TSSOP (RU-16)



20-Lead Thin Surface Mount (TSSOP) (RU-20)



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