Low-Cost, High-Speed Differential Driver

AD8131

FEATURES

High Speed
- **400 MHz –3 dB Full Power Bandwidth**
- **2000 V/μs Slew Rate**

Fixed Gain of 2 with No External Components
Internal Common-Mode Feedback to Improve Gain and Phase Balance
- **–60 dB @10 MHz**

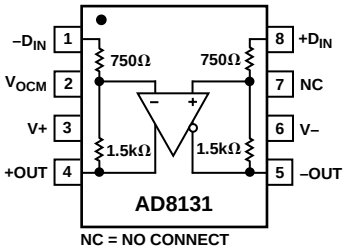
Separate Input to Set the Common-Mode Output Voltage
Low Distortion
- **68 dB SFDR @ 5 MHz 200 Ω Load**

Low Power 7.5 mA @ 3 V
Power Supply Range +2.7 V to ±5 V

APPLICATIONS

Video Line Driver
Digital Line Driver
Low Power Differential ADC Driver
Differential In/Out Level Shifting
Single-Ended Input to Differential Output Driver

FUNCTIONAL BLOCK DIAGRAM



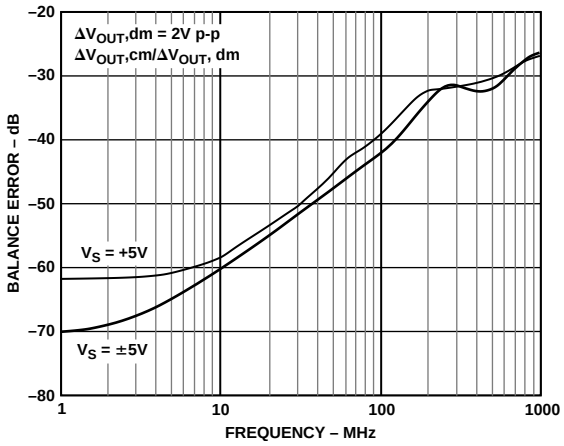


Figure 1. Output Balance Error vs. Frequency

GENERAL DESCRIPTION

The AD8131 is a differential or single-ended input to differential output driver requiring no external components for a fixed gain of 2. The AD8131 is a major advancement over op amps for driving signals over long lines or for driving differential input ADCs. The AD8131 has a unique internal feedback feature that provides output gain and phase matching that are balanced to –60 dB at 10 MHz, reducing radiated EMI and suppressing harmonics. Manufactured on ADI's next generation XFCB bipolar process, the AD8131 has a –3 dB bandwidth of 400 MHz and delivers a differential signal with very low harmonic distortion.

The AD8131 is a differential driver for the transmission of high-speed signals over low-cost twisted pair or coax cables. The AD8131 can be used for either analog or digital video signals or for other high-speed data transmission. The AD8131 driver is capable of driving either Cat3 or Cat5 twisted pair or coax with minimal line attenuation. The AD8131 has considerable cost and performance improvements over discrete line driver solutions.

The AD8131 can replace transformers in a variety of applications preserving low frequency and dc information. The AD8131 does not have the susceptibility to magnetic interference and hysteresis of transformers, while being smaller in size, easier to work with, and has the high reliability associated with ICs.

The AD8131's differential output also helps balance the input for differential ADCs, optimizing the distortion performance of the ADCs. The common-mode level of the differential output is adjustable by a voltage on the V_{OCM} pin, easily level-shifting the input signals for driving single supply ADCs with dual supply signals. Fast overload recovery preserves sampling accuracy.

The AD8131 will be available in both SOIC and μSOIC packages for operation over –40°C to +85°C.

REV. 0

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AD8131—SPECIFICATIONS (@ 25°C, V_S = ±5 V, V_{OCM} = 0, G = 2, $R_{L,dm}$ = 200 Ω, unless otherwise noted. Refer to Figures 2 and 37 for test setup and label descriptions. All specifications refer to single-ended input and differential outputs unless noted.)

Parameter	Conditions	Min	Typ	Max	Unit
±D_{IN} to ±OUT Specifications					
DYNAMIC PERFORMANCE					
–3 dB Large Signal Bandwidth	V_{OUT} = 2 V p-p		400		MHz
–3 dB Small Signal Bandwidth	V_{OUT} = 0.2 V p-p		320		MHz
Bandwidth for 0.1 dB Flatness	V_{OUT} = 0.2 V p-p		85		MHz
Slew Rate	V_{OUT} = 2 V p-p, 10% to 90%		2000		V/µs
Settling Time	0.1%, V_{OUT} = 2 V p-p		14		ns
Overdrive Recovery Time	V_{IN} = 5 V to 0 V Step		5		ns
NOISE/HARMONIC PERFORMANCE					
Second Harmonic	V_{OUT} = 2 V p-p, 5 MHz, $R_{L,dm}$ = 200 Ω		–68		dBc
	V_{OUT} = 2 V p-p, 20 MHz, $R_{L,dm}$ = 200 Ω		–63		dBc
	V_{OUT} = 2 V p-p, 5 MHz, $R_{L,dm}$ = 800 Ω		–95		dBc
	V_{OUT} = 2 V p-p, 20 MHz, $R_{L,dm}$ = 800 Ω		–79		dBc
Third Harmonic	V_{OUT} = 2 V p-p, 5 MHz, $R_{L,dm}$ = 200 Ω		–94		dBc
	V_{OUT} = 2 V p-p, 20 MHz, $R_{L,dm}$ = 200 Ω		–70		dBc
	V_{OUT} = 2 V p-p, 5 MHz, $R_{L,dm}$ = 800 Ω		–101		dBc
	V_{OUT} = 2 V p-p, 20 MHz, $R_{L,dm}$ = 800 Ω		–77		dBc
IMD	20 MHz, $R_{L,dm}$ = 800 Ω		–54		dBc
IP3	20 MHz, $R_{L,dm}$ = 800 Ω		30		dBm
Voltage Noise (RTO)	f = 20 MHz		25		nV/√Hz
Differential Gain Error	NTSC, $R_{L,dm}$ = 150 Ω		0.01		%
Differential Phase Error	NTSC, $R_{L,dm}$ = 150 Ω		0.06		Degrees
INPUT CHARACTERISTICS					
Offset Voltage	$V_{OS,dm}$ = $V_{OUT,dm}$; V_{DIN+} = V_{DIN-} = V_{OCM} = 0 V		±2	±7	mV
	T_{MIN} to T_{MAX} Variation		±8		µV/°C
	V_{OCM} = Float		±4		mV
	T_{MIN} to T_{MAX} Variation		±10		µV/°C
Input Resistance	Single-Ended Input		1.125		kΩ
	Differential Input		1.5		kΩ
Input Capacitance			1		pF
Input Common-Mode Voltage			–7.0 to +5.0		V
CMRR	$\Delta V_{OUT,dm}/\Delta V_{IN,cm}$; $\Delta V_{IN,cm}$ = ±0.5 V		–70		dB
OUTPUT CHARACTERISTICS					
Output Voltage Swing	Maximum ΔV_{OUT}; Single-Ended Output		–3.6 to +3.6		V
Linear Output Current			60		mA
Gain	$\Delta V_{OUT,dm}/\Delta V_{IN,dm}$; $\Delta V_{IN,dm}$ = ±0.5 V	1.97	2	2.03	V/V
Output Balance Error	$\Delta V_{OUT,cm}/\Delta V_{OUT,dm}$; $\Delta V_{OUT,dm}$ = 1 V		–70		dB
V_{OCM} to ±OUT Specifications					
DYNAMIC PERFORMANCE					
–3 dB Bandwidth	ΔV_{OCM} = 600 mV		210		MHz
Slew Rate	V_{OCM} = –1 V to +1 V		500		V/µs
DC PERFORMANCE					
Input Voltage Range			±3.6		V
Input Resistance			120		kΩ
Input Offset Voltage	$V_{OS,cm}$ = $V_{OUT,cm}$; V_{DIN+} = V_{DIN-} = V_{OCM} = 0 V		±1.5	±7	mV
	V_{OCM} = Float		±2.5		mV
Input Bias Current			0.5		µA
V_{OCM} CMRR	[$\Delta V_{OUT,dm}/\Delta V_{OCM}$]; ΔV_{OCM} = ±0.5 V		–60		dB
Gain	$\Delta V_{OUT,cm}/\Delta V_{OCM}$; ΔV_{OCM} = ±1 V	0.988	1	1.012	V/V
POWER SUPPLY					
Operating Range		±1.4		±5.5	V
Quiescent Current	V_{DIN+} = V_{DIN-} = V_{OCM} = 0 V	10.5	11.5	12.5	mA
	T_{MIN} to T_{MAX} Variation		25		µA/°C
Power Supply Rejection Ratio	$\Delta V_{OUT,dm}/\Delta V_S$; ΔV_S = ±1 V		–70	–56	dB
OPERATING TEMPERATURE RANGE		–40		+85	°C

Specifications subject to change without notice.

SPECIFICATIONS

(@ 25°C, V_S = 5 V, V_{OCM} = 2.5 V, G = 2, $R_{L,dm}$ = 200 Ω, unless otherwise noted. Refer to Figures 2 and 37 for test setup and label descriptions. All specifications refer to single-ended input and differential outputs unless noted.)

Parameter	Conditions	Min	Typ	Max	Unit
±D_{IN} to ±OUT Specifications					
DYNAMIC PERFORMANCE					
–3 dB Large Signal Bandwidth	V_{OUT} = 2 V p-p		385		MHz
–3 dB Small Signal Bandwidth	V_{OUT} = 0.2 V p-p		285		MHz
Bandwidth for 0.1 dB Flatness	V_{OUT} = 0.2 V p-p		65		MHz
Slew Rate	V_{OUT} = 2 V p-p, 10% to 90%		1600		V/µs
Settling Time	0.1%, V_{OUT} = 2 V p-p		18		ns
Overdrive Recovery Time	V_{IN} = 5 V to 0 V Step		5		ns
NOISE/HARMONIC PERFORMANCE					
Second Harmonic	V_{OUT} = 2 V p-p, 5 MHz, $R_{L,dm}$ = 200 Ω		–67		dBc
	V_{OUT} = 2 V p-p, 20 MHz, $R_{L,dm}$ = 200 Ω		–56		dBc
	V_{OUT} = 2 V p-p, 5 MHz, $R_{L,dm}$ = 800 Ω		–94		dBc
	V_{OUT} = 2 V p-p, 20 MHz, $R_{L,dm}$ = 800 Ω		–77		dBc
Third Harmonic	V_{OUT} = 2 V p-p, 5 MHz, $R_{L,dm}$ = 200 Ω		–74		dBc
	V_{OUT} = 2 V p-p, 20 MHz, $R_{L,dm}$ = 200 Ω		–67		dBc
	V_{OUT} = 2 V p-p, 5 MHz, $R_{L,dm}$ = 800 Ω		–95		dBc
	V_{OUT} = 2 V p-p, 20 MHz, $R_{L,dm}$ = 800 Ω		–74		dBc
IMD	20 MHz, $R_{L,dm}$ = 800 Ω		–51		dBc
IP3	20 MHz, $R_{L,dm}$ = 800 Ω		29		dBm
Voltage Noise (RTO)	f = 20 MHz		25		nV/√Hz
Differential Gain Error	NTSC, $R_{L,dm}$ = 150 Ω		0.02		%
Differential Phase Error	NTSC, $R_{L,dm}$ = 150 Ω		0.08		Degrees
INPUT CHARACTERISTICS					
Offset Voltage	$V_{OS,dm}$ = $V_{OUT,dm}$; V_{DIN+} = V_{DIN-} = V_{OCM} = 2.5 V		±3	±7	mV
	T_{MIN} to T_{MAX} Variation		±8		µV/°C
	V_{OCM} = Float		±4		mV
	T_{MIN} to T_{MAX} Variation		±10		µV/°C
Input Resistance	Single-Ended Input		1.125		kΩ
	Differential Input		1.5		kΩ
Input Capacitance			1		pF
Input Common-Mode Voltage			–1.0 to +4.0		V
CMRR	$\Delta V_{OUT,dm}/\Delta V_{IN,cm}$; $\Delta V_{IN,cm}$ = ±0.5 V		–70		dB
OUTPUT CHARACTERISTICS					
Output Voltage Swing	Maximum ΔV_{OUT}; Single-Ended Output		1.0 to 3.7		V
Linear Output Current			45		mA
Gain	$\Delta V_{OUT,dm}/\Delta V_{IN,dm}$; $\Delta V_{IN,dm}$ = ±0.5 V	1.96	2	2.04	V/V
Output Balance Error	$\Delta V_{OUT,cm}/\Delta V_{OUT,dm}$; $\Delta V_{OUT,dm}$ = 1 V		–62		dB
V_{OCM} to ±OUT Specifications					
DYNAMIC PERFORMANCE					
–3 dB Bandwidth	ΔV_{OCM} = 600 mV		200		MHz
Slew Rate	V_{OCM} = 1.5 V to 3.5 V		450		V/µs
DC PERFORMANCE					
Input Voltage Range			1.0 to 3.7		V
Input Resistance			30		kΩ
Input Offset Voltage	$V_{OS,cm}$ = $V_{OUT,cm}$; V_{DIN+} = V_{DIN-} = V_{OCM} = 2.5 V		±5	±12	mV
	V_{OCM} = Float		±10		mV
Input Bias Current			0.5		µA
V_{OCM} CMRR	$[\Delta V_{OUT,dm}/\Delta V_{OCM}]$; ΔV_{OCM} = 2.5 V ± 0.5 V		–60		dB
Gain	$\Delta V_{OUT,cm}/\Delta V_{OCM}$; ΔV_{OCM} = 2.5 V ± 1 V	0.985	1	1.015	V/V
POWER SUPPLY					
Operating Range		2.7		11	V
Quiescent Current	V_{DIN+} = V_{DIN} = V_{OCM} = 2.5 V	9.25	10.25	11.25	mA
	T_{MIN} to T_{MAX} Variation		20		µA/°C
Power Supply Rejection Ratio	$\Delta V_{OUT,dm}/\Delta V_S$; ΔV_S = ±0.5 V		–70	–56	dB
OPERATING TEMPERATURE RANGE		–40		+85	°C

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

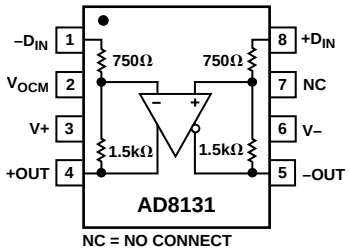
Supply Voltage . . . . . ±5.5 V
V_{OCM} . . . . . $\pm V_S$
Internal Power Dissipation[2] . . . . . 250 mW
Operating Temperature Range . . . . . –40°C to +85°C
Storage Temperature Range . . . . . –65°C to +150°C
Lead Temperature (Soldering 10 sec) . . . . . 300°C

NOTES
[1] Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only, functional operation of the device at these or any other conditions above listed in the operational section of this specification is not implied. Exposure to Absolute Maximum Ratings for any extended periods may affect device reliability.
[2] Thermal resistance measured on SEMI standard 4-layer board.
8-Lead SOIC θ_{JA} = 121°C/W
8-Lead µSOIC θ_{JA} = 142°C/W

PIN FUNCTION DESCRIPTIONS

Pin No.	Name	Function
1	$-D_{IN}$	Negative Input.
2	V_{OCM}	Voltage applied to this pin sets the common-mode output voltage with a ratio of 1:1. For example, 1 V dc on V_{OCM} will set the dc bias level on +OUT and –OUT to 1 V.
3	V+	Positive Supply Voltage.
4	+OUT	Positive Output. Note: the voltage at $-D_{IN}$ is inverted at +OUT.
5	–OUT	Negative Output. Note: the voltage at $+D_{IN}$ is inverted at –OUT.
6	V–	Negative Supply Voltage.
7	NC	No Connect.
8	$+D_{IN}$	Positive Input

PIN CONFIGURATION



ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD8131AR	–40°C to +85°C	8-Lead SOIC	SO-8
AD8131AR-REEL			
AD8131AR-REEL7			
AD8131ARM	–40°C to +85°C	8-Lead µSOIC	RM-8
AD8131ARM-REEL			
AD8131ARM-REEL7			
AD8131-EVAL		Evaluation Board	

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD8131 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

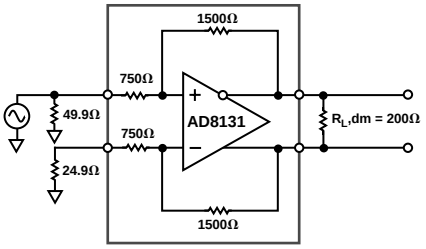


Figure 2. Basic Test Circuit

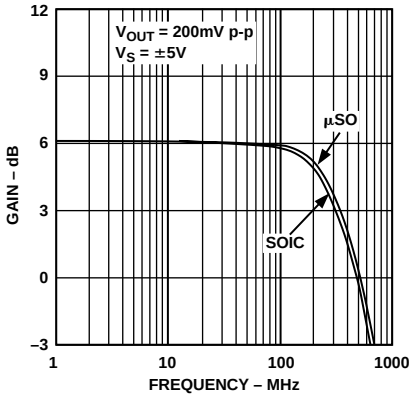


Figure 3. Small Signal Frequency Response

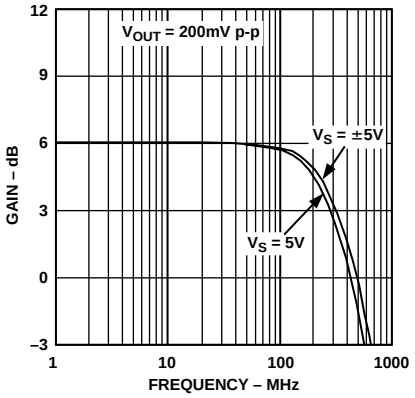


Figure 4. Small Signal Frequency Response

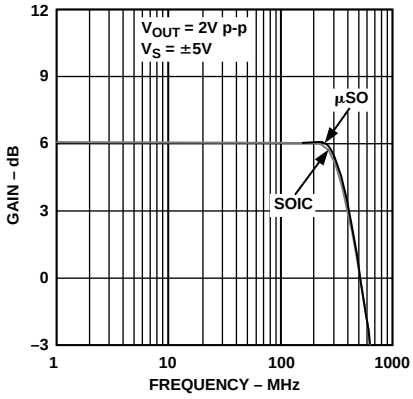


Figure 5. Large Signal Frequency Response

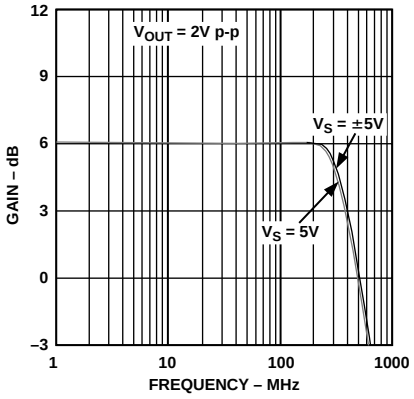


Figure 6. Large Signal Frequency Response

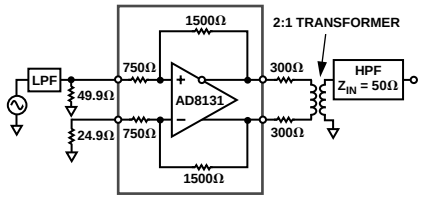


Figure 7. Harmonic Distortion Test Circuit ($R_{L,dm}$ = 800 Ω)

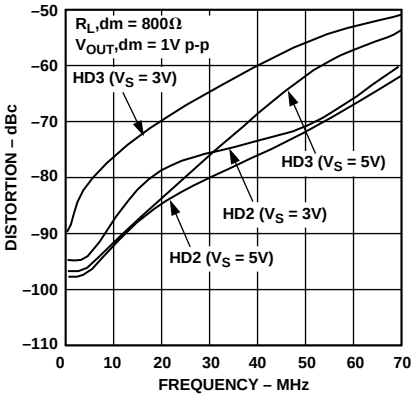


Figure 8. Harmonic Distortion vs. Frequency

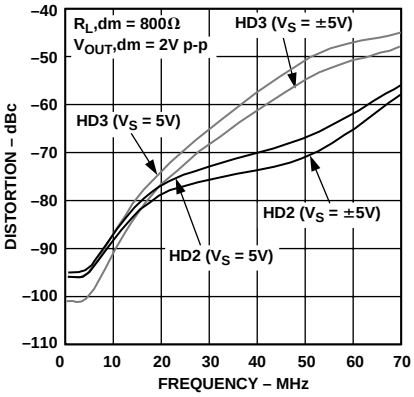


Figure 9. Harmonic Distortion vs. Frequency

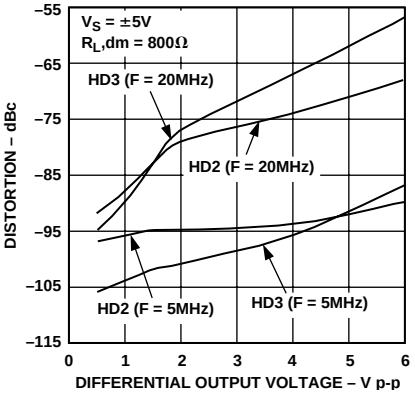


Figure 10. Harmonic Distortion vs. Differential Output Voltage

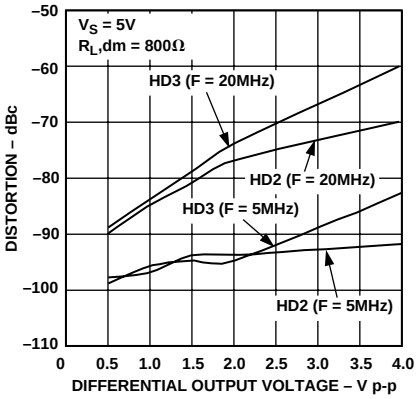


Figure 11. Harmonic Distortion vs. Differential Output Voltage

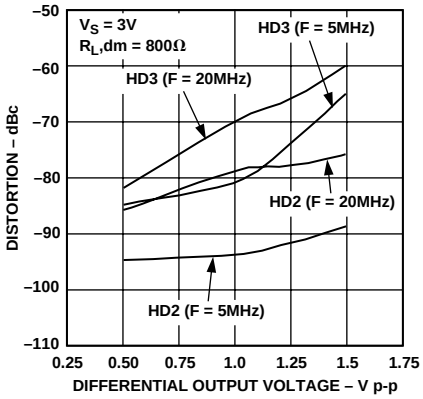


Figure 12. Harmonic Distortion vs. Differential Output Voltage

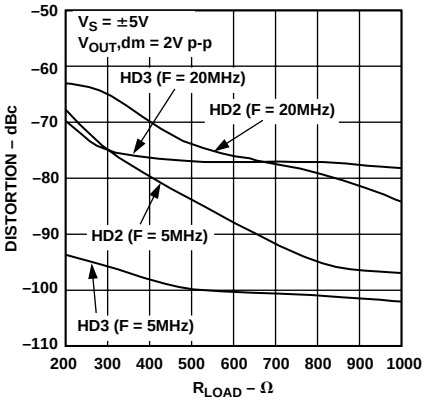


Figure 13. Harmonic Distortion vs. R_{LOAD}

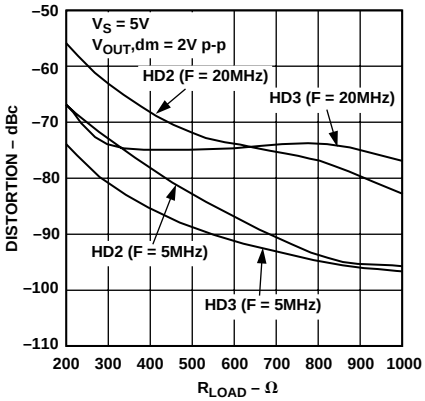


Figure 14. Harmonic Distortion vs. R_{LOAD}

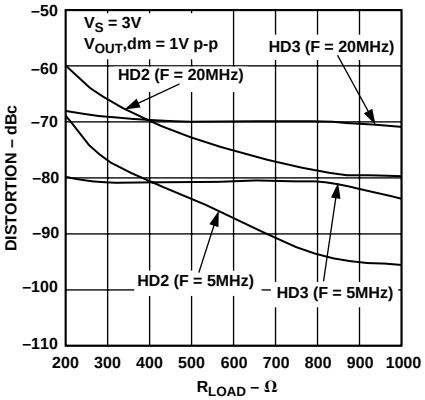


Figure 15. Harmonic Distortion vs. R_{LOAD}

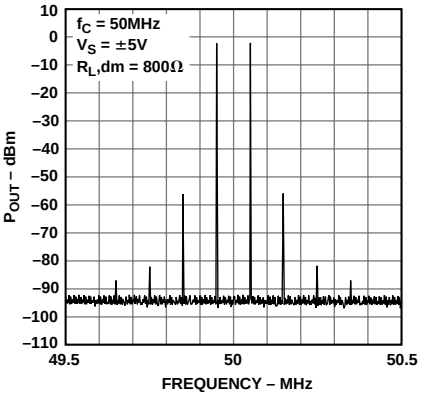


Figure 16. Intermodulation Distortion

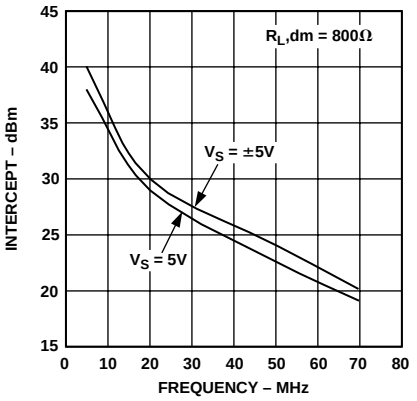


Figure 17. Third Order Intercept vs. Frequency

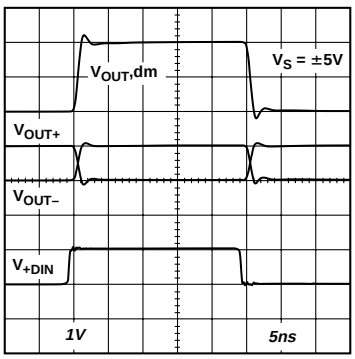


Figure 18. Large Signal Transient Response

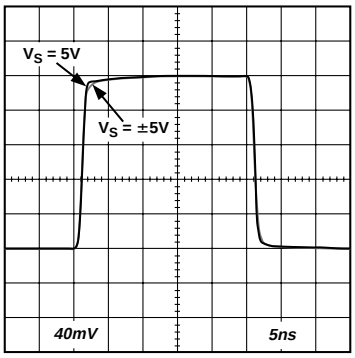


Figure 19. Small Signal Transient Response

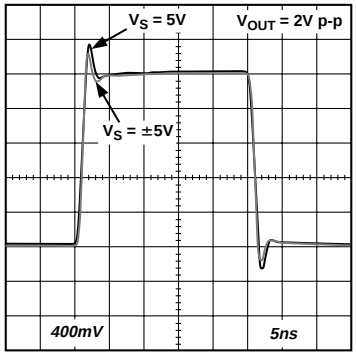


Figure 20. Large Signal Transient Response

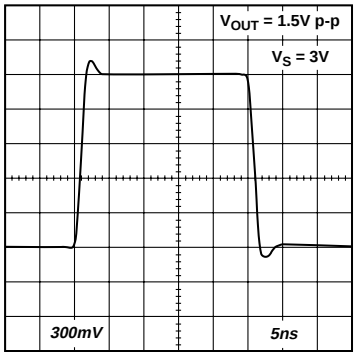


Figure 21. Large Signal Transient Response

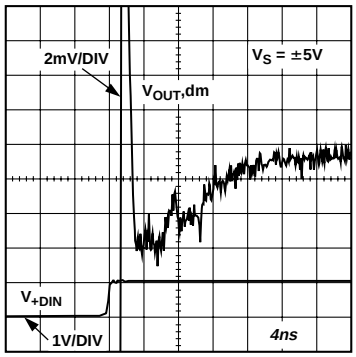


Figure 22. 0.1% Settling Time

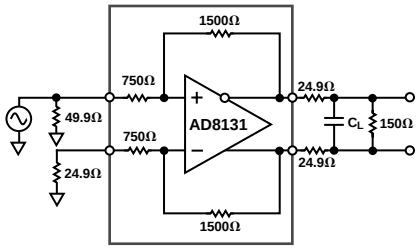


Figure 23. Capacitor Load Drive Test Circuit

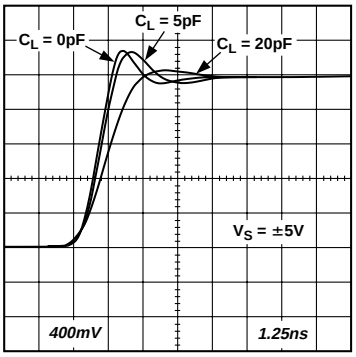


Figure 24. Large Signal Transient Response for Various Capacitor Loads

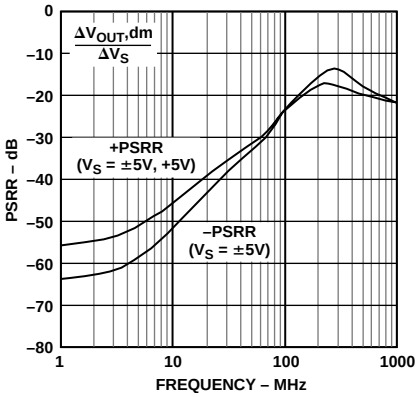


Figure 25. PSRR vs. Frequency

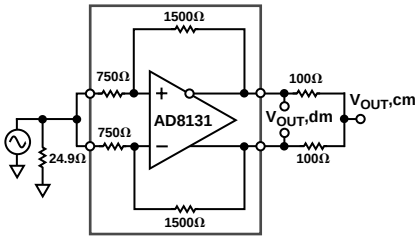


Figure 26. CMRR Test Circuit

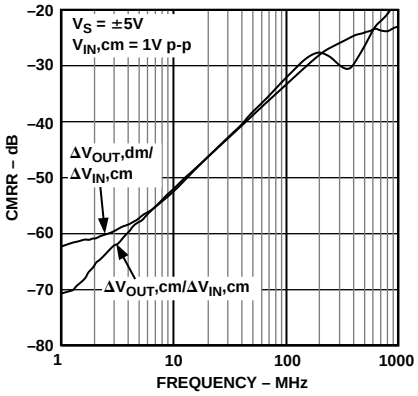


Figure 27. CMRR vs. Frequency

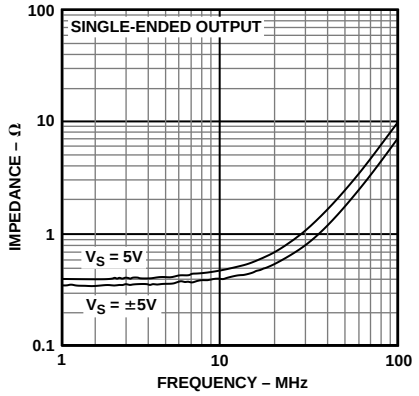


Figure 28. Single-Ended Z_{OUT} vs. Frequency

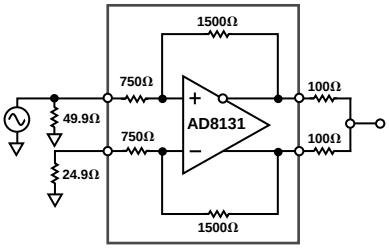


Figure 29. Output Balance Error Test Circuit

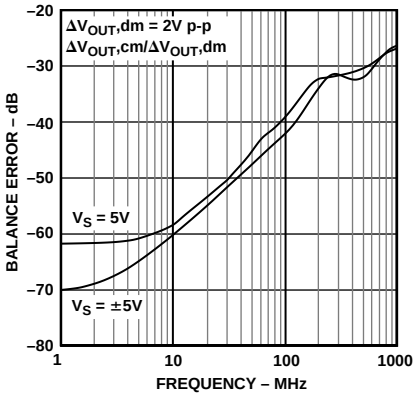


Figure 30. Output Balance Error vs. Frequency

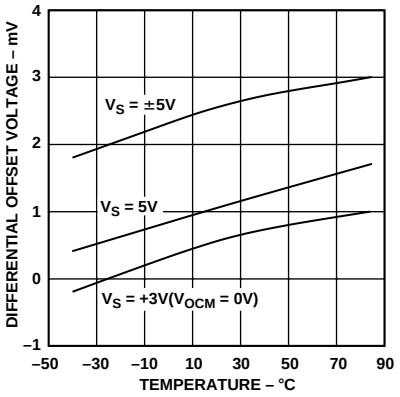


Figure 31. Output Offset Voltage vs. Temperature

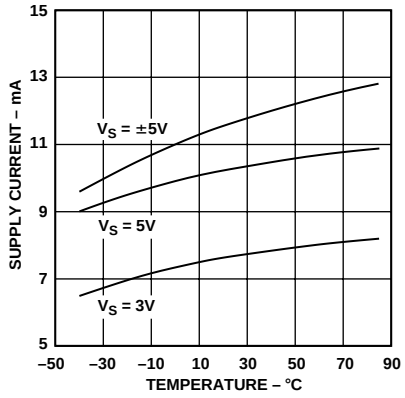


Figure 32. Quiescent Current vs. Temperature

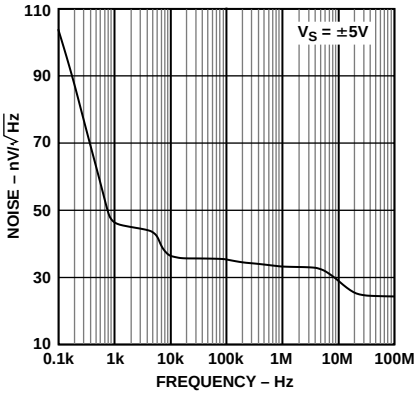


Figure 33. Voltage Noise vs. Frequency

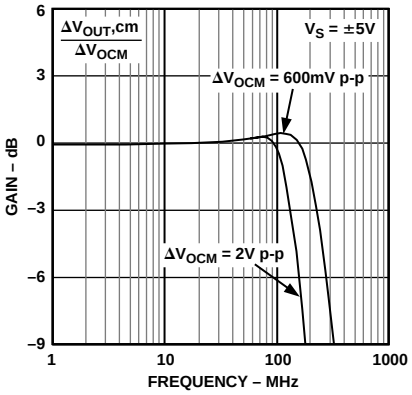


Figure 34. V_{OCM} Gain Response

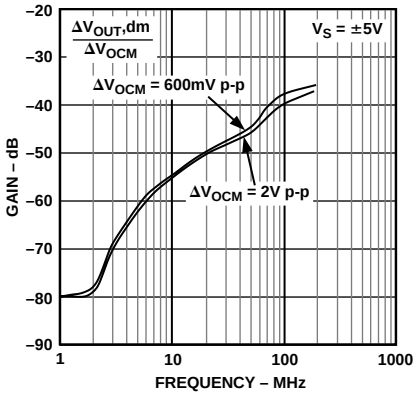


Figure 35. V_{OCM} CMRR vs. Frequency

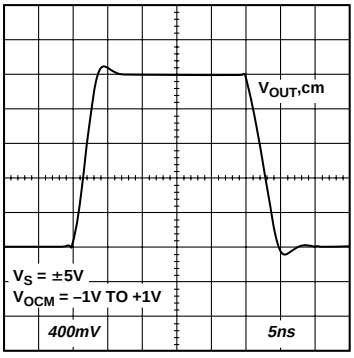


Figure 36. V_{OCM} Transient Response

OPERATIONAL DESCRIPTION

Definition of Terms

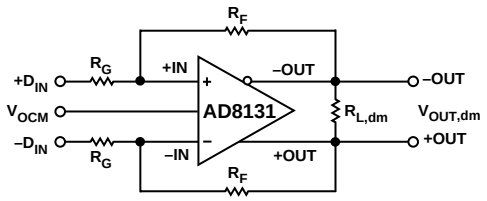


Figure 37. Circuit Definitions

Differential voltage refers to the difference between two node voltages. For example, the output differential voltage (or equivalently output differential-mode voltage) is defined as:

$$V_{OUT,dm} = (V_{+OUT} - V_{-OUT})$$

V_{+OUT} and V_{-OUT} refer to the voltages at the +OUT and –OUT terminals with respect to a common reference.

Common-mode voltage refers to the average of two node voltages. The output common-mode voltage is defined as:

$$V_{OUT,cm} = (V_{+OUT} + V_{-OUT})/2$$

Balance is a measure of how well differential signals are matched in amplitude and exactly 180 degrees apart in phase. Balance is most easily determined by placing a well-matched resistor divider between the differential voltage nodes and comparing the magnitude of the signal at the divider's midpoint with the magnitude of the differential signal. By this definition, output balance is the magnitude of the output common-mode voltage divided by the magnitude of the output differential-mode voltage:

$$Output\ Balance\ Error = \left| \frac{V_{OUT,cm}}{V_{OUT,dm}} \right|$$

THEORY OF OPERATION

The AD8131 differs from conventional op amps in that it has two outputs whose voltages move in opposite directions. Like an op amp, it relies on high open-loop gain and negative feedback to force these outputs to the desired voltages. The AD8131 behaves much like a standard voltage feedback op amp and makes it easy to perform single-ended-to-differential conversion, common-mode level-shifting, and amplification of differential signals.

Previous differential drivers, both discrete and integrated designs, have been based on using two independent amplifiers, and two independent feedback loops, one to control each of the outputs. When these circuits are driven from a single-ended source, the resulting outputs are typically not well balanced. Achieving a balanced output has typically required exceptional matching of the amplifiers and feedback networks.

DC common-mode level-shifting has also been difficult with previous differential drivers. Level-shifting has required the use of a third amplifier and feedback loop to control the output common-mode level. Sometimes the third amplifier has also been used to attempt to correct an inherently unbalanced circuit. Excellent performance over a wide frequency range has proven difficult with this approach.

The AD8131 uses two feedback loops to separately control the differential and common-mode output voltages. The differential feedback, set by internal resistors, controls only the differential output voltage. The common-mode feedback controls only the common-mode output voltage. This architecture makes it easy to arbitrarily set the output common-mode level. It is forced, by internal common-mode feedback, to be equal to the voltage applied to the V_{OCM} input, without affecting the differential output voltage.

The AD8131 architecture results in outputs that are very highly balanced over a wide frequency range without requiring external components or adjustments. The common-mode feedback loop forces the signal component of the output common-mode voltage to be zeroed. The result is nearly perfectly balanced differential outputs, of identical amplitude and exactly 180 degrees apart in phase.

Analyzing an Application Circuit

The AD8131 uses high open-loop gain and negative feedback to force its differential and common-mode output voltages in such a way as to minimize the differential and common-mode error voltages. The differential error voltage is defined as the voltage between the differential inputs labeled +IN and –IN in Figure 37. For most purposes, this voltage can be assumed to be zero. Similarly, the difference between the actual output common-mode voltage and the voltage applied to V_{OCM} can also be assumed to be zero. Starting from these two assumptions, any application circuit can be analyzed.

Closed-Loop Gain

The differential mode gain of the circuit in Figure 37 can be determined to be described by the following equation:

$$\left| \frac{V_{OUT,dm}}{V_{IN,dm}} \right| = \frac{R_F}{R_G} = 2$$

where R_F = 1.5 kΩ and R_G = 750 Ω nominally.

Estimating the Output Noise Voltage

Similar to the case of a conventional op amp, the differential output errors (noise and offset voltages) can be estimated by multiplying the input referred terms, at +IN and –IN, by the circuit noise gain. The noise gain is defined as:

$$G_N = 1 + \left(\frac{R_F}{R_G} \right) = 3$$

The total output referred noise for the AD8131, including the contributions of R_F, R_G, and op amp, is nominally 25 nV/$\sqrt{\text{Hz}}$ at 20 MHz.

Calculating an Application Circuit's Input Impedance

The effective input impedance of a circuit such as that in Figure 37, at $+D_{IN}$ and $-D_{IN}$, will depend on whether the amplifier is being driven by a single-ended or differential signal source. For balanced differential input signals, the input impedance ($R_{IN,dm}$) between the inputs ($+D_{IN}$ and $-D_{IN}$) is simply:

$$R_{IN,dm} = 2 \times R_G = 1.5\ k\Omega$$

In the case of a single-ended input signal (for example if $-D_{IN}$ is grounded and the input signal is applied to $+D_{IN}$), the input impedance becomes:

$$R_{IN,dm} = \left(\frac{R_G}{1 - \frac{R_F}{2 \times \left(R_G + R_F\right)}} \right) = 1.125\,k\Omega$$

The circuit's input impedance is effectively higher than it would be for a conventional op amp connected as an inverter because a fraction of the differential output voltage appears at the inputs as a common-mode signal, partially bootstrapping the voltage across the input resistor R_G.

Input Common-Mode Voltage Range in Single Supply Applications

The AD8131 is optimized for level-shifting "ground" referenced input signals. For a single-ended input this would imply, for example, that the voltage at $-D_{IN}$ in Figure 37 would be zero volts when the amplifier's negative power supply voltage (at V–) was also set to zero volts.

Setting the Output Common-Mode Voltage

The AD8131's V_{OCM} pin is internally biased at a voltage approximately equal to the midsupply point (average value of the voltages on V+ and V–). Relying on this internal bias will result in an output common-mode voltage that is within about 25 mV of the expected value.

In cases where more accurate control of the output common-mode level is required, it is recommended that an external source, or resistor divider (made up of 10 kΩ resistors), be used.

Driving a Capacitive Load

A purely capacitive load can react with the pin and bondwire inductance of the AD8131 resulting in high frequency ringing in the pulse response. One way to minimize this effect is to place a small resistor in series with the amplifier's outputs as shown in Figure 23.

APPLICATIONS

Twisted-Pair Line Driver

The AD8131 has on-chip resistors that provide for a gain-of-two without any external parts. Several on-chip resistors are trimmed to ensure that the gain is accurate, the common-mode rejection is good, and the output is well balanced. This makes the AD8131 very suitable as a single-ended-to-differential twisted-pair line driver.

Figure 38 shows a circuit of an AD8131 driving a twisted-pair line, like a Category 3 or Category 5 (Cat3 or Cat5), that are already installed in many buildings for telephony and data communications. The characteristic impedance of such transmission lines is usually about 100 Ω. The outstanding balance of the AD8131 output will minimize the common-mode signal and therefore the amount of EMI generated by driving the twisted pair.

The two resistors in series with each output terminate the line at the transmit end. Since the impedances of the outputs of the AD8131 are very low, they can be thought of as a short circuit, and the two terminating resistors form a 100 Ω termination at the transmit end of the transmission line. The receive end is directly terminated by a 100 Ω resistor across the line.

This back-termination of the transmission line divides the output signal by two. The fixed gain of two of the AD8131 will create a net unity gain for the system from end to end.

In this case, the input signal is provided by a signal generator with an output impedance of 50 Ω. This is terminated with a 49.9 Ω resistor near $+D_{IN}$ of the AD8131. The effective parallel resistance of the source and termination is 25 Ω. The 24.9 Ω resistor from $-D_{IN}$ to ground matches the $+D_{IN}$ source impedance and minimizes any dc and gain errors.

If $+D_{IN}$ is driven by a low-impedance source over a short distance, such as the output of an op amp, then no termination resistor is required at $+D_{IN}$. In this case, the $-D_{IN}$ can be directly tied to ground.

+3 V Supply Differential A-to-D Driver

Many newer A-to-D converters can run from a single +3 V supply, which can save significant system power. In order to increase the dynamic range at the analog input, they have differential inputs, which doubles the dynamic range with respect to a single-ended input. An added benefit of using a differential input is that the distortion can be improved.

The low distortion and ability to run from a single +3 V supply make the AD8131 suited as an A-to-D driver for some 10-bit, single supply applications. Figure 39 shows a schematic for a circuit for an AD8131 driving an AD9203, a 10-bit, 40 MSPS A-to-D converter.

The common mode of the AD8131 output is set at midsupply by the voltage divider connected to V_{OCM}, and ac bypassed with a 0.1 μF capacitor. This provides for maximum dynamic range between the supplies at the output of the AD8131. The 110 Ω resistors at the AD8131 output, along with the shunt capacitors form a one pole, low-pass filter for lowering noise and antialiasing.

Figure 40 shows an FFT plot that was taken from the combined devices at an analog input frequency of 2.5 MHz and a 40 MSPS sampling rate. The performance of the AD8131 compares very favorably with a center-tapped transformer drive, which has typically been the best way to drive this A-to-D converter. The AD8131 has the advantage of maintaining dc performance, which a transformer solution cannot provide.

Unity-Gain, Single-Ended-to-Differential Driver

If it is not necessary to offset the output common-mode voltage (via the V_{OCM} pin), then the AD8131 can make a simple unity-gain single-ended-to-differential amplifier that does not require any external components. Figure 41 shows the schematic for this circuit.

Referring to Figure 2, when $-D_{IN}$ is left floating, there is 100 percent feedback of +OUT to –IN via the internal feedback resistor. This contrasts with the typical gain-of-two operation where $-D_{IN}$ is grounded and one third of the +OUT is fed back to –IN. The result is a closed-loop differential gain of one.

Upon careful observation, it can be seen that only $+D_{IN}$ and V_{OCM} are referenced to ground. It is the case that the ground voltage at V_{OCM} is the reference for this circuit. In this unity gain configuration, if a dc voltage is applied to V_{OCM} to shift the common-mode voltage, a differential dc voltage will be created at the output, along with the common-mode voltage change. Thus, this configuration cannot be used when it is desired to offset the common-mode voltage of the output with respect to the input at $+D_{IN}$.

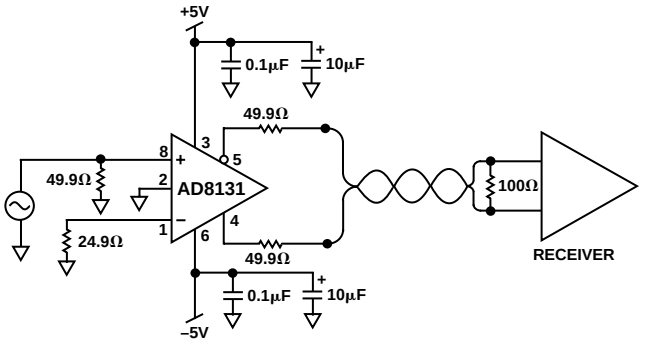


Figure 38. Single-Ended-to-Differential 100 Ω Line Driver

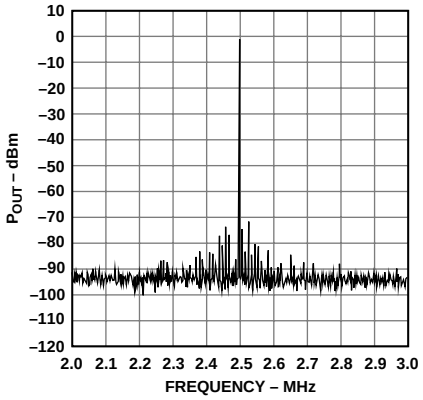


Figure 40. FFT Plot for AD8131/AD9203

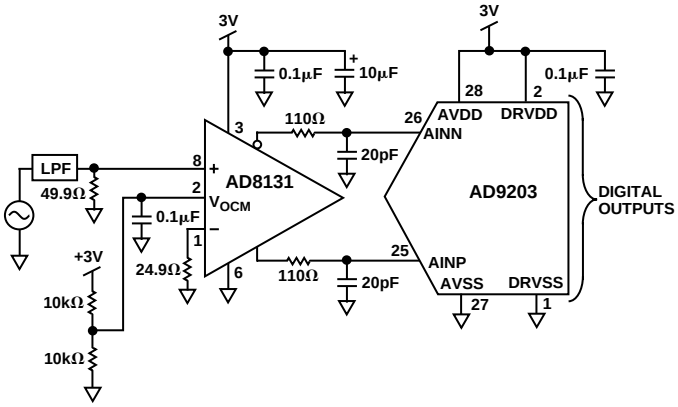


Figure 39. Test Circuit for AD8131 Driving an AD9203, 10 Bit, 40 Msps A-to-D Converter

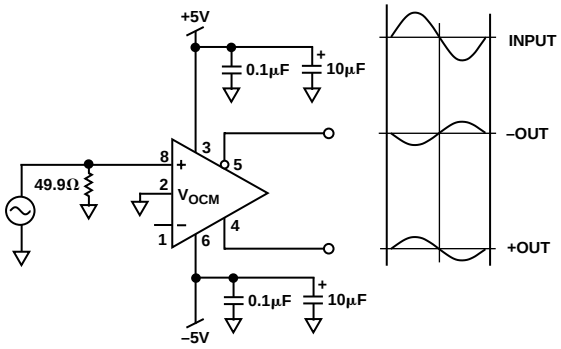
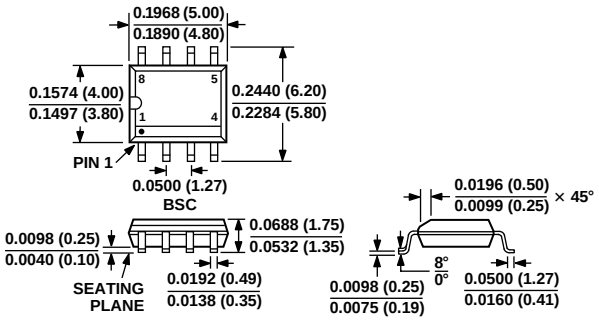


Figure 41. Unity Gain, Single-Ended-to-Differential Amplifier

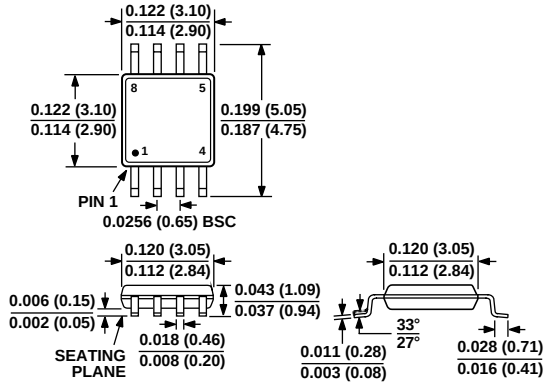
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

8-Lead SOIC
(SO-8)



8-Lead μSOIC
(RM-8)



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