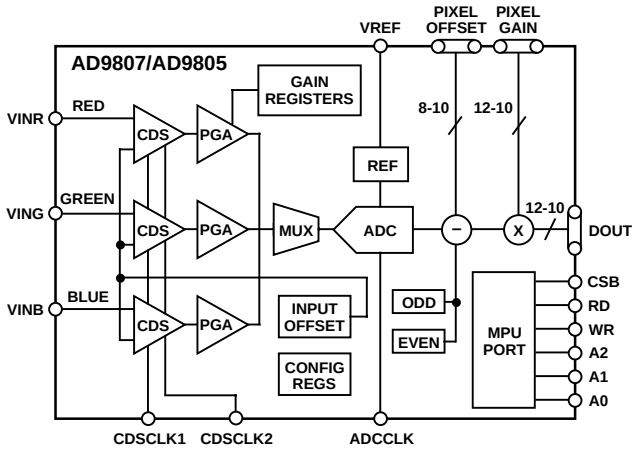
Complete 12-Bit/10-Bit 6 MSPS CCD/CIS Signal Processors

AD9807/AD9805

FEATURES

Pin Compatible 12-Bit and 10-Bit Versions
12-Bit/10-Bit 6 MSPS A/D Converter
Integrated Triple Correlated Double Sampler
3-Channel, 2 MSPS Color Mode
1× – 4× Analog Programmable Gain Amplifier
Pixel-Rate Digital Gain Adjustment
Pixel-Rate Digital Offset Adjustment
Internal Voltage Reference
No Missing Codes Guaranteed
Microprocessor-Compatible Control Interface
+3.3 V/+5 V Digital I/O Compatibility
Low Power CMOS: 500 mW
64-Pin PQFP Surface Mount Package

FUNCTIONAL BLOCK DIAGRAM



PRODUCTION DESCRIPTION

The AD9807 and AD9805 are complete CCD/CIS imaging decoders and signal processors on a single monolithic integrated circuit. The input of the AD9807/AD9805 allows direct ac coupling of the charge-coupled device (CCD) or contact image sensor (CIS) output(s). The AD9807/AD9805 includes all the circuitry to perform three-channel correlated double sampling (CDS) and programmable gain adjustment of the CCD output; a 12-bit or 10-bit analog-to-digital converter (ADC) quantizes the analog signal. After digitization, the on-board digital signal processor (DSP) circuitry allows pixel rate offset and gain correction. The DSP also corrects odd/even CCD register imbalance errors. A parallel control bus provides a simple interface to 8-bit microcontrollers. The AD9807/AD9805 comes in a space saving 64-pin plastic quad flatpack (PQFP) and is specified over the commercial (0°C to +70°C) temperature range. By disabling the CDS, the AD9807/AD9805 are also suitable for non-CCD applications, or applications that do not require CDS, such as CIS signal processing.

PRODUCT HIGHLIGHTS

The AD9807/AD9805 offers a complete, single chip CCD imaging front end in a 64-pin plastic quad flatpack (PQFP).

On-Chip PGA—The AD9807/AD9805 includes a 3-channel analog programmable gain amplifier; it is programmable from 1× to 4× in 16 increments.

On-Chip CDS—An integrated 3-channel correlated double sampler allows easy ac coupling directly from the CCD sensor outputs. Additionally, the CDS reduces low frequency noise and reset feedthrough.

On-Chip Voltage Reference—The AD9807/AD9805 includes a 2 V bandgap reference that allows the input range of the device to be configured for input spans up to 4 V.

6 MSPS A/D Converter—A highly linear 12-bit or 10-bit A/D converter sequentially digitizes the red, green and blue CDS outputs ensuring no missing code performance. The user may also configure the AD9807/AD9805 for single channel operation.

Digital Gain & Offset Correction—Pixel rate digital gain and offset correction blocks allow precise repeatable correction of imaging system error sources.

Digital I/O Compatibility—The AD9807/AD9805 offers +3.3 V/+5 V logic level compatibility.

Pin-Compatible 12-Bit and 10-Bit Versions—The AD9807 is also offered in a pin-compatible 10-bit version, the AD9805, allowing upgrade-ability and simplifying design issues across different scanner models.

REV. 0

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AD9807–SPECIFICATIONS

ANALOG SPECIFICATIONS

(T_{MIN} to T_{MAX} with AV_{DD} = +5.0 V, DV_{DD} = +5.0 V, f_{ADCCLK} = 6 MSPS, $f_{CDSCLK1}$ = 2 MSPS, $f_{CDSCLK2}$ = 2 MSPS, PGA Gain = 1 unless otherwise noted)

Parameter	Min	Typ	Max	Units
RESOLUTION	12			Bits
CONVERSION RATE				
3-Channel Mode With CDS		6		MSPS
1-Channel Mode With CDS[1]		6		MSPS
DC ACCURACY				
Integral Nonlinearity (INL)[2]		1.5		LSB
Differential Nonlinearity (DNL)[2]		0.4	0.75	LSB
No Missing Codes	12			Bits Guaranteed
Unipolar Offset Error (@ +25°C)			0.4	% FSR
Gain Error (@ +25°C)			1.2	% FSR
ANALOG INPUTS				
Full-Scale Input Span	0.0625		4	V p-p
Input Limits[3]	AV_{SS} – 0.3 V		AV_{DD} + 0.3	V
Input Capacitance		10		pF
Input Bias Current		0.01		µA
Input Referred Noise		0.3		LSB rms
PSRR (AV_{DD} = +5 V ± 0.25 V)		0.06		% FSR
INTERNAL VOLTAGE REFERENCE				
1 V Output Tolerance (@+25°C)			±15	mV
2 V Output Tolerance (@+25°C)			±30	mV
POWER SUPPLIES				
Operating Voltages				
AV_{DD}	+4.75		+5.25	V
DV_{DD}	+4.75		+5.25	V
Operating Current				
AV_{DD}		73	86	mA
DV_{DD}		16.6	20	mA
POWER CONSUMPTION		450	530	mW
TEMPERATURE RANGE				
Operating	0		+70	°C

NOTES
[1]Blue and green channels. Red channel conversion rate for 1-channel mode is 5 MSPS.
[2]Measured with 4 V p-p input range.
[3]Input signals exceeding these limits are subject to excessive overvoltage recovery times.
Specifications subject to change without notice.

DIGITAL SPECIFICATIONS

(T_{MIN} to T_{MAX} with AV_{DD} = +5.0 V, DV_{DD} = +5.0 V, f_{ADCCLK} = 6 MSPS, $f_{CDSCLK1}$ = 2 MSPS, $f_{CDSCLK2}$ = 2 MSPS, C_L = 20 pF, unless otherwise noted)

Parameter	Symbol	Min	Typ	Max	Units
LOGIC INPUTS					
High Level Input Voltage	V_{IH}	2.0			V
Low Level Input Voltage	V_{IL}			0.8	V
High Level Input Current	I_{IH}		10		µA
Low Level Input Current	I_{IL}		10		µA
Input Capacitance	C_{IN}		10		pF
LOGIC OUTPUTS					
High Level Output Voltage (I_{OH} = 50 µA)	V_{OH}	4.5	4.9		V
High Level Output Voltage (I_{OH} = 0.5 mA)	V_{OH}	2.4			V
Low Level Output Voltage (I_{OL} = 50 µA)	V_{OL}			0.1	V
Low Level Output Voltage (I_{OL} = –0.6 mA)	V_{OL}			0.4	V
Output Capacitance	C_{OUT}		5		pF

Specifications subject to change without notice.

ANALOG SPECIFICATIONS

(T_{MIN} to T_{MAX} with AV_{DD} = +5.0 V, DV_{DD} = +5.0 V, f_{ADCCLK} = 6 MSPS, $f_{CDSCLK1}$ = 2 MSPS, $f_{CDSCLK2}$ = 2 MSPS, PGA Gain = 1 unless otherwise noted)

Parameter	Min	Typ	Max	Units
RESOLUTION	10			Bits
CONVERSION RATE				
3-Channel Mode With CDS		6		MSPS
1-Channel Mode With CDS[1]		6		MSPS
DC ACCURACY				
Integral Nonlinearity (INL)[2]			1.0	LSB
Differential Nonlinearity (DNL)[2]			0.5	LSB
No Missing Codes	10			Bits Guaranteed
Unipolar Offset Error (@ +25°C)			0.6	% FSR
Gain Error (@ +25°C)			1.2	% FSR
ANALOG INPUTS				
Full-Scale Input Span	0.0625		4	V p-p
Input Limits[3]	AV_{SS} – 0.3 V		AV_{DD} + 0.3	V
Input Capacitance		10		pF
Input Bias Current		0.01		µA
Input Referred Noise		0.1		LSB rms
PSRR (AV_{DD} = +5 V ± 0.25 V)		0.06		% FSR
INTERNAL VOLTAGE REFERENCE				
1 V Output Tolerance (@ +25°C)			±15	mV
2 V Output Tolerance (@ +25°C)			±30	mV
POWER SUPPLIES				
Operating Voltages				
AV_{DD}	+4.75		+5.25	V
DV_{DD}	+4.75		+5.25	V
Operating Current				
AV_{DD}		73	86	mA
DV_{DD}		16.6	20	mA
POWER CONSUMPTION		450	530	mW
TEMPERATURE RANGE				
Operating	0		+70	°C

NOTES
[1]Blue and green channels. Red channel conversion rate for 1-channel mode is 5 MSPS.
[2]Measured with 4 V p-p input range.
[3]Input signals exceeding these limits are subject to excessive overvoltage recovery times.

Specifications subject to change without notice.

DIGITAL SPECIFICATIONS

(T_{MIN} to T_{MAX} with AV_{DD} = +5.0 V, DV_{DD} = +5.0 V, f_{ADCCLK} = 6 MSPS, $f_{CDSCLK1}$ = 2 MSPS, $f_{CDSCLK2}$ = 2 MSPS, C_L = 20 pF, unless otherwise noted)

Parameter	Symbol	Min	Typ	Max	Units
LOGIC INPUTS					
High Level Input Voltage	V_{IH}	2.0			V
Low Level Input Voltage	V_{IL}			0.8	V
High Level Input Current	I_{IH}		10		µA
Low Level Input Current	I_{IL}		10		µA
Input Capacitance	C_{IN}		10		pF
LOGIC OUTPUTS					
High Level Output Voltage (I_{OH} = 50 µA)	V_{OH}	4.5	4.9		V
High Level Output Voltage (I_{OH} = 0.5 mA)	V_{OH}	2.4			V
Low Level Output Voltage (I_{OL} = 50 µA)	V_{OL}			0.1	V
Low Level Output Voltage (I_{OL} = –0.6 mA)	V_{OL}			0.4	V
Output Capacitance	C_{OUT}		5		pF

Specifications subject to change without notice.

TIMING SPECIFICATIONS (T_{MIN} to T_{MAX} with AV_{DD} = +5.0 V, DV_{DD} = +5.0 V, unless otherwise noted)

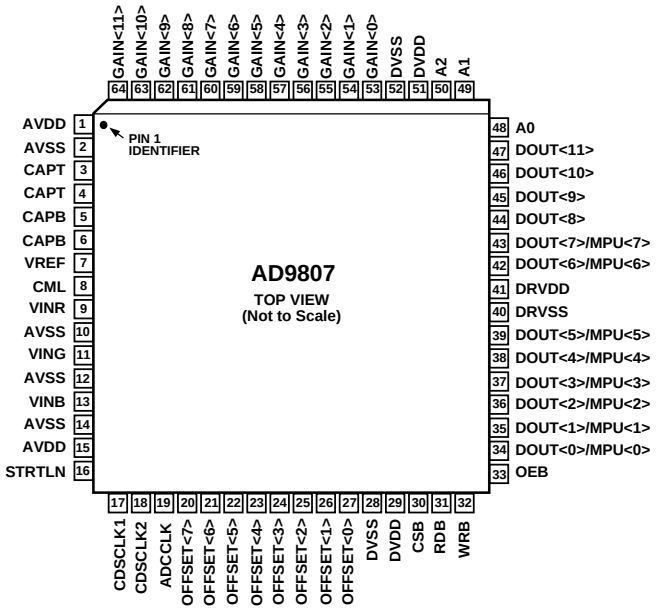
Parameter	Symbol	Min	Typ	Max	Units
CLOCK PARAMETERS					
3-Channel Conversion Rate	t_{CRA}	500			ns
1-Channel Conversion Rate	t_{CRB}	166			ns
CDSCK1 Pulse Width	t_{C1A}	30			ns
CDSCK1 Pulse Width	t_{C1B}	30			ns
CDSCK2 Pulse Width	t_{C2A}	30			ns
CDSCK2 Pulse Width	t_{C2B}	30			ns
CDS Clocks Digital Quiet Time	t_{Q}	20			ns
CDSCK2 Falling to CDSCK1 Rising	t_{C2C1A}	80			ns
CDSCK2 Falling to CDSCK1 Rising	t_{C2C1B}	40			ns
CDSCK1 Falling to CDSCK2 Rising	t_{C1C2A}	20			ns
CDSCK1 Falling to CDSCK2 Rising	t_{C1C2B}	20			ns
ADCCLK Rising to CDSCK1 Falling	t_{C1AD}	35			ns
ADCCLK Pulse Width	t_{ACLK}	50			ns
ADCCLK Period	t_{CP}	166			ns
ADCCLK Period (Red Single Channel Mode)	t_{CP2}	200			ns
3-Channel Settling Time	t_{STL1}	60			ns
1-Channel Settling Time (B and G Only)	t_{STL2}	30			ns
ADCCLK Rising to Control Data Setup	t_{GOS}	15			ns
ADCCLK Rising to Control Data Hold	t_{GOH}	15			ns
STRTLN Rising, Falling Setup	t_{S}	15			ns
STRTLN Rising, Falling Hold	t_{H}	15			ns
Aperture Delay	t_{AD}	10			ns
REGISTER WRITE/READ					
Address Setup Time	t_{AS}	15			ns
Address Hold Time	t_{AH}	15			ns
Data Setup Time	t_{DS}	15			ns
Data Hold Time	t_{DH}	15			ns
Chip Select Setup Time	t_{CSS}	15			ns
Chip Select Hold Time	t_{CSH}	15			ns
Write Pulse Width	t_{PWW}	25			ns
Read Pulse Width	t_{PWR}	50			ns
Read To Data Valid	t_{DD}	40			ns
DATA OUTPUT					
Output Delay	t_{OD}		15		ns
3-State to Data Valid	t_{EDV}	15			ns
Output Enable High to 3-State	t_{HZ}	5			ns
Latency			6		ADCCLK Cycles

Table I. Output Controls

CSB	0	0	0	0	0	0	1	1
RDB	0	0	1	1	1	1	x	x
WRB	0	1	0	0	1	1	x	x
OEB	x	x	0	1	0	1	0	1
DOUT	X	Q MPU	X	D MPU	X	Z	Q ADC	Z

LEGEND:
x = Don't Care
X = Unknown (Not Recommended)
Q = Outputs
D = Inputs
Z = 3-State

PIN CONFIGURATION

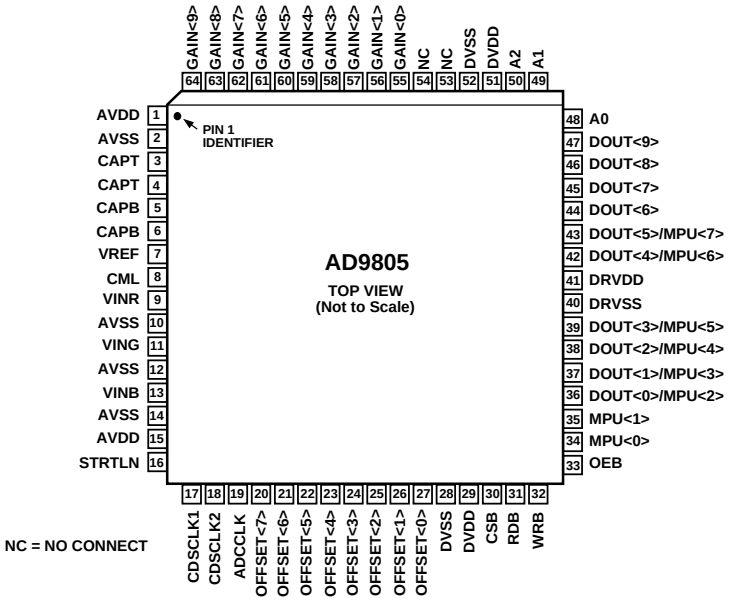


PIN DESCRIPTIONS

Pin No.	Pin Name	Type	Description
1, 15	AVDD	P	+5 V Analog Supply.
2, 10, 12, 14	AVSS	P	Analog Ground.
3, 4	CAPT	AO	Reference Decoupling. See Figure 22.
5, 6	CAPB	AO	Reference Decoupling.
7	VREF	AO	Internal Reference Output. Decouple with 10 µF + 0.1 µF.
8	CML	AO	Internal Bias Voltage. Decouple with 0.1 µF.
9	VINR	AI	Analog Input, Red.
11	VING	AI	Analog Input, Green.
13	VINB	AI	Analog Input, Blue.
16	STRTLN	DI	STRTLN. Indicates beginning of scan line.
17	CDSCLK1	DI	CDS Reset Clock Pulse Input.
18	CDSCLK2	DI	CDS Data Clock Pulse Input.
19	ADCCLK	DI	A/D Sample Clock Input.
28, 52	DVSS	P	Digital Ground.
29, 51	DVDD	P	+5 V Digital Supply.
20	OFFSET<7>	DI	Pixel Rate Offset Coefficient Inputs. Most Significant Bit.
21–26	OFFSET<6:1>	DI	Pixel Rate Offset Coefficient Inputs.
27	OFFSET<0>	DI	Pixel Rate Offset Coefficient Inputs. Least Significant Bit.
30	CSB	DI	Chip Select. Active Low.
31	RDB	DI	Read Strobe. Active Low.
32	WRB	DI	Write Strobe. Active Low.
33	OEB	DI	Output Enable. Active Low.
34	DOUT<0>/MPU<0>	DIO	Data Output LSB/Register Input LSB
35–39, 42	DOUT<1:6>/MPU<1:6>	DIO	Data Outputs/Register Inputs.
40	DRVSS	P	Digital Driver Ground
41	DRVDD	P	Digital Driver Supply
43	DOUT<7>/MPU<7>	DIO	Data Output/Register Input MSB.
44–46	DOUT<8:10>	DO	Data Outputs.
47	DOUT<11>	DO	Data Output MSB.
48, 49, 50	A0, A1, A2	DI	Register Select Pins.
53	GAIN<0>	DI	Pixel Rate Gain Coefficient Input. LSB.
54–63	GAIN<1:10>	DI	Pixel Rate Gain Coefficient Inputs.
64	GAIN<11>	DI	Pixel Rate Gain Coefficient Input. MSB.

TYPE: AI = Analog Input; AO = Analog Output; DI = Digital Input; DO = Digital Output; DIO = Digital Input/Output; P = Power.

PIN CONFIGURATION



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1, 15	AVDD	P	+5 V Analog Supply.
2, 10, 12, 14	AVSS	P	Analog Ground.
3, 4	CAPT	AO	Reference Decoupling. See Figure 22.
5, 6	CAPB	AO	Reference Decoupling.
7	VREF	AO	Internal Reference Output. Decouple with 10 μF + 0.1 μF.
8	CML	AO	Internal Bias Voltage. Decouple with 0.1 μF.
9	VINR	AI	Analog Input, Red.
11	VING	AI	Analog Input, Green.
13	VINB	AI	Analog Input, Blue.
16	STRTLN	DI	STRTLN. Indicates beginning of scan line.
17	CDSCLK1	DI	CDS Reset Clock Pulse Input.
18	CDSCLK2	DI	CDS Data Clock Pulse Input.
19	ADCCLK	DI	A/D Sample Clock Input.
28, 52	DVSS	P	Digital Ground.
29, 51	DVDD	P	+5 V Digital Supply.
20	OFFSET<7>	DI	Pixel Rate Offset Coefficient Inputs. Most Significant Bit.
21–26	OFFSET<6:1>	DI	Pixel Rate Offset Coefficient Inputs.
27	OFFSET<0>	DI	Pixel Rate Offset Coefficient Inputs. Least Significant Bit.
30	CSB	DI	Chip Select. Active Low.
31	RDB	DI	Read Strobe. Active Low.
32	WRB	DI	Write Strobe. Active Low.
33	OEB	DI	Output Enable. Active Low.
34	MPU<0>	DIO	Register Input-Output LSB.
35	MPU<1>	DIO	Register Input-Output.
36	DOUT<0>/MPU<2>	DIO	Data Output LSB/Register Input-Output.
37–39, 42	DOUT<1:4>/MPU<3:6>	DIO	Data Output/Register Input-Output.
40	DRVSS	P	Digital Driver Ground.
41	DRVDD	P	Digital Driver Supply.
43	DOUT<5>/MPU<7>	DIO	Data Output/Register Input-Output MSB.
44–46	DOUT<6:8>	DO	Data Outputs.
47	DOUT<9>	DO	Data Output MSB.
48, 49, 50	A0, A1, A2	DI	Register Select Pins.
53, 54	NC		No Connection.
55	GAIN<0>	DI	Pixel Rate Gain Coefficient Input LSB.
56–63	GAIN<1:8>	DI	Pixel Rate Gain Coefficient Inputs.
64	GAIN<9>	DI	Pixel Rate Gain Coefficient Input MSB.

TYPE: AI = Analog Input; AO = Analog Output; DI = Digital Input; DO = Digital Output; DIO = Digital Input/Output; P = Power.

ABSOLUTE MAXIMUM RATINGS*

Parameter	With Respect to	Min	Max	Units
AVDD	AVSS	–0.5	+6.5	Volts
AVSS	AVDD	–6.5	+0.5	Volts
DVDD	DVSS	–0.5	+6.5	Volts
AGND	DVSS	–0.3	+0.3	Volts
AVDD	DVDD	–6.5	+6.5	Volts
Clock Input	DVSS	–0.5	DVDD + 0.5	Volts
Digital Outputs	DVSS	–0.5	AVDD + 0.3	Volts
AIN, VREF	AVSS	–0.3	AVDD + 0.3	Volts
Junction Temperature			+150	°C
Storage Temperature		–65	+150	°C
Lead Temperature (10 sec)			+300	°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option*
AD9807JS	0°C to +70°C	PQFP	S-64
AD9805JS	0°C to +70°C	PQFP	S-64

*S = Plastic Quad Flatpack.

DEFINITIONS OF SPECIFICATIONS

INTEGRAL NONLINEARITY

Linearity error refers to the deviation of each individual code from a line drawn from "negative full scale" through "positive full scale." The point used as "negative full scale" occurs 1/2 LSB before the first code transition. "Positive full scale" is defined as a level 1 1/2 LSB beyond the last code transition. The deviation is measured from the middle of each particular code to the true straight line.

DIFFERENTIAL LINEARITY ERROR (DNL, NO MISSING CODES)

An ideal ADC exhibits code transitions that are exactly 1 LSB apart. DNL is the deviation from this ideal value. Thus every code must have a finite width. Guaranteed no missing codes to 12-bit resolution indicates that all 4096 codes, respectively, must be present over all operating ranges.

UNIPOLAR OFFSET ERROR

In the unipolar mode, the first transition should occur at a level 1/2 LSB above analog common. Unipolar offset is defined as the deviation of the actual from that point. The unipolar offset temperature coefficient specifies the maximum change of the transition point over temperature, with or without external adjustments.

GAIN ERROR

The last transition should occur for an analog value 1 1/2 LSB below the nominal full scale. Gain error is the deviation of the actual difference between first and last code transitions and the ideal difference between first and last code transitions.

POWER SUPPLY REJECTION

Power Supply Rejection specifies the maximum full-scale change from the initial value with the supplies at the various limits.

APERTURE DELAY

Aperture delay is a timing measurement between the sampling clocks and the CDS. It is measured from the falling edge of the CDSCLK2 input to when the input signal is held for conversion in CDS mode. In non-CDS mode, it is the falling edge of CDSCLK1.

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD9807/AD9805 feature proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

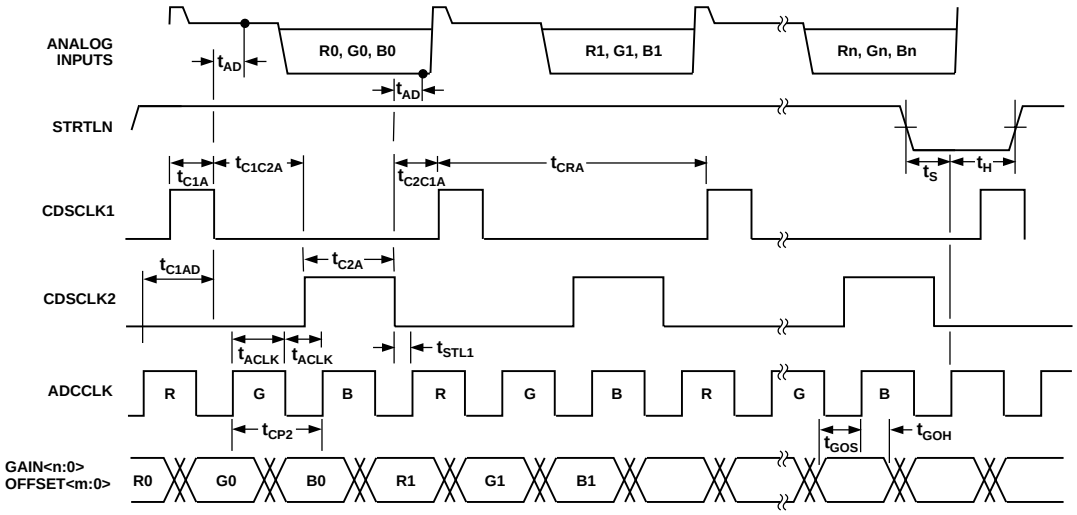


Figure 1a. 3-Channel CDS-Mode Clock Timing

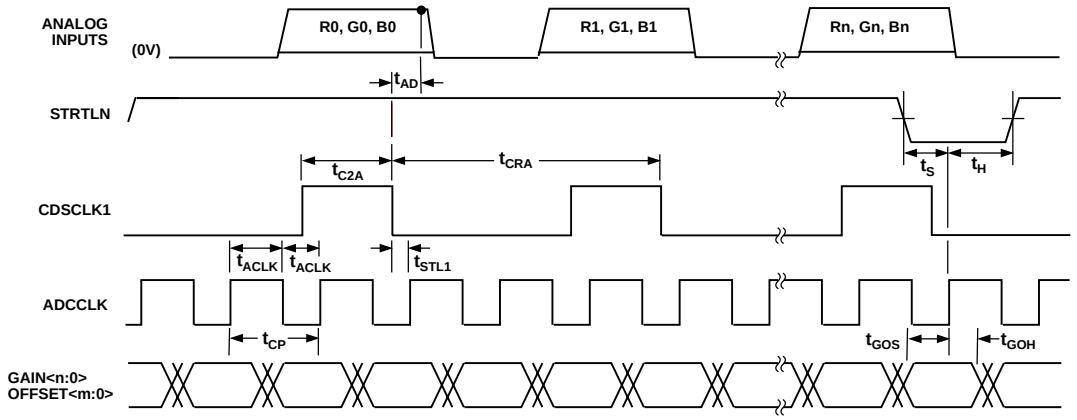


Figure 1b. 3-Channel SHA-Mode Clock Timing

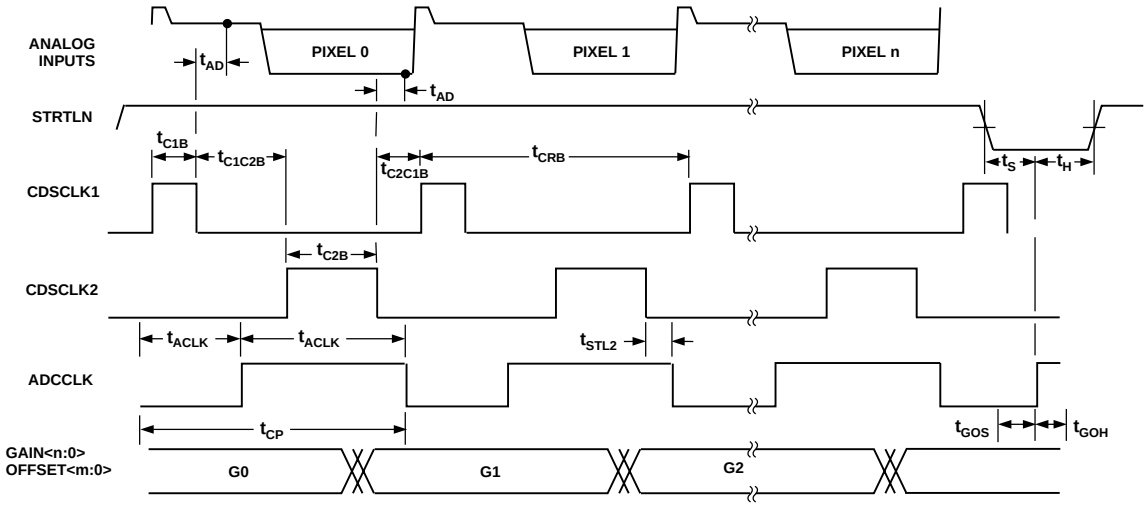


Figure 1c. 1-Channel CDS-Mode Clock Timing (for B and G Only)

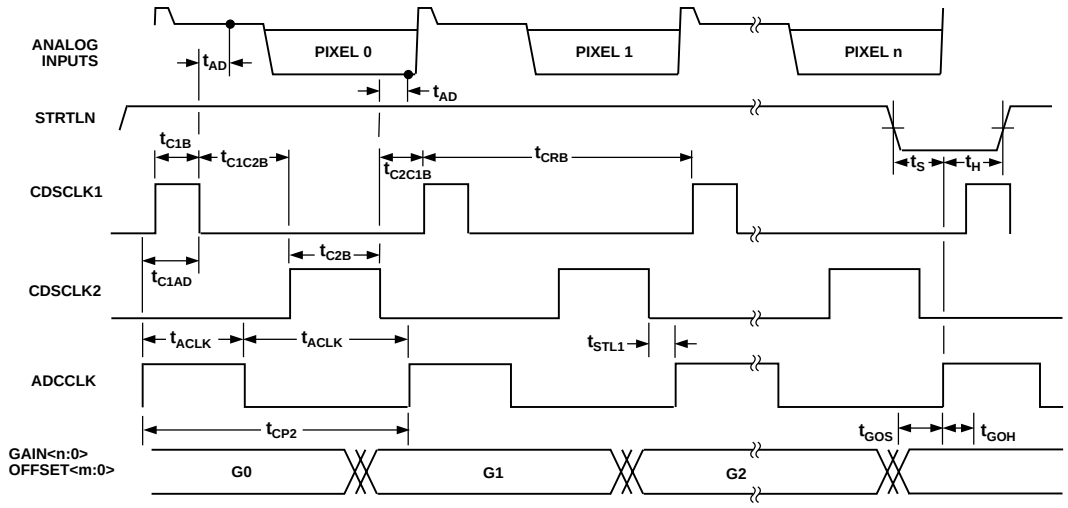


Figure 1d. 1-Channel CDS-Mode Clock Timing (Red Channel)

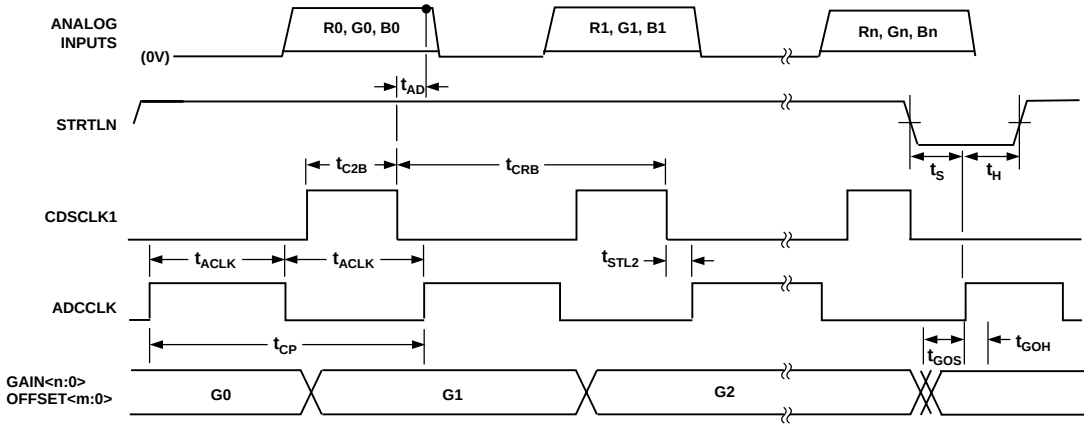


Figure 1e. 1-Channel SHA-Mode Clock Timing (for Blue and Green Channels)

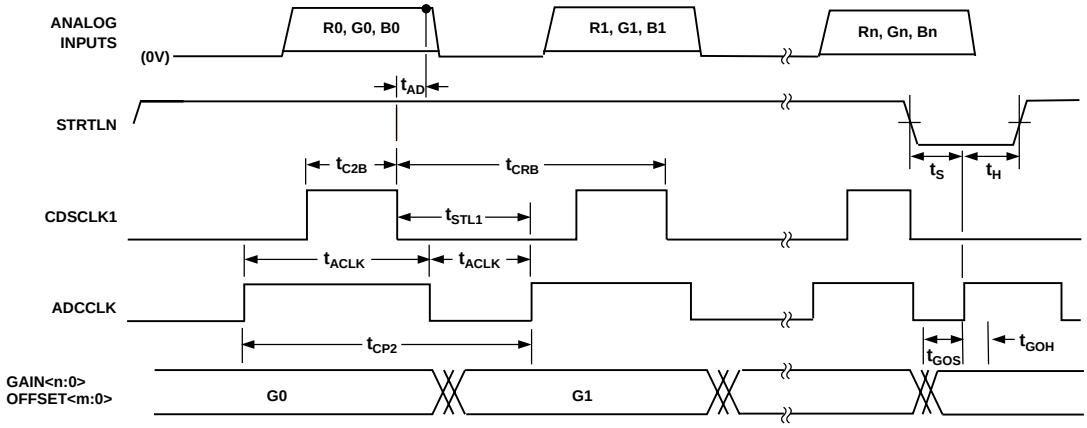


Figure 1f. 1-Channel SHA-Mode Clock Timing (Red Channel)

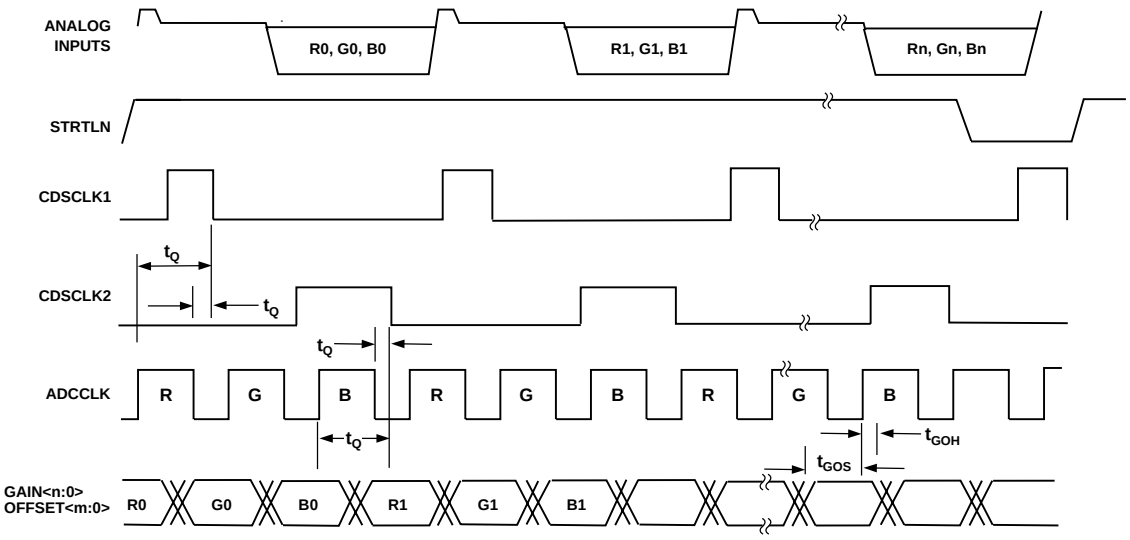


Figure 1g. CDS Clocks Digital Quiet Time

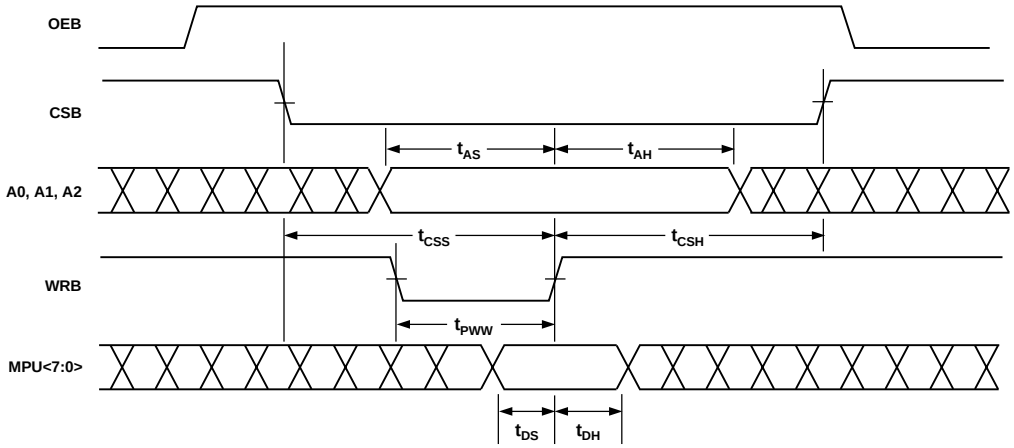


Figure 2. Write Timing

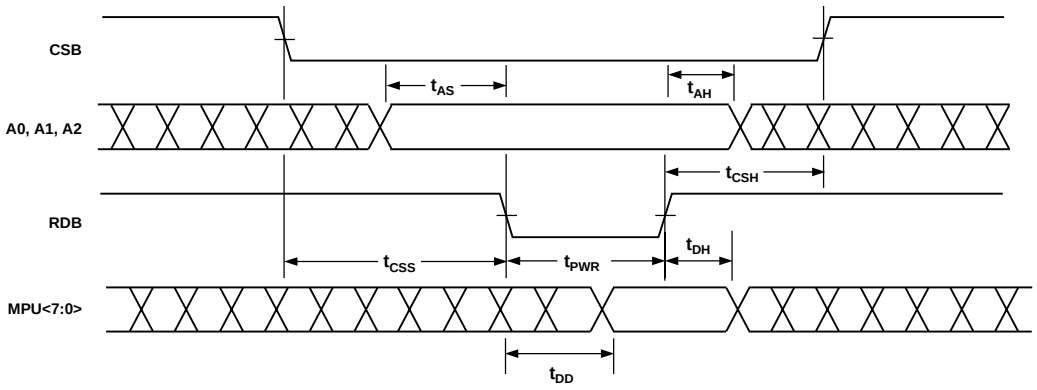


Figure 3. Read Timing

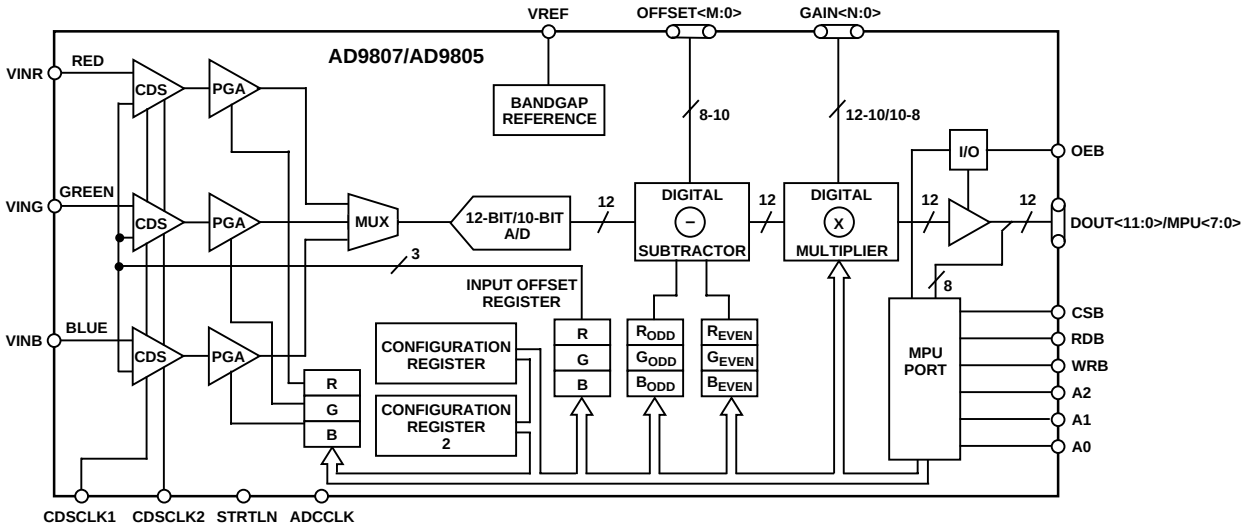


Figure 4. Block Diagram

REGISTER OVERVIEW

MPU Port Map

Table II shows the MPU Port Map. The MPU Port Map is accessed through pins A0, A1 and A2 of the AD9807/AD9805, and provides the decoding scheme for the various registers of the AD9807/AD9805. When writing or reading from any of the registers, the appropriate bits must be applied to A0–A2.

Table II. MPU Port Map Format

A2	A1	A0	Register
0	0	0	Configuration Register
0	0	1	Configuration Register 2
0	1	0	PGA Gain Register
0	1	1	Odd Offset Register
1	0	0	Even Offset Register
1	0	1	Input Offset Register
1	1	0	RESERVED
1	1	1	Bayer Mode

Configuration Register/AD9807

The Configuration Register controls three functions: a color pointer, gain and offset pin configurations, and digital gain scaling. Figure 5 shows the AD9807 Configuration Register. Bits 0–2 control the digital scaling function. Setting a bit makes the corresponding condition true. Resetting Bits 0–2 disables and bypasses the digital multiplier. Bits 3–5 control the gain and offset pin distribution. Resetting Bits 3–5 disables and bypasses the digital subtracter and sets the gain word width to 12. Setting any bit makes the corresponding condition true. For example, if Bit 3 is set, the 2 LSBs of the gain word become the 2 MSBs of the offset word. If Bit 4 is set, the LSB of the gain word becomes MSB of the offset word. Bits 6 and 7 direct register data written to the MPU<7:0> bus to the appropriate red, green or blue register.

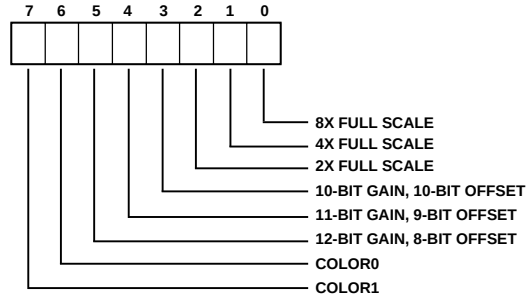


Figure 5. AD9807 Configuration Register Format

Configuration Register/AD9805

The Configuration Register controls three functions: a color pointer, gain and offset pin configurations, and digital gain scaling. Figure 6 shows the AD9805 Configuration Register. Bits 0–2 control the digital scaling function. Setting a Bit makes the corresponding condition true. Resetting Bits 0–2 disables and bypasses the digital multiplier. Bits 3–5 control the gain and offset pin distribution. Resetting Bits 3–5 disables and bypasses the digital subtracter and sets the gain word width to 10. Setting any bit makes the corresponding condition true. If Bit 3 is set, the 2 LSBs of the gain word become the 2 MSBs of the offset word. If Bit 4 is set, the LSB of the gain word becomes MSB of the offset word. Bits 6 and 7 direct register data written to the MPU<7:0> bus to the appropriate red, green or blue register.

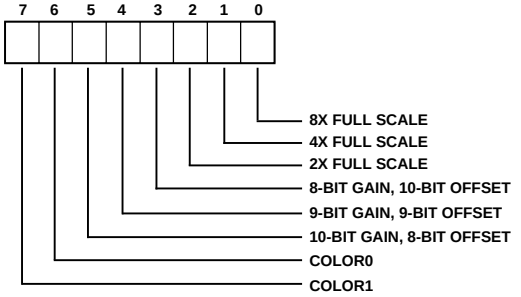


Figure 6. AD9805 Configuration Register Format

Color Pointer

Both the AD9807 and the AD9805 use Bits 6 and 7 in the Configuration Register to direct data to the corresponding internal registers. Table III shows the mapping of Bits 6 and 7 to their corresponding color.

Table III. Color Pointer Map

Bit 7	Bit 6	Color Register
0	0	Red
0	1	Green
1	0	Blue
1	1	RESERVED

Configuration Register 2

Configuration Register 2 controls several functions: color/black and white selection, CDS enabling, A/D Reference Control and Input Clamp Mode. Figure 7 shows the AD9807 and AD9805 Configuration Register 2 format. Setting Bit 0 enables the three internal CDS blocks of the AD9807/AD9805. Resetting Bit 0 disables the internal CDS blocks, configuring the part for SHA operation. Setting Bit 1 places the AD9807/AD9805 in single-channel (black & white) mode. In this mode, only one of the three input channels is used. The color bits in the configuration register at the time of the last write indicate the particular channel used. Resetting Bit 1 places the AD9807/AD9805 in color mode and all three input channels are enabled. Bits 2-4 control the full-scale input span of the A/D. Setting Bit 2 results in a 4 V p-p input span. Setting Bit 3 results in a 2 V p-p full-scale input span. Setting Bit 4 results in a full-scale span set by an external reference connected to the VREF pin of the AD9807/AD9805 (Full Scale = 2 × VREF). Resetting Bits 2, 3 or 4 disables that particular mode. Bits 6 and 7 select the desired clamp mode (see Figure 17). Table IV shows the truth table for clamp mode functionality. Line clamp mode allows control of the input switch (S1) via CDSCLK1 only while STRTLN is reset. Pixel clamp mode allows control of the input switch (S1) via CDSCLK1 regardless of the state of STRTLN. No clamp mode disables the input switch (S1) regardless of the selected mode of CDS operation.

Table IV. Clamp Mode Truth Table

Bit 7	Bit 6	Clamp Mode
0	0	Line Clamp
0	1	Pixel Clamp
1	0	No Clamp
1	1	RESERVED

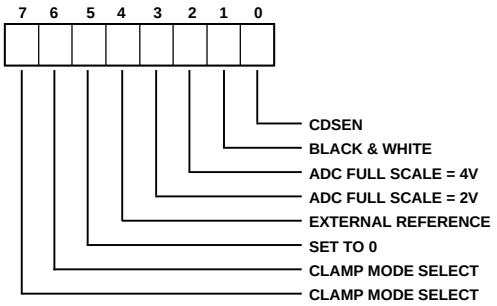


Figure 7. AD9807/AD9805 Configuration Register 2 Format

Input Offset Registers

The Input Offset Registers control the amount of analog offset applied to the analog inputs prior to the PGA portion of the AD9807/AD9805; there is one Input Offset Register for each color. Figure 8 shows the Input Offset Register format. The offset range may be varied between –80 mV and 20 mV. The data format for the Input Offset Registers is straight binary coding. An all "zeros" data word corresponds to –80 mV. An all "ones" data word corresponds to 20 mV. The offset is variable in 256 steps. The contents of the color pointer in the Configuration Register at the time an Input Offset Register is written indicates the color for which that offset setting applies.

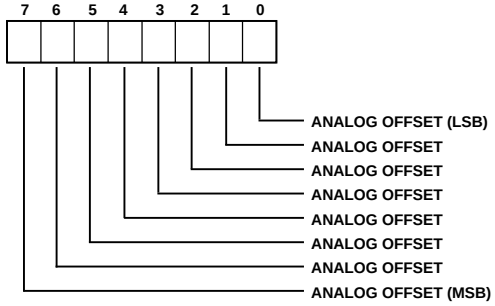


Figure 8. Input Offset Registers Format

PGA Gain Registers

Bits 0–3 of the PGA Gain Registers control the amount of gain applied to the analog inputs prior to the A/D conversion portion of the AD9807/AD9805; there is one PGA Gain Register for each channel. Figure 9 shows the PGA Gain Register format. The gain range may be varied between 1 and 4. The data format for the PGA Gain Registers is straight binary coding. An all "zeros" data word corresponds to an analog gain of 1. An all "ones" data word corresponds to an analog gain of 4. The gain is variable in 16 steps (see Figure 16). The contents of the color pointer in the Configuration Register at the time a PGA Gain Register is written indicates the color for which that gain setting applies. Bits 4–7 of the PGA Gain Registers are reserved.

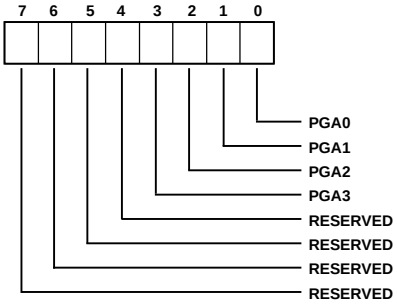


Figure 9. PGA Gain Registers Format

Odd, Even Offset Registers

The Odd and Even Offset Registers provide a means of digitally compensating the odd and even offset error (Register Imbalance) typical of multiplexed CCD imagers; there is one Odd and one Even Offset Register for each color. Figure 10 shows the AD9807/AD9805 Odd and Even Offset Register Formats. The data format for the Odd and Even Offset Registers is twos complement. The offsets may be varied between positive

127 LSBs and negative 128 LSBs. The offset is variable in 1 LSB increments (see Table V). The contents of the color pointer in the Configuration Register at the time an Odd or Even Register is written indicates the color for which that offset setting applies.

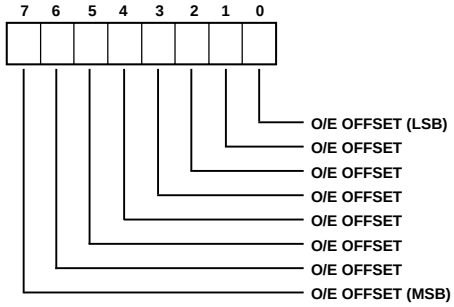


Figure 10. Odd and Even Offset Registers Format

Table V. Odd/Even Offset Register Coding

Odd/Even Register Contents	Offset Value
0111 1111	+127 LSB
.	.
.	.
.	.
0000 0001	+1 LSB
0000 0000	0 LSB
1111 1111	–1 LSB
.	.
.	.
.	.
1000 0000	–128 LSB

DATA BUSES

GAIN<n:0>—The GAIN data bus gives the user access to the internal digital multiplier. Data from the GAIN bus is latched into the appropriate internal registers in accordance with the timing shown in Figure 1. Note that the GAIN data must be valid on the rising edges of ADCCLK. The contents of the register become one multiplicand of the digital multiplier; the output data from the digital subtracter is the other multiplicand. The AD9807/AD9805 provide a variable word length for the GAIN data word. Based on the setting in the Configuration Register, the GAIN data word may be 10, 11 or 12 bits wide (8, 9 or 10 bits wide for the AD9805). The data format for the GAIN data bus is straight binary coding. An all "zeros" data word always corresponds to a gain setting of 1×. An all "ones" data word corresponds to a gain setting dependent on Bits 0–2 of the Configuration Register. The gain is variable in 1024, 2048, or 4096 (256, 512 or 1024 for the AD9805) increments depending on the width of GAIN data word.

OFFSET<m:0>

The OFFSET data bus gives the user access to the internal digital subtracter. Data from the OFFSET bus is latched into the appropriate internal registers in accordance with the timing shown in Figure 1. Note that the OFFSET data must be valid on the rising edges of ADCCLK. The contents of the register become the subtrahend; the output data from the A/D converter (after odd/even correction) is the other input. The AD9807/AD9805 provide a variable word length for the OFFSET data word. Based on the setting in the Configuration Register, the OFFSET data word may be 8, 9 or 10 bits wide. The data format for the OFFSET data bus is straight binary coding. An all "zeros" data word corresponds to an offset value of 0 LSBs. An all "ones" data word subtracts an offset value of 256, 512 or 1024 LSBs, depending on the width of OFFSET data word. The offset is variable in 256, 512 or 1024 increments.

DOUT<n:0>—The DOUT data bus is bidirectional. CMOS compatible digital data is available as an output on the DOUT bus. Data is coded in straight binary format. When CSB and either WRB or RDB are applied to the AD9807/AD9805, the DOUT data bus becomes an input/output port for the register data, shown as MPU<7:0>. The timing and latency for the DOUT data bus are given in Figures 11 through 15.

FUNCTIONAL OVERVIEW

It is possible to operate the AD9807/AD9805 in one of five modes: 3-Channel Operation with CDS, 3-Channel SHA Operation, 1-Channel Operation with CDS, 1-Channel SHA Operation and 2-Channel Bayer Mode. A description of each of the five modes follows.

3-Channel Operation with CDS

This mode of the AD9807/AD9805 enables simultaneous sampling of a triple output CCD. The CCD waveforms are ac coupled to the VINR, VING and VINB pins of the AD9807/AD9805 where they are automatically biased at an appropriate voltage level using the on-chip clamp; the inputs may alternatively be dc coupled if they have already been appropriately level shifted. The internal CDSs take two samples of the incoming pixel data: the first samples (CDSCLK1) are taken during the reset time while the second samples (CDSCLK2) are taken during the video, or data, portion of the input pixels. The offsets of the three input channels are modified by the values stored in the input offset registers. The voltage differences of the reset levels and video levels are inverted and amplified by the PGAs; the settings in the corresponding PGA Gain Registers determine the gains of the PGAs. These outputs from the PGAs are then routed through a high speed multiplexer to a 12-bit A/D converter (10-bit for AD9805) for digitization; the multiplexer cycles between the red, green and then blue channels. After digitization, the data is modified by the amount indicated in the Odd and Even Offset Registers. A digital subtracter allows additional pixel rate offset modification of each color based on the values written to the OFFSET data bus. Finally, a digital multiplier allows pixel rate gain modification of each color based on the values written to the GAIN data bus. Latency for the red, green and blue channels is 6 ADCCLK cycles (9 cycles for the gain and offset bus; see Figure 12).

The STRTLN signal indicates the first red, green and blue pixels in a scan line, and the red channel is always the first pixel digitized. The state of STRTLN is evaluated on the rising edges of ADCCLK. When STRTLN is low, the internal circuitry is reset on the next rising edge of ADCCLK; the multiplexer is switched to the red channel and the odd/even circuitry is configured to expect even pixels. After STRTLN goes high, the first set of pixels is assumed to be even. Consecutive sets of pixels (red, green and blue) are assumed to alternate between odd and even pixel sets.

3-Channel SHA Operation
This mode of the AD9807/AD9805 enables 3-channel simultaneous sampling; it differs from the CDS sampling mode in that the CDS functions are replaced with sample-and-hold amplifiers (SHAs). CDSCLK1 becomes the sample-and-hold clock; CDSCLK2 is tied to ground. The input is sampled on the falling edge of CDSCLK1. The input signals must be either dc coupled and level shifted, or dc restored prior to driving the VINR, VING, and VINB pins of the AD9807/AD9805 (clamp mode must be disabled). The input signal in this mode is ground-referenced. The offsets of the three input channels are modified by the values stored in the input offset registers. The part does not invert the input signals prior to amplification by the PGAs; the settings in the corresponding PGA Gain Registers determine the gains of the PGAs. These outputs from the PGAs are then routed through a high speed multiplexer to a 12-bit A/D converter (10-bit for AD9805) for digitization; the multiplexer cycles between the red, green and then blue channels. After digitization, the data is modified by the amount indicated in the Odd and Even Offset Registers. A digital subtracter allows additional pixel rate offset modification of each color based on the values written to the OFFSET data bus. Finally, a digital multiplier allows pixel rate gain modification of each color based on the values written to the GAIN data bus. Latency for the red, green and blue channels is 6 ADCCLK cycles (9 cycles for the gain and offset bus; see Figure 13).

The STRTLN signal indicates the first red, green and blue pixels in a scan line and the red channel is always the first pixel digitized. The state of STRTLN is evaluated on the rising edges of ADCCLK. When STRTLN is low, the internal circuitry is reset on the next rising edge of ADCCLK; the multiplexer is switched to the red channel and the odd/even circuitry is configured to expect even pixels. After STRTLN goes high, the first set of pixels is assumed to be even. Consecutive sets of pixels (red, green and blue) are assumed to alternate between odd and even pixel sets.

1-Channel Operation with CDS
This mode of the AD9807/AD9805 enables single-channel, or monochrome, sampling. The CCD waveform is ac coupled to either the VINR, VING, and VINB pin of the AD9807/AD9805 where it is biased at an appropriate voltage level using the on-chip clamp; the input may alternatively be dc coupled if it has already been appropriately level shifted. Bits 6 and 7 in the Configuration Register select the desired input. The internal CDS takes two samples of the incoming pixel data: the first sample (CDSCLK1) is taken during the reset time while the second sample (CDSCLK2) is taken during the video, or data, portion of the input pixel. The offset of the input signal is modified by the value stored in the input offset register. The voltage *difference* of the reset level and video level is inverted and amplified by the PGA; the setting in the corresponding PGA Gain Register determines the gain of the PGA. The output from the PGA is then routed through a high-speed multiplexer to a 12-bit A/D converter (10-bit for AD9805) for digitization; the multiplexer does not cycle in this mode. After digitization, the data is modified by the amount indicated in the Odd and Even Offset Registers. A digital subtracter allows additional pixel rate offset modification of the signal based on the values written to the OFFSET data bus. Finally, a digital multiplier allows pixel rate gain modification of the signal based on the values written to the GAIN data bus. Latency is 6 ADCCLK cycles (7 cycles for the gain and offset bus; see Figure 14).

The state of STRTLN is evaluated on the rising edges of ADCCLK. When STRTLN is low, the internal circuitry is reset on the next rising edge of ADCCLK; the odd/even circuitry is configured to expect an even pixel. After STRTLN goes high, the first pixel is assumed to be even. Consecutive pixels (red, green or blue) are assumed to alternate between odd and even. The blue and green channels are recommended for single channel operation to achieve the maximum sampling rate; if using red, invert ADCCLK as shown in Figure 1d.

1-Channel SHA Operation
This mode of the AD9807/AD9805 enables single-channel, or monochrome sampling; it differs from the CDS monochrome sampling mode in that the CDS function is replaced with a sample-and-hold amplifier (SHA). CDSCLK1 becomes the sample-and-hold clock; CDSCLK2 is tied to ground. The input is sampled on the falling edge of CDSCLK1. The input waveform would typically be either dc coupled and level shifted, or dc restored prior to driving either the VINR, VING and VINB pins of the AD9807/AD9805 (clamp mode must be disabled).

Bits 6 and 7 in the Configuration Register select the desired input. The input signal in this mode is ground referenced. The input signal is not inverted prior to amplification by the PGA; the setting in the corresponding PGA Gain Register determines the gain of the PGA. The offset of the input signal is modified by the value stored in the input offset register. This signal is then routed through a high speed multiplexer to a 12-bit A/D converter (10-bit for AD9805) for digitization; the multiplexer does not cycle in this mode. After digitization, the data is modified by the amount indicated in the Odd and Even Offset Registers. A digital subtracter allows additional pixel rate offset modification of the signal based on the values written to the OFFSET data bus. Finally, a digital multiplier allows pixel rate gain modification of the signal based on the values written to the GAIN data bus. Latency is 6 ADCCLK cycles (7 cycles for gain and offset; see Figure 15).

The state of STRTLN is evaluated on the rising edges of ADCCLK. When STRTLN is low, the internal circuitry is reset on the next rising edge of ADCCLK; the odd/even circuitry is configured to expect an even pixel. After STRTLN goes high, the first pixel is assumed to be even. Consecutive pixels (red, green or blue) are assumed to alternate between odd and even. The blue and green channels are recommended for single channel operation to achieve the maximum sampling rate; if using red, invert ADCCLK as shown in Figure 1f.

2-Channel Bayer Mode Operation with CDS
This mode of the AD9807/AD9805 enables Bayer Mode. The CCD waveform is ac coupled to both the VING and VINB pins of the AD9807/AD9805 where it is biased at an appropriate voltage level using the on-chip clamp; the input may alternatively be dc coupled if it has already been appropriately level shifted. The internal CDS takes two samples of the incoming pixel data: the first sample (CDSCLK1) is taken during the reset time while the second sample (CDSCLK2) is taken during the video, or data, portion of the input pixel. The offset of the input signal is modified by the value stored in the input offset register. The voltage difference of the reset level and video level

is inverted and amplified by the PGA; the setting in the corresponding PGA Gain Register determines the gain of the PGA. The output from the PGA is then routed through a high speed multiplexer to a 12-bit A/D converter (10-bit for AD9805) for digitization; the multiplexer does cycle in this mode. After digitization, the data is modified by the amount indicated in the Even Offset Registers. A digital subtracter allows additional pixel rate offset modification of the signal based on the values written to the OFFSET data bus. Finally, a digital multiplier allows pixel rate gain modification of the signal based on the values written to the GAIN data bus. Latency is 6 ADCCLK cycles (7 cycles for the gain and offset bus; see Figure 14).

The state of STRTLN is evaluated on the rising edges of ADCCLK. When STRTLN is low, the internal circuitry is reset on the next rising edge of ADCCLK; the odd/even circuitry is configured to expect even pixels.

This feature has been included to accommodate the use of the part with an area CCD (Bayer Mode). The mode is initiated by writing a one to the LSB of the register at Address 7 (see Figure 21). The write to enable the mode should be performed when the STRTLN input is inactive (low) and the ADCCLK is running. The first pixel after an active edge on STRTLN will be a green pixel. All pixels in Bayer Mode are even and use the even offset registers. The line will continue alternating GRGRGR pixels until STRTLN goes inactive. The next line will be BGBGBG pixels (the first pixel after the active STRTLN edge being blue). Line type will then alternate between GRGRGR and BGBGBG type. To reset the next line to GRGRGR type at the start of the next frame/image, rewrite the Bayer mode enable bit to a one during the inactive STRTLN period. All red and blue pixels pass through the blue channel of the part and use the blue PGA and offset registers. To use a different offset/PGA gain value the register must be written to between lines. Green pixels on either line type pass through the green channel.

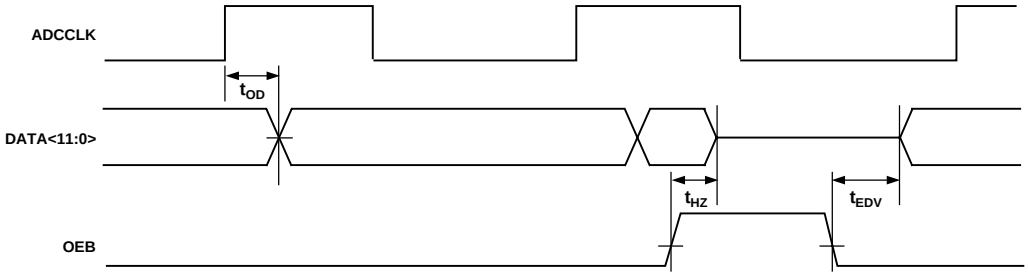


Figure 11. Digital Output Timing

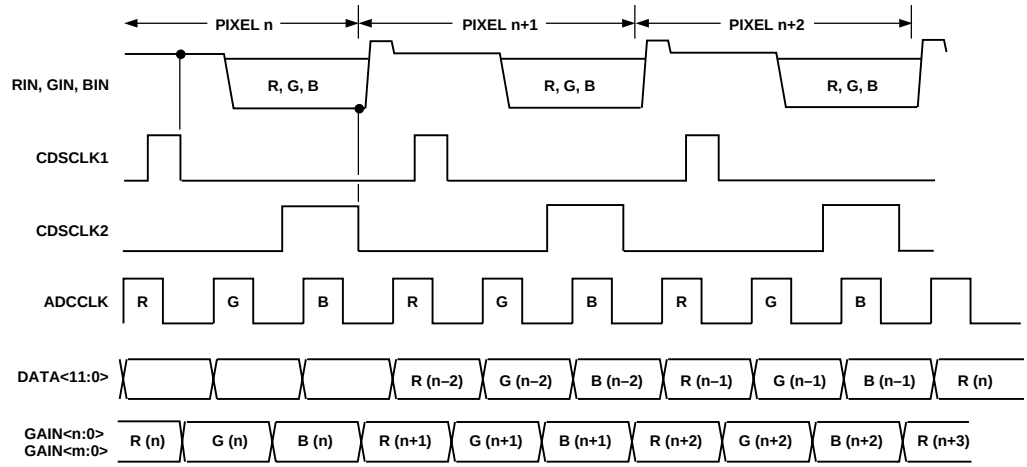


Figure 12. DOUT Latency, 3-Channel CDS Mode

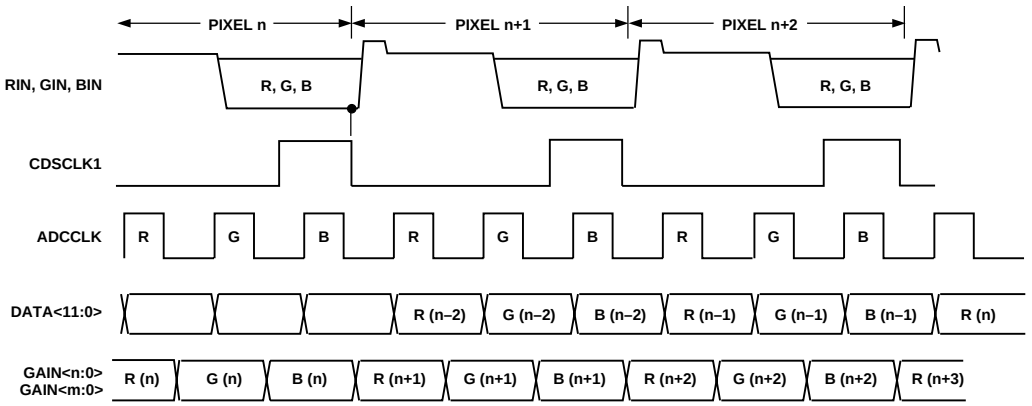


Figure 13. DOUT Latency, 3-Channel SHA Mode

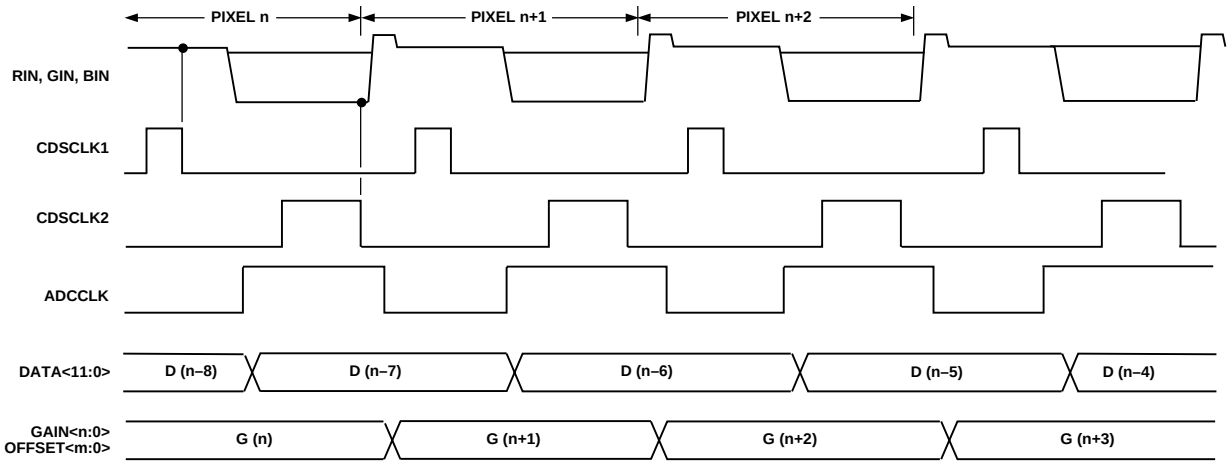


Figure 14. DOUT Latency, 1-Channel CDS Mode

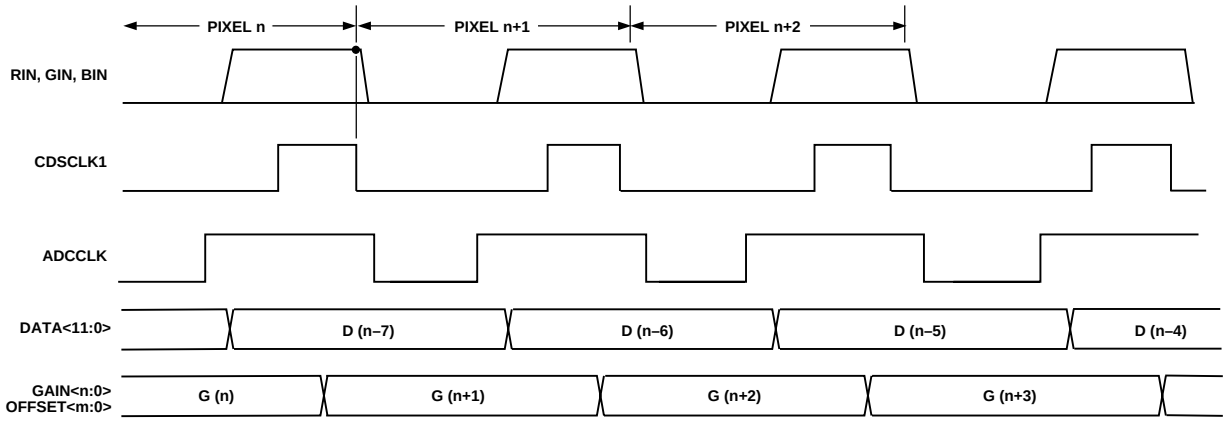


Figure 15. DOUT Latency, 1-Channel SHA Mode

Calculating Overall Gain

The overall gain for the AD9807/AD9805 can accommodate a wide range of input voltage spans. The total gain is a composite of analog gain (from the PGAs), digital gain (from the digital multiplier) and the input span setting for the A/D (2 V or 4 V). To determine the overall gain setting for the AD9807/AD9805, always multiply the PGA gain setting by the digital gain setting. In addition, the 2 V/4 V reference option can effectively provide analog gain for input signals less than 2 V p-p.

$$Overall\ Gain = Analog\ Gain \times Digital\ Gain$$

For example, with the PGA gain equal to 1 (gain setting equals all "zeros") and the digital multiplier equal to 1, the minimum gain equals 1. With these settings, input signals can be as large as 2 V or 4 V depending on the reference setting. Alternatively, with the PGA gain equal to 4 (gain setting equals all "ones") and the digital multiplier equal to 8, the maximum gain equals 32. With the A/D reference span set to 2 V, an input signal span as small as 62.5 mV p-p will produce a digital output spanning from all "zeros" to all "ones." For ranges between 62.5 mV and 4 V, see the Digital Gain and Analog Gain sections of the data sheet.

Analog Gain

The transfer function of the PGA is:

$$Analog\ Input = \frac{4}{1+3\times\left[\frac{15-x}{15}\right]}$$

where x is the decimal representation of the settings in the PGA gain register. Figure 16 shows the graph of this transfer function on both a linear and logarithmic scale. The transfer function is approximately linear in dB.

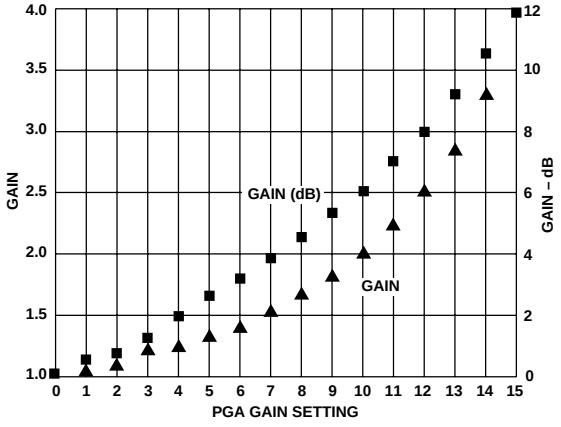


Figure 16. PGA Transfer Function

Digital Gain

The digital multiplier section of the AD9807/AD9805 allows the user to apply gain in addition to that afforded by the analog PGA. The minimum gain of the digital multiplier is always 1. The user sets the maximum gain of the digital multiplier to be 8, 4, or 2 with Bits 0–2 in the Configuration Register. (The max gain is the same for all three channels.) The digital gain applied to the output from the digital subtracter is calculated using the equation:

$$Digital\ Gain = \left[1+\left(\frac{Gain<n{:}0>}{Y}\right)\times X\right]$$

where $GAIN<n{:}0>$ is the decimal representation of the GAIN bus data bits, Y = 4096 for the AD9807, Y = 1024 for the AD9805, and X equals 1, 3 or 7 depending on Bits 0–2 in the Configuration Register.

Overall Transfer Function

The overall transfer function for the AD9807 can be calculated as follows:

$$ADC_{OUT} = \frac{\left[\left(V_{IN} \pm InputOffset\right)\times PGA\ Gain\right]}{2\times V_{REF}} \times 4096$$

$$D_{OUT} = [ADC_{OUT} + Offset\ Register - Offset\ Bus][Digital\ Gain]$$

Choosing the Input Coupling Capacitors

Because of the dc offset present at the output of CCDs, it is likely that these outputs will require some form of dc restoration to be compatible with the input requirements of the AD9807/AD9805. To simplify input level shifting, a dc blocking capacitor may be used in conjunction with the internal biasing circuits of the AD9807/AD9805 to accomplish the necessary dc restoration.

Figure 17 shows the equivalent analog input for the VINR, VING and VINB inputs.

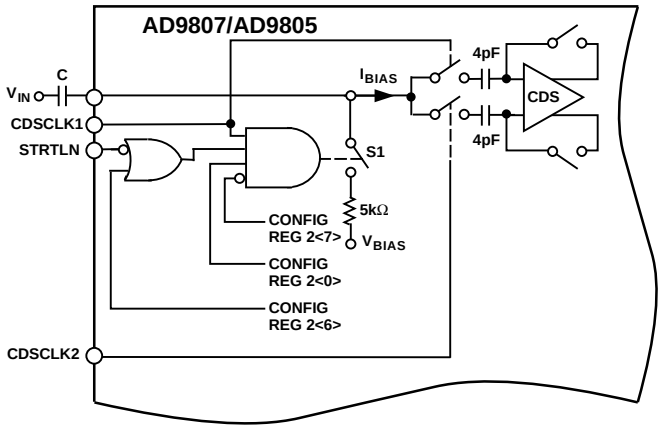


Figure 17. Equivalent Analog Inputs (VINR, VING, and VINB)

Enabling CDS functionality and Line Clamp Mode with Bits 0, 6 and 7 in Configuration Register 2 allows switch S1 to turn on when STRTLN is low and CDSCLK1 goes high. This connects a 5 kΩ biasing resistor to the inputs. This arrangement acts to bias the average level of the input signal at voltage, V_{BIAS}. The voltage, V_{BIAS}, changes depending on the selected PGA gain setting. Specifically, for gain settings from 0 to 5, V_{BIAS} equals 4 V; for gain settings from 10 to 15, V_{BIAS} equals 3 V. For gain settings between 5 and 10, V_{BIAS} decreases linearly from 4 V to 3 V.

The size of the coupling capacitor is dependent on several factors including signal swing, allowable droop, and acquisition time. The following procedure shows how to determine the recommended range of capacitors.

Calculating C_{MAX}

The maximum capacitor value is largely dependent on the degree of accuracy and how quickly the input signal must be level-shifted into the valid input range of the degree of accuracy. Other factors affecting the speed of the capacitor charging or

discharging include the amount of time that input switch S1 is turned on, the input impedance of the AD9807/AD9805 and the output impedance of the circuit driving the coupling capacitor. The impedance of the drive circuit, R_{OUT}, the input impedance of the AD9807/AD9805, R_{IN}, and the desired charging time, t_{ACQ}, are all known quantities. Note that t_{ACQ} may not necessarily occur over a continuous period of time; it may actually be an accumulation of discrete charging periods. This is typical where CDSCLK1 is asserted only during the reset levels of the pixels. In this case, the quantity, m × T, may be substituted for t_{ACQ}, where m is the number of periods CDSCLK1 is asserted and T is the period of the assertion. Given these quantities, the maximum value for the input coupling capacitor is computed from the equation:

$$C_{MAX} \cong \frac{t_{ACQ}}{R_{IN} + R_{OUT}} / \ln\left(\frac{V_C}{V_E}\right)$$

where V_C is the required voltage change across the coupling capacitor and V_E is the maximum tolerable error voltage. V_C is calculated by taking the difference between the CCD's reset level and the internal bias level of the AD9807/AD9805. V_E is the level of accuracy to which the input capacitor must be charged and is system dependent. Usually the allowable droop of the capacitor voltage is taken into account. This is discussed below. For example, if the CCD output can droop up to 1 volt without affecting the accuracy of the CDS, then clamping to within about one tenth of the allowable droop (100 mV) should be sufficient in most cases.

Calculating C_{MIN}

Determining C_{MIN} is a function of the amount of allowable voltage droop. It is important that the signals at the inputs of the AD9807/AD9805 remain within the supply voltage limits so the CDSs are able to accurately digitize the difference between the reset level and the video level. Assuming the input voltages are initially biased at the correct levels, the input bias current of the AD9807/AD9805 inputs will discharge the input coupling capacitors resulting in voltage droop. After taking into account any droop, the peaks of the input signal must remain within the required voltage limits of AD9807/AD9805 inputs.

Specifically, C_{MIN} is a function of the maximum allowable droop, dV, in one scan line, the number of pixels across one scan line, n, the period of one pixel, t, and the input bias current of the AD9807/AD9805, I_{BIAS}. C_{MIN} is calculated from the equation:

$$C_{MIN} = \left(\frac{I_{BIAS}}{dV}\right) \times n \times t$$

Some examples are given below showing the typical range of capacitor values.

Example 1

A 5000 pixel CCD running at a 2 MHz (t = 500 ns) has a reset level of 4.5 volts and an output voltage of 1.8 volts. The number of optical black pixels available at the start of a line is 18. Using the AD9807/AD9805 with an input span of 4 volts and a PGA gain of 2 gives a V_{BIAS} of 3 volts. If the input signal is clamped to 3 volts during the optical black pixels, the required voltage change on the input capacitor, V_C, equals (4.5 – 3) or 1.5 volts and the maximum droop allowable during one line, dV, will be (3 – 1.8) or 1.2 volts before the signal droops below 0 volts.

With dV = 1.2 volts, a clamp accuracy of 100 mV should be sufficient (V_E =100 mV), but this value can be adjusted. The amount of time available to charge up the input capacitor, T_{ACQ}, will equal the period of CDSCLK1 (when the clamp switch is closed) times the number of optical black pixels. With a pixel rate of 2 MHz, CDSCLK1 would typically be around 100 ns wide, giving T_{ACQ} =1800 ns or 1.8 µs. The input impedance of the AD9807 is 5K, and the input bias current is 10 nA. Assume the source impedance driving the AD9807 is low (R_{OUT} = 0).

$$C_{MAX} = (1.8\ \mu s/5K) \times (1/\ln(1.5/0.1)) = 133\ pF$$

$$C_{MIN} = (10\ nA/1.2) \times 5000 \times 500\ ns = 21\ pF$$

Note that a capacitor larger than 133 pF would still work, it would just take several lines to charge the input capacitor up to the full V_C level. Another option to lengthen T_{ACQ} is by clocking the CCD and CDSCLK1 while the transport motor moves the scanner carriage. This would extend T_{ACQ} to several hundred µs or more, meaning that only very fine adjustment would be needed during the limited number of optical black pixels.

Example 2

A 7926 pixel CCD running at 2 MHz has a reset level of 6 volts, an output voltage of 2.9 volts and 80 optical black pixels. Using the AD9807 with an input span of 4 volts and a PGA gain of 1.25, V_{BIAS} = 4 volts. The maximum required voltage change on the capacitor, V_C, is 2 volts and the maximum amount of droop dV for one line is 1.1 volts. T_{ACQ} will be 80 × 100 ns or 8 µs, and V_E = 100 mV should be sufficient. Again, R_{IN} = 5K, R_{OUT} = 0, and I_{BIAS} = 10 nA.

$$C_{MAX} = (8\ \mu s/5K) \times (1/\ln(2/0.1)) \cong 534\ pF$$

$$C_{MIN} = (10\ nA/1.1) \times (7926) \times (500\ ns) = 36\ pF$$

Again, a larger capacitor may be used if several lines are allowed for to initially charge up the cap, or if the CCD and CDSCLK1 are clocked during the moving of the scanner carriage.

Generating 3-Channel Timing from a 16 × Master Clock

Generating the required signals for CDSCLK1, CDSCLK2 and ADCCLK is easily accomplished with a master clock running 16 × the desired per channel pixel rate (i.e., 2 MSPS pixel rate requires 32 MHz master clock). The timing diagram shown in Figure 18 meets all the minimum and maximum timing specifications. Note that a 16 × master clock using only rising edges was chosen instead of using both edges of an 8 × rate clock to ensure immunity to duty cycle variations.

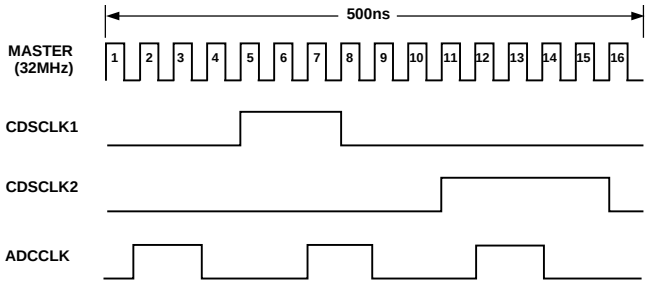


Figure 18. Timing Scheme Using 16× Master Clock

Power-On Initialization and Calibration Sequence

When the AD9807/AD9805 is powered on, the following sequence should be used to initialize the part to a known state. The digital gain and offset buses are disabled until the calibration sequence. The Bayer mode register must be written to and set to zero if this mode is not going to be used.

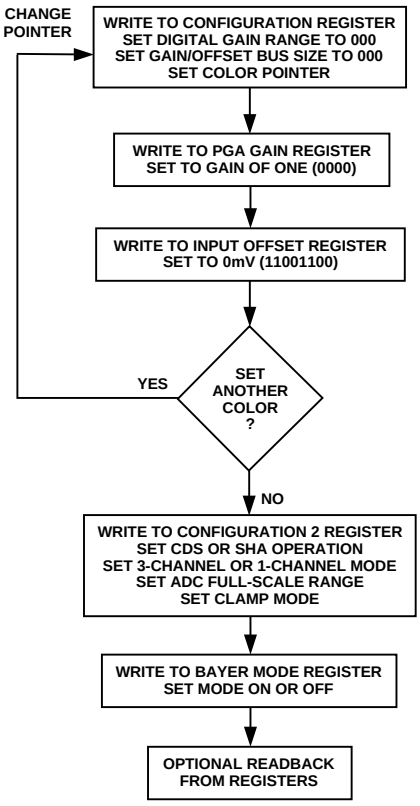


Figure 19. Initialization

To calibrate the AD9807/AD9805 for a particular scan, use the following sequence.

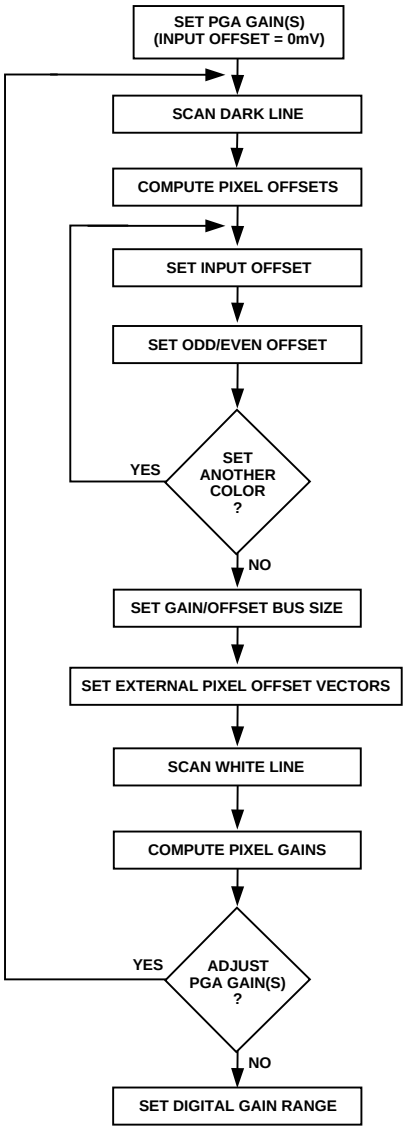


Figure 20. Calibration

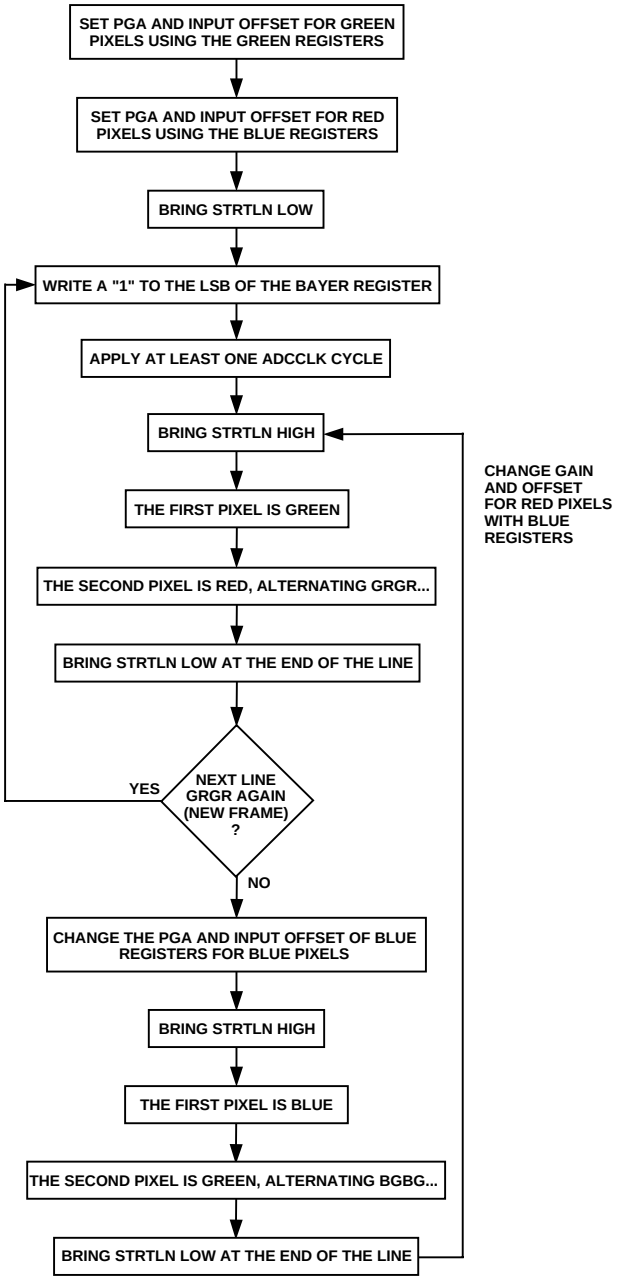


Figure 21. Bayer Mode Operation

Grounding and Decoupling

Figure 22 shows the recommended decoupling capacitors and ground connections for the AD9807/AD9805. Notice that all of the power and ground connections are common for the analog and digital portions of the chip. This would be the best way to connect the device on a board containing a large number of digital components. By treating the AD9807/AD9805 as an analog component, the on-board digital circuitry is considered "quiet digital" and the digital supply pins are connected to the clean analog supply and analog ground plane. For this technique to work well, it is important that the digital supply pins be well decoupled to the analog ground plane and that the digital outputs of the AD9807/AD9805 are buffered to minimize the digital drive current. The buffers would be referred to the digital supply and ground. This scheme is preferable to tying the digital portion of the AD9807/AD9805 to a noisy digital ground and power plane, capacitively coupling noise to the analog circuitry within the device. The AD9807/AD9805 evaluation boards use this grounding method, shown in Figures 26 and 27. If a minimum amount of digital circuitry exists on the board, it is possible that the power and ground connections of the AD9807 can be separated; be sure to maintain a single point connection between the two ground planes at the AD9807/AD9805.

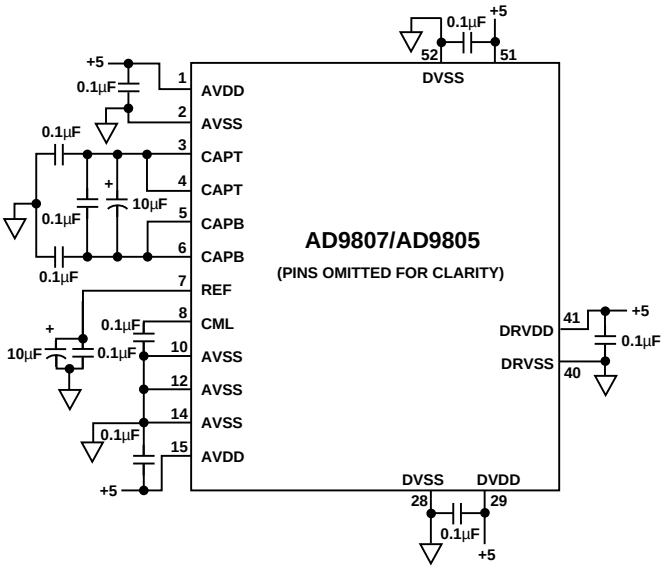


Figure 22.

CIS Application

Unlike many other integrated circuit CCD signal processors, the AD9807/AD9805 can easily be implemented in imaging systems that do not use a CCD. By disabling the input clamp and the CDS blocks, any dc coupled signal within the input limits of the part can be digitized. Figure 23 shows a typical block diagram of the AD9807 used with a color CIS module, in this case Dyna Image Corporation's DL100*. The three color output signals are dc coupled into the AD9807. The Dyna CIS module's output levels are around 70 mV to 500 mV dark to bright, well within the input range of the AD9807. The AD9807 is configured for 3-channel SHA operation through the MPU registers. Timing used with the Dyna DL100 is shown in Figure 24; the CIS output levels are sampled on the falling edge of CDSCLK1. The digital ASIC shown can be implemented in a variety of ways: it could include the MPU interface and timing generator, as well as memory for the output data and pixel gain and offset correction vectors.

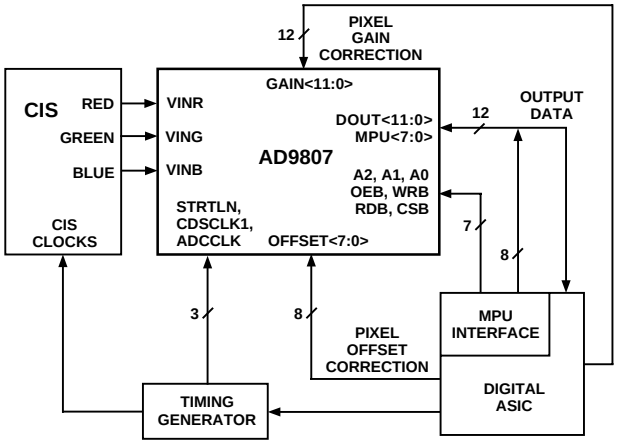


Figure 23. CIS Application Diagram (Power, Ground, and Decoupling Omitted)

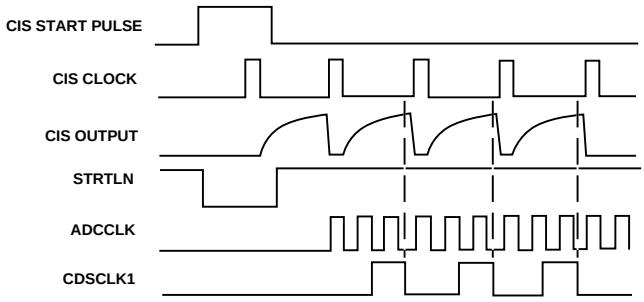


Figure 24. CIS Application Timing Signals

EVALUATION BOARDS

The AD9807 and AD9805 evaluation boards are designed to provide an easy interface to a standard PC, simplifying the task of evaluating the performance of the AD9807/AD9805 with an existing imaging system. The system level block diagram shown in Figure 25 illustrates the basic evaluation setup for the AD9807 (the AD9805 is the same). The user needs to supply the analog input signals (such as outputs from a CCD), the AD9807/AD9805's clock signals, a power supply and a printer cable to connect the evaluation board to the PC's parallel port. Software is included to allow the user to easily accomplish three major tasks: first, configure the AD9807/AD9805 in one of several operating modes (1 Channel, 3 Channel, CDS or SHA mode, etc.), second, acquire output data from the part and third, download pixel gain and offset correction data to the evaluation board and enable pixel rate shading and offset correction.

Figures 26 and 27 show the signal routing and decoupling for the AD9807 evaluation board.

The evaluation boards are designated with the part numbers AD9807-EB and AD9805-EB.

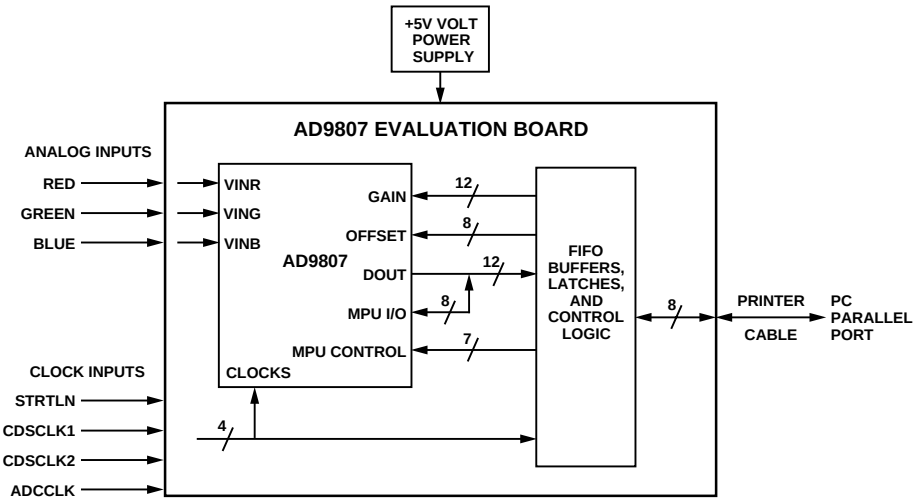


Figure 25. Evaluation System Block Diagram

*All trademarks are properties of their respective holders.

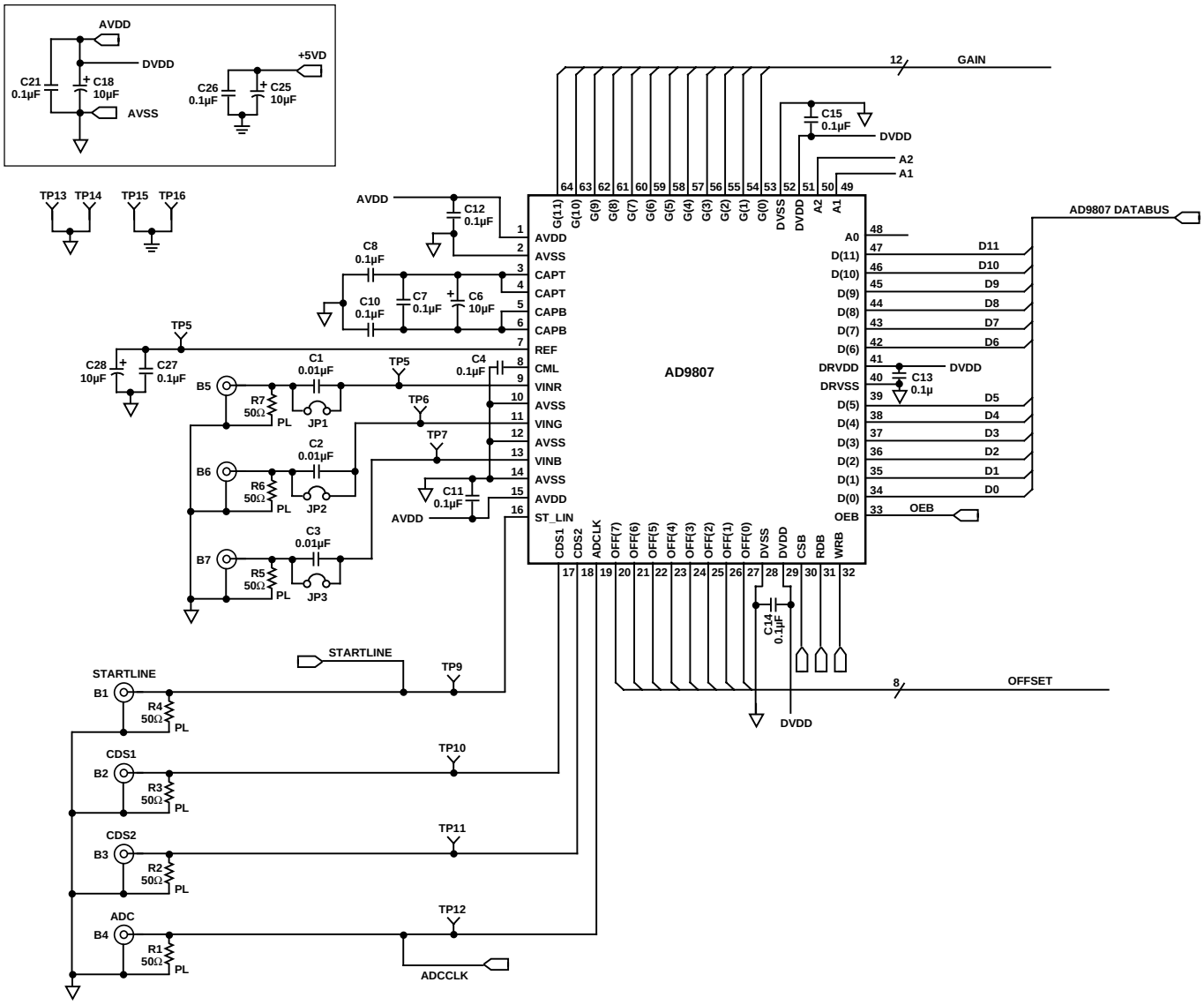


Figure 26. AD9807 Evaluation Board (Digital Circuitry Omitted)

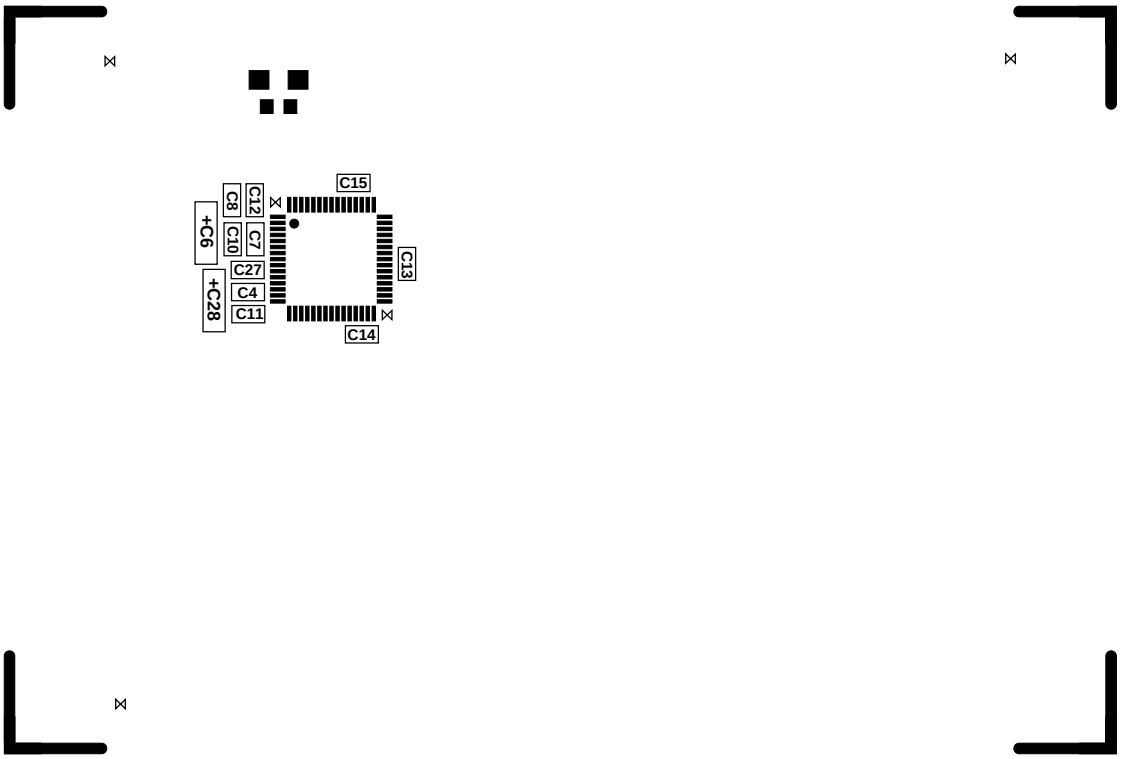
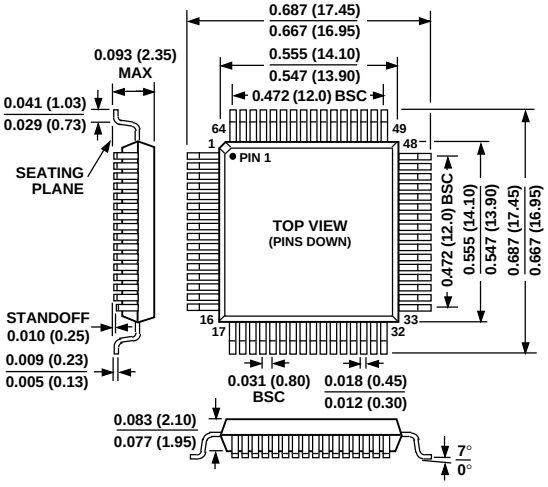


Figure 27. Suggested Capacitor Placement for Single-Side Component Layout

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

64-Terminal PQFP
(S-64)



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