



10-Bit 40 MSPS CCD Signal Processor with Integrated Timing Driver

AD9847

FEATURES

- Correlated Double Sampler (CDS)
- 2 dB to +10 dB Pixel Gain Amplifier (PxGA®)
- 2 dB to 36 dB 10-Bit Variable Gain Amplifier (VGA)
- 10-Bit 40 MHz A/D Converter
- Black Level Clamp with Variable Level Control
- Complete On-Chip Timing Driver
- Precision Timing™ Core with 500 ps Resolution at 40 MSPS
- On-Chip 5 V Horizontal and RG Drivers
- 48-Lead LQFP Package

APPLICATIONS

Digital Still Cameras

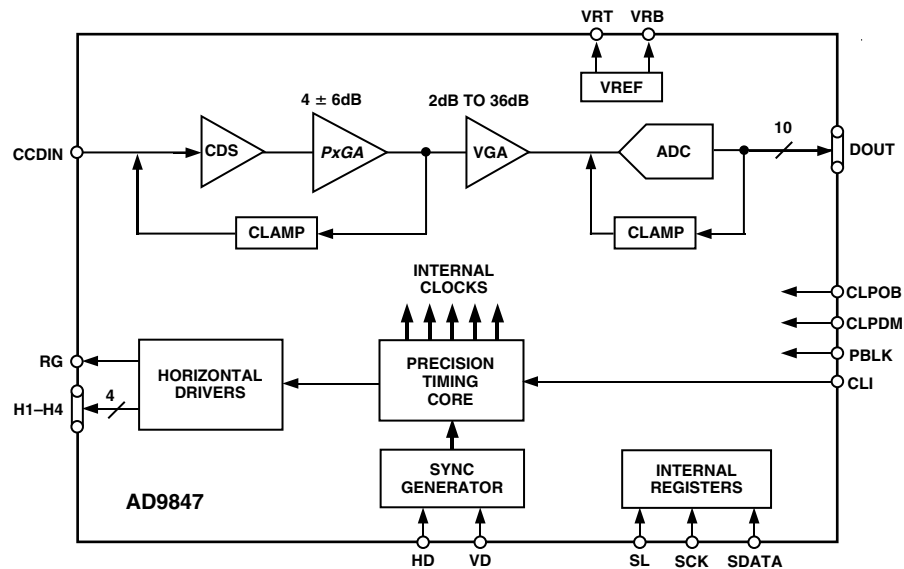
GENERAL DESCRIPTION

The AD9847 is a highly integrated CCD signal processor for digital still camera applications. The AD9847 includes a complete analog front end with A/D conversion, combined with a programmable timing driver. The *Precision Timing* core allows adjustment of high speed clocks with approximately 500 ps resolution at clock speeds of 40 MHz.

The AD9847 is specified at pixel rates of 40 MHz. The analog front end includes black level clamping, CDS, PxGA, VGA, and a 10-bit A/D converter. The timing driver provides the high speed CCD clock drivers for RG and H1-H4. Operation is programmed using a 3-wire serial interface.

Packaged in a space-saving 48-lead LQFP, the AD9847 is specified over an operating temperature range of -20°C to +85°C.

FUNCTIONAL BLOCK DIAGRAM



REV. A

Information furnished by Analog Devices is believed to be accurate and reliable. However, no responsibility is assumed by Analog Devices for its use, nor for any infringements of patents or other rights of third parties that may result from its use. No license is granted by implication or otherwise under any patent or patent rights of Analog Devices. Trademarks and registered trademarks are the property of their respective companies.

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781/329-4700
Fax: 781/326-8703
www.analog.com
© 2003 Analog Devices, Inc.

AD9847—SPECIFICATIONS

GENERAL SPECIFICATIONS

| Parameter | Min | Typ | Max | Unit |
|--|-----|-----|------|------|
| TEMPERATURE RANGE | | | | |
| Operating | -20 | | +85 | °C |
| Storage | -65 | | +150 | °C |
| MAXIMUM CLOCK RATE | 40 | | | MHz |
| POWER SUPPLY VOLTAGE | | | | |
| Analog (AVDD1, 2, 3) | 2.7 | | 3.6 | V |
| Digital1 (DVDD1) H1–H4 | 3.0 | | 5.5 | V |
| Digital2 (DVDD2) RG | 3.0 | | 5.5 | V |
| Digital3 (DVDD3) D0–D11 | | 3.0 | | V |
| Digital4 (DVDD4) All Other Digital | | 3.0 | | V |
| POWER DISSIPATION | | | | |
| DVDD1 (@ 5 V, 100 pF H Loading, 40 MSPS) | | 450 | | mW |
| DVDD2 (@ 5 V, 20 pF RG Loading, 40 MSPS) | | 45 | | mW |
| DVDD1 (@ 3 V, 100 pF H Loading, 40 MSPS) | | 180 | | mW |
| DVDD2 (@ 3 V, 20 pF H Loading, 40 MSPS) | | 15 | | mW |
| AVDD1, 2, 3, DVDD3, 4 (@ 3 V, 40 MSPS) | | 200 | | mW |
| Total Shutdown Mode | | 1 | | mW |

Specifications subject to change without notice.

DIGITAL SPECIFICATIONS (T_{MIN} to T_{MAX} , AVDD1 = DVDD3, DVDD4 = 2.7 V, DVDD1, DVDD2 = 5.25 V, C_L = 20 pF, unless otherwise noted.)

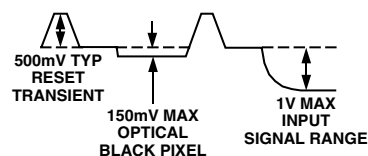
| Parameter | Symbol | Min | Typ | Max | Unit |
|---|--------------|------|-----|------|---------|
| LOGIC INPUTS | | | | | |
| High Level Input Voltage | V_{IH} | 2.1 | | | V |
| Low Level Input Voltage | V_{IL} | | | 0.6 | V |
| High Level Input Current | I_{IH} | | 10 | | μ A |
| Low Level Input Current | I_{IL} | | 10 | | μ A |
| Input Capacitance | C_{IN} | | 10 | | pF |
| LOGIC OUTPUTS | | | | | |
| High Level Output Voltage, $I_{OH} = 2$ mA | V_{OH} | 2.2 | | | V |
| Low Level Output Voltage, $I_{OL} = 2$ mA | V_{OL} | | | 0.5 | V |
| CLI INPUT | | | | | |
| High Level Input Voltage (AVDD1, 2 + 0.5 V) | V_{IH-CLI} | 1.85 | | | V |
| Low Level Input Voltage | V_{IL-CLI} | | | 0.85 | V |
| RG AND H-DRIVER OUTPUTS | | | | | |
| High Level Output Voltage (DVDD1, 2 – 0.5 V) | V_{OH} | 4.75 | | | V |
| Low Level Output Voltage | V_{OL} | | | 0.5 | V |
| Maximum Output Current (Programmable) | | 24 | | | mA |
| Maximum Load Capacitance | | 100 | | | pF |

Specifications subject to change without notice.

ANALOG SPECIFICATIONS (T_{MIN} to T_{MAX} , $AVDD = DVDD = 3.0\text{ V}$, $f_{CLI} = 40\text{ MHz}$, unless otherwise noted.)

| Parameter | Min | Typ | Max | Unit | Notes |
|--|-----|------------|-----------|---------|---|
| CDS | | | | | |
| Gain | | 0 | | dB | |
| Allowable CCD Reset Transient* | | 500 | | mV | |
| Max Input Range before Saturation* | 1.0 | | | V p-p | |
| Max CCD Black Pixel Amplitude* | | 150 | | mV | |
| PIXEL GAIN AMPLIFIER ($PxGA$) | | | | | |
| Max Input Range | 1.0 | | | V p-p | |
| Max Output Range | 1.6 | | | V p-p | |
| Gain Control Resolution | | 64 | | Steps | |
| Gain Monotonicity | | Guaranteed | | | |
| Gain Range | | | | | |
| Min Gain (32) | | -2 | | dB | |
| Med Gain (0) | | 4 | | dB | Med Gain (4 dB) Is Default Setting |
| Max Gain (31) | | 10 | | dB | |
| VARIABLE GAIN AMPLIFIER (VGA) | | | | | |
| Max Input Range | 1.6 | | | V p-p | |
| Max Output Range | 2.0 | | | V p-p | |
| Gain Control Resolution | | 1024 | | Steps | |
| Gain Monotonicity | | Guaranteed | | | |
| Gain Range | | | | | |
| Low Gain (91) | | 2 | | dB | |
| Max Gain (1023) | | 36 | | dB | |
| BLACK LEVEL CLAMP | | | | | |
| Clamp Level Resolution | | 256 | | Steps | |
| Clamp Level | | | | | Measured at ADC Output |
| Min Clamp Level (0) | | 0 | | LSB | |
| Max Clamp Level (255) | | 63.75 | | LSB | |
| A/D CONVERTER | | | | | |
| Resolution | 10 | | | Bits | |
| Differential Nonlinearity (DNL) | | ± 0.4 | ± 1.0 | LSB | |
| No Missing Codes | | Guaranteed | | | |
| Full-Scale Input Voltage | | 2.0 | | V | |
| VOLTAGE REFERENCE | | | | | |
| Reference Top Voltage (VRT) | | 2.0 | | V | |
| Reference Bottom Voltage (VRB) | | 1.0 | | V | |
| SYSTEM PERFORMANCE | | | | | |
| Gain Accuracy | | | | | Specifications Include Entire Signal Chain Gain Includes 4 dB Default $PxGA$ |
| Low Gain (91) | 5 | 6 | 7 | dB | |
| Max Gain (1023) | | 38 | | dB | |
| Peak Nonlinearity, 500 mV Input Signal | | 0.2 | | % | 12 dB Gain Applied |
| Total Output Noise | | 0.25 | | LSB rms | AC Grounded Input, 6 dB Gain Applied |
| Power Supply Rejection (PSR) | | 40 | | dB | Measured with Step Change on Supply |

*Input signal characteristics defined as follows:



Specifications subject to change without notice.

AD9847

TIMING SPECIFICATIONS (C_L to 29 pF, f_{CLI} = 40 MHz, Serial Timing in Figures 3a and 3b, unless otherwise noted.)

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---------------------|------|-----|-----|--------|
| MASTER CLOCK (CLI) | | | | | |
| CLI Clock Period | t _{CLI} | 25 | | | ns |
| CLI High/Low Pulsewidth | t _{ADC} | 12.5 | | | ns |
| Delay from CLI to Internal Pixel Period Position | t _{CLIDLY} | | 6 | | ns |
| EXTERNAL MODE CLAMPING | | | | | |
| CLPDM Pulsewidth | t _{CDM} | 4 | 10 | | Pixels |
| CLPOB Pulsewidth* | t _{COB} | 2 | 20 | | Pixels |
| SAMPLE CLOCKS | | | | | |
| SHP Rising Edge to SHD Rising Edge | t _{S1} | 10 | | | ns |
| DATA OUTPUTS | | | | | |
| Output Delay from Programmed Edge | t _{OD} | | 6 | | ns |
| Pipeline Delay | | | 9 | | Cycles |
| SERIAL INTERFACE | | | | | |
| Maximum SCK Frequency | f _{SCLK} | 10 | | | MHz |
| SL to SCK Setup Time | t _{LS} | 10 | | | ns |
| SCK to SL Hold Time | t _{LH} | 10 | | | ns |
| SDATA Valid to SCK Rising Edge Setup | t _{DS} | 10 | | | ns |
| SCK Falling Edge to SDATA Valid Hold | t _{DH} | 10 | | | ns |
| SCK Falling Edge to SDATA Valid Read | t _{DV} | 10 | | | ns |

*Maximum CLPOB pulsewidth is for functional operation only. Wider typical pulses are recommended to achieve low noise clamp reference.
Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS

| | |
|----------------------------|-----------------------|
| AVDD1, 2, 3 to AVSS | −0.3 to +3.9 V |
| DVDD1, 2 to DVSS | −0.3 to +5.5 V |
| DVDD3, 4 to DVSS | −0.3 to +3.9 V |
| Digital Outputs to DVSS3 | −0.3 to DVDD3 + 0.3 V |
| CLPOB, CLPDM, BLK to DVSS4 | −0.3 to DVDD4 + 0.3 V |
| CLI to AVSS | −0.3 to AVDD + 0.3 V |
| SCK, SL, SDATA to DVSS4 | −0.3 to DVDD4 + 0.3 V |
| VRT, VRB to AVSS | −0.3 to AVDD + 0.3 V |
| BYP1–3, CCDIN to AVSS | −0.3 to AVDD + 0.3 V |
| Junction Temperature | 150°C |
| Lead Temperature (10 sec) | 300°C |

THERMAL CHARACTERISTICS

| | |
|---------------------------|---|
| Thermal Resistance | |
| 48-Lead LQFP Package | $\theta_{JA} = 92^{\circ}\text{C}/\text{W}$ |

ORDERING GUIDE

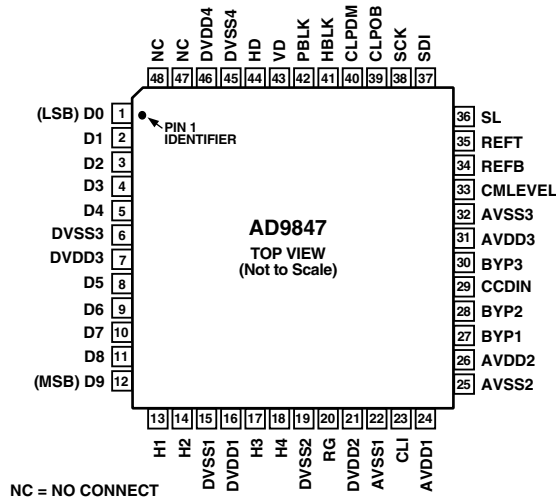
| Model | Temperature Range | Package Description | Package Option |
|------------|-------------------|-----------------------------------|----------------|
| AD9847AKST | −20°C to +85°C | Thin Plastic Quad Flatpack (LQFP) | ST-48 |

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD9847 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



PIN CONFIGURATION

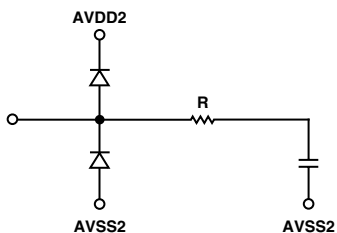


PIN FUNCTION DESCRIPTIONS

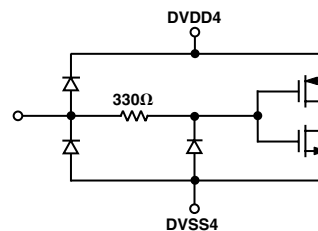
| Pin No. | Mnemonic | Type* | Description |
|---------|----------|-------|---|
| 1–5 | D0–D4 | DO | Data Outputs |
| 6 | DVSS3 | P | Digital Ground 3—Data Outputs |
| 7 | DVDD3 | P | Digital Supply 3—Data Outputs |
| 8–12 | D5–D9 | DO | Data Outputs (D9 Is MSB) |
| 13, 14 | H1, H2 | DO | Horizontal Clocks (to CCD) |
| 15 | DVSS1 | P | Digital Ground 1—H Drivers |
| 16 | DVDD1 | P | Digital Supply 1—H Drivers |
| 17, 18 | H3, H4 | DO | Horizontal Clocks (to CCD) |
| 19 | DVSS2 | P | Digital Ground 1—RG Driver |
| 20 | RG | DO | Reset Gate Clock (to CCD) |
| 21 | DVDD2 | P | Digital Supply 2—RG Driver |
| 22 | AVSS1 | P | Analog Ground 1 |
| 23 | CLI | DI | Master Clock Input |
| 24 | AVDD1 | P | Analog Supply 1 |
| 25 | AVSS2 | P | Analog Ground 2 |
| 26 | AVDD2 | P | Analog Supply 2 |
| 27 | BYP1 | AO | Bypass Pin (0.1 μ F to AVSS) |
| 28 | BYP2 | AO | Bypass Pin (0.1 μ F to AVSS) |
| 29 | CCDIN | AI | Analog Input for CCD Signal |
| 30 | BYP3 | AO | Bypass Pin (0.1 μ F to AVSS) |
| 31 | AVDD3 | P | Analog Supply 3 |
| 32 | AVSS3 | P | Analog Ground 3 |
| 33 | CMLEVEL | AO | Internal Bias Level Decoupling (0.1 μ F to AVSS) |
| 34 | REFB | AO | Reference Bottom Decoupling (1.0 μ F to AVSS) |
| 35 | REFT | AO | Reference Top Decoupling (1.0 μ F to AVSS) |
| 36 | SL | DI | 3-Wire Serial Load (from μ P) |
| 37 | SDI | DI | 3-Wire Serial Data Input (from μ P) |
| 38 | SCK | DI | 3-Wire Serial Clock (from μ P) |
| 39 | CLPOB | DI | Optical Black Clamp Pulse |
| 40 | CLPDM | DI | Dummy Black Clamp Pulse |
| 41 | HBLK | DI | HCLK Blanking Pulse |
| 42 | PBLK | DI | Preblanking Pulse |
| 43 | VD | DI | Vertical Sync Pulse |
| 44 | HD | DI | Horizontal Sync Pulse |
| 45 | DVSS4 | P | Digital Ground 4—VD, HD, CLPOB, CLPDM, HBLK, PBLK, SCK, SL, SDATA |
| 46 | DVDD4 | P | Digital Supply 4—VD, HD, CLPOB, CLPDM, HBLK, PBLK, CK, SL |
| 47, 48 | NC | NC | Internally Not Connected |

*Type: AI = Analog Input, AO = Analog Output, DI = Digital Input, DO = Digital Output, P = Power

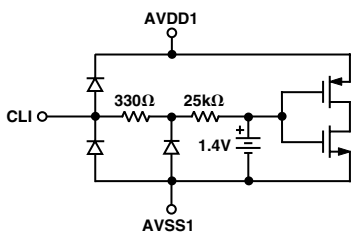
Equivalent Input/Output Circuits



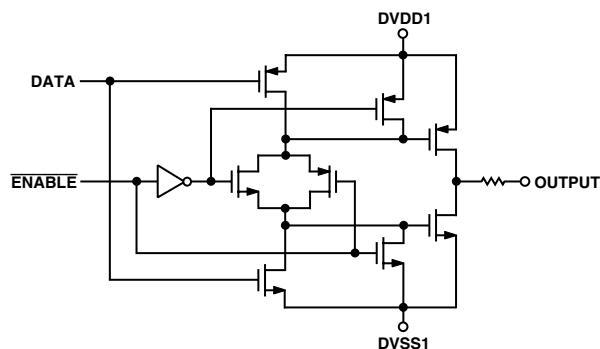
Circuit 1. CCDIN (Pin 29)



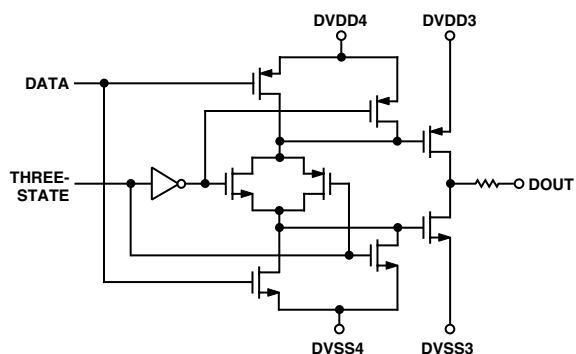
Circuit 4. Digital Inputs (Pins 36-44)



Circuit 2. CLI (Pin 23)

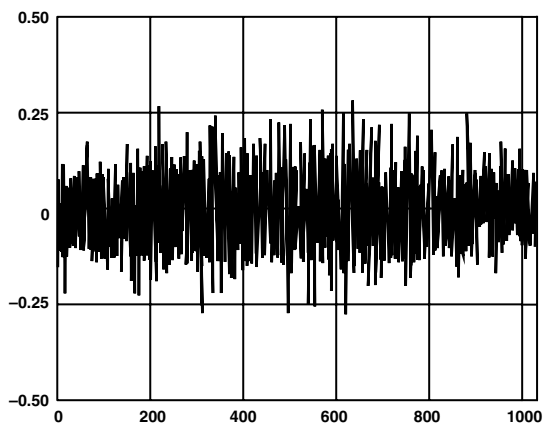


Circuit 5. H1-H4 and RG (Pins 13, 14, 17, 18, 20)

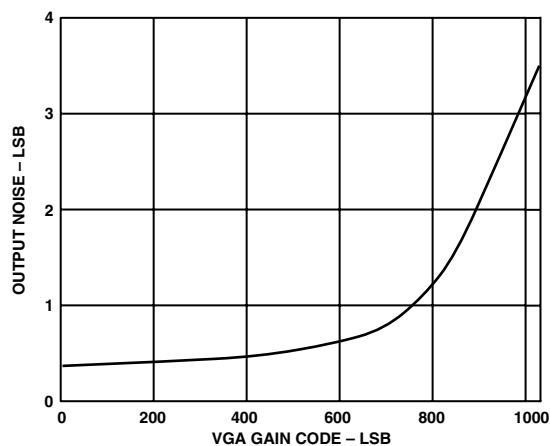


Circuit 3. Data Outputs D0-D9 (Pins 1-5, 8-12)

Typical Performance Characteristics



TPC 1. Typical DNL



TPC 2. Output Noise vs. VGA Gain Setting

AD9847

SYSTEM OVERVIEW

Figures 1a and 1b show the typical system application diagrams for the AD9847. The CCD output is processed by the AD9847's AFE circuitry, which consists of a CDS, P_xGA , VGA, black level clamp, and A/D converter. The digitized pixel information is sent to the digital image processor chip, where all post-processing and compression occurs. To operate the CCD, CCD timing parameters are programmed into the AD9847 from the image processor through the 3-wire serial interface. From the system master clock, CLI, provided by the image processor, the AD9847 generates the high speed CCD clocks and all internal AFE clocks. All AD9847 clocks are synchronized with VD and HD.

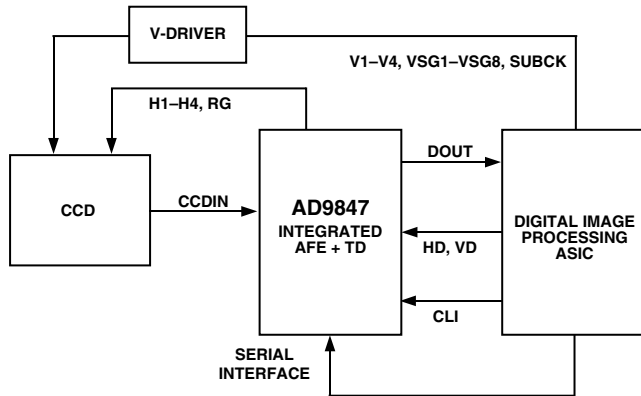


Figure 1a. Typical Application (Internal Mode)

Figure 1a shows the AD9847 used in internal mode, in which all the horizontal pulses (CLPOB, CLPDM, PBLK, and HBLK) are programmed and generated internally. Figure 1b shows the AD9847 operating in external mode, in which the horizontal pulses are supplied externally by the image processor.

The H-drivers for H1-H4 and RG are included in the AD9847, allowing these clocks to be directly connected to the CCD. The AD9847 supports H-drive voltage of 5 V.

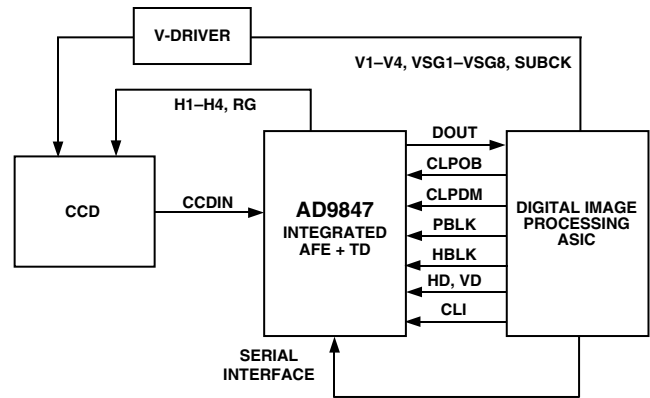


Figure 1b. Typical Application (External Mode)

Figure 2 shows the horizontal and vertical counter dimensions for the AD9847. All internal horizontal clocking is programmed using these dimensions to specify line and pixel locations.

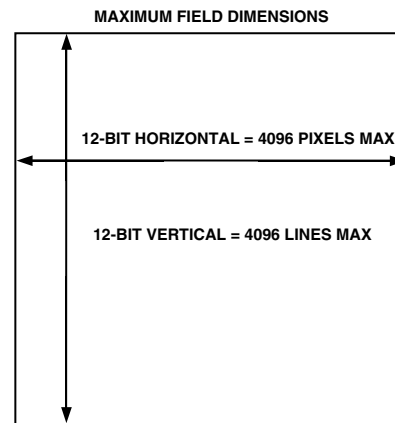


Figure 2. Vertical and Horizontal Counters

SERIAL INTERFACE TIMING

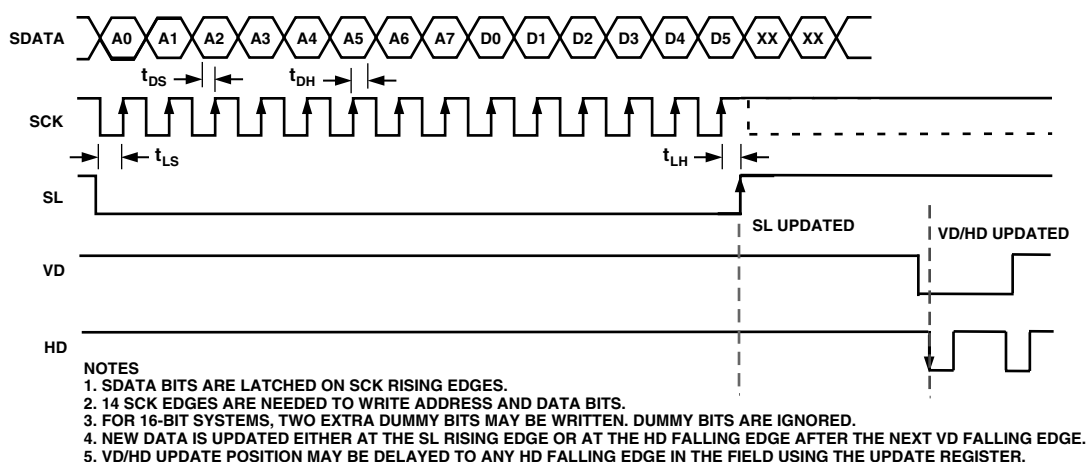


Figure 3a. Serial Write Operation

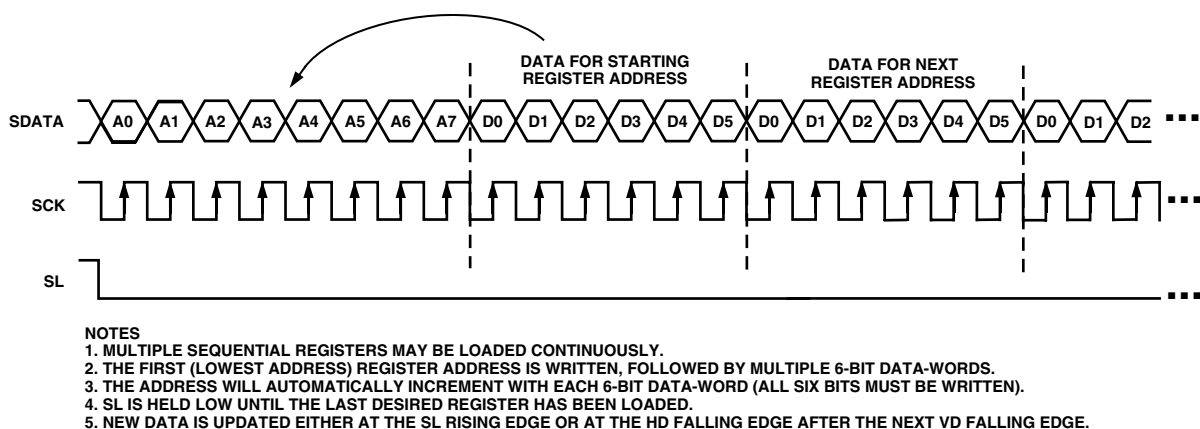


Figure 3b. Continuous Serial Write Operation

COMPLETE REGISTER LISTING

Table I. SL Updated Registers

| Register | Description | Register | Description |
|--------------|--|-----------|---------------------------|
| oprmode | AFE Operation Modes | h1drv | H1 Drive Current |
| ctlmode | AFE Control Modes | h2drv | H2 Drive Current |
| preventpdate | Prevents Loading of VD-Updated Registers | h3drv | H3 Drive Current |
| readback | Enables Serial Register Readback Mode | h4drv | H4 Drive Current |
| vdhdpol | VD/HD Active Polarity | rgpol | RG Polarity |
| fieldval | Internal Field Pulse Value | rgposloc | RG Positive Edge Location |
| hblkretime | Retimes the H1 hblk to Internal Clock | rgnegloc | RG Negative Edge Location |
| tgcore_rstb | Reset Bar Signal for Internal TG Core | rgdrv | RG Drive Current |
| h12pol | H1/H2 Polarity Control | shposloc | SHP Sample Location |
| h1posloc | H1 Positive Edge Location | shdposloc | SHD Sample Location |
| h1negloc | H1 Negative Edge Location | | |

NOTES

All addresses and default values are expressed in hexadecimal.

All registers are VD/HD updated as shown in Figure 3a, except for those that are SL updated.

AD9847

Accessing a Double-Wide Register

There are many double-wide registers in the AD9847, e.g., oprmode, clpdmto1_0, and clpdmscp3, and so on. These registers are configured into two consecutive 6-bit registers with the least significant six bits located in the lower of the two addresses and the remaining most significant bits located in the higher of the two addresses. For example, the six LSBs of the clpdmscp3 register, clpdmscp3[5:0], are located at address 0x81. The most significant six bits of the clpdmscp3 register, clpdmscp3[11:6], are located at Address 0x82. The following rules must be followed when accessing double-wide registers:

1. When accessing a double-wide register, BOTH addresses must be written to.
2. The lower of the two consecutive addresses for the double-wide register must be written to first. In the example of the

clpdmscp3 register, the contents of Address 0x81 must be written first, followed by the contents of Address 0x82. The register will be updated after the completion of the write to Register 0x82, either at the next SL rising edge or the next VD/HD falling edge.

3. A single write to the lower of the two consecutive addresses of a double-wide register that is not followed by a write to the higher address of the registers is not permitted. This will not update the register.
4. A single write to the higher of the two consecutive addresses of a double-wide register that is not preceded by a write to the lower of the two addresses is not permitted. Although the write to the higher address will update the full double-wide register, the lower six bits of the register will be written with an indeterminate value if the lower address was not written to first.

| Address | Bit Content | Width | Default Value | Register Name | Register Description |
|--------------------------------|-------------|-------|---------------|---------------|---|
| AFE Registers # Bits 56 | | | | | |
| 00 | [5:0] | 6 | 00 | oprmode[5:0] | AFE Operation Mode (See AFE Register Breakdown) |
| 01 | [1:0] | 2 | 00 | oprmode[7:6] | |
| 02 | [5:0] | 6 | 16 | ccdgain[5:0] | VGA Gain |
| 03 | [3:0] | 4 | 02 | ccdgain[9:6] | |
| 04 | [5:0] | 6 | 00 | refblack[5:0] | Black Clamp Level |
| 05 | [1:0] | 2 | 02 | refblack[7:6] | |
| 06 | [5:0] | 6 | 00 | ctlmode | Control Mode (See AFE Register Breakdown) |
| 07 | [5:0] | 6 | 00 | pxga gain0 | PxGA Color 0 Gain |
| 08 | [5:0] | 6 | 00 | pxga gain1 | PxGA Color 1 Gain |
| 09 | [5:0] | 6 | 00 | pxga gain2 | PxGA Color 2 Gain |
| 0A | [5:0] | 6 | 00 | pxga gain3 | PxGA Color 3 Gain |

Miscellaneous/Extra # Bits 26

| | | | | | |
|----|-------|---|----|----------------|---|
| 0F | [5:0] | 6 | 00 | INITIAL2 | See Recommended Power Up Sequence Section. Should be set to "4" decimal (000100). |
| 16 | [0] | 1 | 00 | out_cont | Output Control (0 = Make All Outputs DC Inactive) |
| 17 | [5:0] | 6 | 00 | update[5:0] | Serial Data Update Control (Sets the line within the field for serial data update to occur) |
| 18 | [5:0] | 6 | 00 | update[11:6] | |
| 19 | [0] | 1 | 00 | preventupdate | Prevent the Update of the VD/HD Updated Registers |
| 1B | [5:0] | 6 | 00 | doutphase | DOUT Phase Control |
| 1C | [0] | 1 | 00 | disablerestore | Disable CCDIN DC Restore Circuit During PBLK (1 = Disable) |
| 1D | [0] | 1 | 00 | vdhdpol | VD/HD Active Polarity (0 = Low Active, 1 = High Active) |
| 1E | [0] | 1 | 01 | fieldval | Internal Field Pulse Value (0 = Next Field Odd, 1 = Next Field Even) |
| 1F | [0] | 1 | 00 | hblkretime | Re-Sync hblk to h1 Clock |
| 20 | [5:0] | 6 | 00 | INITIAL1 | See Recommended Power Up Sequence. Should be set to "53" decimal (110101). |
| 26 | [0] | 1 | 00 | tgcore_rstb | TG Core Reset_Bar (0 = Hold TG Core in Reset, 1 = Resume Normal Operation) |

| Address | Bit Content | Width | Default Value | Register Name | Register Description |
|-------------------------|-------------|-------|---------------|-------------------|--|
| CLPDM # Bits 146 | | | | | |
| 64 | [0] | 1 | 01 | clpdmkdir | CLPDM Internal/External (0 = Internal, 1 = External) |
| 65 | [0] | 1 | 00 | clpdmopol | CLPDM External Active Polarity (0 = Low Active, 1 = High Active) |
| 66 | [0] | 1 | 01 | clpdmspol0 | Sequence #0: Start Polarity for CLPDM |
| 67 | [5:0] | 6 | 2C | clpdmtog1_0[5:0] | Sequence #0: Toggle Position 1 for CLPDM |
| 68 | [5:0] | 6 | 00 | clpdmtog1_0[11:6] | |
| 69 | [5:0] | 6 | 35 | clpdmtog2_0[5:0] | Sequence #0: Toggle Position 2 for CLPDM |
| 6A | [5:0] | 6 | 00 | clpdmtog2_0[11:6] | |
| 6B | [0] | 1 | 01 | clpdmspol1 | Sequence #1: Start Polarity for CLPDM |
| 6C | [5:0] | 6 | 3E | clpdmtog1_1[5:0] | Sequence #1: Toggle Position 1 for CLPDM |
| 6D | [5:0] | 6 | 02 | clpdmtog1_1[11:6] | |
| 6E | [5:0] | 6 | 16 | clpdmtog2_1[5:0] | Sequence #1: Toggle Position 2 for CLPDM |
| 6F | [5:0] | 6 | 03 | clpdmtog2_1[11:6] | |
| 70 | [0] | 1 | 00 | clpdmspol2 | Sequence #2: Start Polarity for CLPDM |
| 71 | [5:0] | 6 | 3F | clpdmtog1_2[5:0] | Sequence #2: Toggle Position 1 for CLPDM |
| 72 | [5:0] | 6 | 3F | clpdmtog1_2[11:6] | |
| 73 | [5:0] | 6 | 3F | clpdmtog2_2[5:0] | Sequence #2: Toggle Position 2 for CLPDM |
| 74 | [5:0] | 6 | 3F | clpdmtog2_2[11:6] | |
| 75 | [0] | 1 | 01 | clpdmspol3 | Sequence #3: Start Polarity for CLPDM |
| 76 | [5:0] | 6 | 3F | clpdmtog1_3[5:0] | Sequence #3: Toggle Position 1 for CLPDM |
| 77 | [5:0] | 6 | 3F | clpdmtog1_3[11:6] | |
| 78 | [5:0] | 6 | 3F | clpdmtog2_3[5:0] | Sequence #3: Toggle Position 2 for CLPDM |
| 79 | [5:0] | 6 | 3F | clpdmtog2_3[11:6] | |
| | | 0 | 00 | clpdmscp0 | CLPDM Sequence-Change-Position #0 (Hardcoded to 0) |
| 7A | [1:0] | 2 | 00 | clpdmsptr0 | CLPDM Sequence Pointer for SCP #0 |
| 7B | [5:0] | 6 | 3F | clpdmscp1[5:0] | CLPDM Sequence-Change-Position #1 |
| 7C | [5:0] | 6 | 3F | clpdmscp1[11:6] | |
| 7D | [1:0] | 2 | 00 | clpdmsptr1 | CLPDM Sequence Pointer for SCP #1 |
| 7E | [5:0] | 6 | 3F | clpdmscp2[5:0] | CLPDM Sequence-Change-Position #2 |
| 7F | [5:0] | 6 | 3F | clpdmscp2[11:6] | |
| 80 | [1:0] | 2 | 00 | clpdmsptr2 | CLPDM Sequence Pointer for SCP #2 |
| 81 | [5:0] | 6 | 3F | clpdmscp3[5:0] | CLPDM Sequence-Change-Position #3 |
| 82 | [5:0] | 6 | 3F | clpdmscp3[11:6] | |
| 83 | [1:0] | 2 | 00 | clpdmsptr3 | CLPDM Sequence Pointer for SCP #3 |

AD9847

| Address | Bit Content | Width | Default Value | Register Name | Register Description |
|-------------------------|-------------|-------|---------------|-------------------|--|
| CLPOB # Bits 146 | | | | | |
| 84 | [0] | 1 | 01 | clpobdir | CLPOB Internal/External (0 = Internal, 1 = External) |
| 85 | [0] | 1 | 00 | clpobpol | CLPOB External Active Polarity (0 = Low Active, 1 = High Active) |
| 86 | [0] | 1 | 01 | clpobpol0 | Sequence #0: Start Polarity for CLPOB |
| 87 | [5:0] | 6 | 0E | clpobtog1_0[5:0] | Sequence #0: Toggle Position 1 for CLPOB |
| 88 | [5:0] | 6 | 00 | clpobtog1_0[11:6] | |
| 89 | [5:0] | 6 | 2B | clpobtog2_0[5:0] | Sequence #0: Toggle Position 2 for CLPOB |
| 8A | [5:0] | 6 | 00 | clpobtog2_0[11:6] | |
| 8B | [0] | 1 | 01 | clpobpol1 | Sequence #1: Start Polarity for CLPOB |
| 8C | [5:0] | 6 | 2B | clpobtog1_1[5:0] | Sequence #1: Toggle Position 1 for CLPOB |
| 8D | [5:0] | 6 | 06 | clpobtog1_1[11:6] | |
| 8E | [5:0] | 6 | 3F | clpobtog2_1[5:0] | Sequence #1: Toggle Position 2 for CLPOB |
| 8F | [5:0] | 6 | 3F | clpobtog2_1[11:6] | |
| 90 | [0] | 1 | 00 | clpobspol2 | Sequence #2: Start Polarity for CLPOB |
| 91 | [5:0] | 6 | 3F | clpobtog1_2[5:0] | Sequence #2: Toggle Position 1 for CLPOB |
| 92 | [5:0] | 6 | 3F | clpobtog1_2[11:6] | |
| 93 | [5:0] | 6 | 3F | clpobtog2_2[5:0] | Sequence #2: Toggle Position 2 for CLPOB |
| 94 | [5:0] | 6 | 3F | clpobtog2_2[11:6] | |
| 95 | [0] | 1 | 01 | clpobspol3 | Sequence #3: Start Polarity for CLPOB |
| 96 | [5:0] | 6 | 3F | clpobtog1_3[5:0] | Sequence #3: Toggle Position 1 for CLPOB |
| 97 | [5:0] | 6 | 3F | clpobtog1_3[11:6] | |
| 98 | [5:0] | 6 | 3F | clpobtog2_3[5:0] | Sequence #3: Toggle Position 2 for CLPOB |
| 99 | [5:0] | 6 | 3F | clpobtog2_3[11:6] | |
| | | 0 | 00 | clpobscp0 | CLPOB Sequence-Change-Position #0 (Hardcoded to 0) |
| 9A | [1:0] | 2 | 03 | clpobsptr0 | CLPOB Sequence Pointer for SCP #0 |
| 9B | [5:0] | 6 | 01 | clpobscp1[5:0] | CLPOB Sequence-Change-Position #1 |
| 9C | [5:0] | 6 | 00 | clpobscp1[11:6] | |
| 9D | [1:0] | 2 | 01 | clpobsptr1 | CLPOB Sequence Pointer for SCP #1 |
| 9E | [5:0] | 6 | 02 | clpobscp2[5:0] | CLPOB Sequence-Change-Position #2 |
| 9F | [5:0] | 6 | 00 | clpobscp2[11:6] | |
| A0 | [1:0] | 2 | 00 | clpobsptr2 | CLPOB Sequence Pointer for SCP #2 |
| A1 | [5:0] | 6 | 37 | clpobscp3[5:0] | CLPOB Sequence-Change-Position #3 |
| A2 | [5:0] | 6 | 03 | clpobscp3[11:6] | |
| A3 | [1:0] | 2 | 03 | clpobsptr3 | CLPOB Sequence Pointer for SCP #3 |

| Address | Bit Content | Width | Default Value | Register Name | Register Description |
|------------------------|-------------|-------|---------------|-------------------|--|
| HBLK # Bits 147 | | | | | |
| A4 | [0] | 1 | 01 | hblkdir | HBLK Internal/External (0 = Internal, 1 = External) |
| A5 | [0] | 1 | 00 | hblkpol | HBLK External Active Polarity (0 = Low Active, 1 = High Active) |
| A6 | [0] | 1 | 01 | hblkextmask | HBLK External Masking Polarity (0 = Mask H1 and H3 Low, 1 = Mask H1 and H3 High) |
| A7 | [0] | 1 | 01 | hblkmask0 | Sequence #0: Masking Polarity for HBLK |
| A8 | [5:0] | 6 | 3E | hblktog1_0[5:0] | Sequence #0: Toggle Low Position for HBLK |
| A9 | [5:0] | 6 | 00 | hblktog1_0[11:6] | |
| AA | [5:0] | 6 | 0D | hblkbtog2_0[5:0] | Sequence #0: Toggle High Position for HBLK |
| AB | [5:0] | 6 | 06 | hblkbtog2_0[11:6] | |
| AC | [0] | 1 | 01 | hblkmask1 | Sequence #1: Masking Polarity for HBLK |
| AD | [5:0] | 6 | 38 | hblktog1_1[5:0] | Sequence #1: Toggle Low Position for HBLK |
| AE | [5:0] | 6 | 00 | hblktog1_1[11:6] | |
| AF | [5:0] | 6 | 3C | hblktog2_1[5:0] | Sequence #1: Toggle High Position for HBLK |
| B0 | [5:0] | 6 | 02 | hblktog2_1[11:6] | |
| B1 | [0] | 1 | 00 | hblkmask2 | Sequence #2: Masking Polarity for HBLK |
| B2 | [5:0] | 6 | 3F | hblktog1_2[5:0] | Sequence #2: Toggle Low Position for HBLK |
| B3 | [5:0] | 6 | 3F | hblktog1_2[11:6] | |
| B4 | [5:0] | 6 | 3F | hblktog2_2[5:0] | Sequence #2: Toggle High Position for HBLK |
| B5 | [5:0] | 6 | 3F | hblktog2_2[11:6] | |
| B6 | [0] | 1 | 01 | hblkmask3 | Sequence #3: Masking Polarity for HBLK |
| B7 | [5:0] | 6 | 3F | hblktog1_3[5:0] | Sequence #3: Toggle Low Position for HBLK |
| B8 | [5:0] | 6 | 3F | hblktog1_3[11:6] | |
| B9 | [5:0] | 6 | 3F | hblktog2_3[5:0] | Sequence #3: Toggle High Position for HBLK |
| BA | [5:0] | 6 | 3F | hblktog2_3[11:6] | |
| | | 0 | 00 | hblkscp0 | HBLK Sequence-Change-Position #0 (Hardcoded to 0) |
| BB | [1:0] | 2 | 00 | hblksptr0 | HBLK Sequence Pointer for SCP #0 |
| BC | [5:0] | 6 | 3F | hblkscp1[5:0] | HBLK Sequence-Change-Position #1 |
| BD | [5:0] | 6 | 3F | hblkscp1[11:6] | |
| BE | [1:0] | 2 | 00 | hblksptr1 | HBLK Sequence Pointer for SCP #1 |
| BF | [5:0] | 6 | 3F | hblkscp2[5:0] | HBLK Sequence-Change-Position #2 |
| C0 | [5:0] | 6 | 3F | hblkscp2[11:6] | |
| C1 | [1:0] | 2 | 00 | hblksptr2 | HBLK Sequence Pointer for SCP #2 |
| C2 | [5:0] | 6 | 3F | hblkscp3[5:0] | HBLK Sequence-Change-Position #3 |
| C3 | [5:0] | 6 | 3F | hblkscp3[11:6] | |
| C4 | [1:0] | 2 | 00 | hblksptr3 | HBLK Sequence Pointer for SCP #3 |

AD9847

| Address | Bit Content | Width | Default Value | Register Name | Register Description |
|------------------------|-------------|-------|---------------|-------------------|---|
| PBLK # Bits 146 | | | | | |
| C5 | [0] | 1 | 01 | pblkdir | PBLK Internal/External (0 = Internal, 1 = External) |
| C6 | [0] | 1 | 00 | pblkspol | PBLK External Active Polarity (0 = Low Active, 1 = High Active) |
| C7 | [0] | 1 | 01 | pblkspol0 | Sequence #0: Start Polarity for PBLK |
| C8 | [5:0] | 6 | 3D | pblktog1_0[5:0] | Sequence #0: Toggle Position 1 for PBLK |
| C9 | [5:0] | 6 | 00 | pblktog1_0[11:6] | |
| CA | [5:0] | 6 | 2A | pblkbtog2_0[5:0] | Sequence #0: Toggle Position 2 for PBLK |
| CB | [5:0] | 6 | 06 | pblkbtog2_0[11:6] | |
| CC | [0] | 1 | 00 | pblkspol1 | Sequence #1: Start Polarity for PBLK |
| CD | [5:0] | 6 | 2A | pblktog1_1[5:0] | Sequence #1: Toggle Position 1 for PBLK |
| CE | [5:0] | 6 | 06 | pblktog1_1[11:6] | |
| CF | [5:0] | 6 | 3F | pblktog2_1[5:0] | Sequence #1: Toggle Position 2 for PBLK |
| D0 | [5:0] | 6 | 3F | pblktog2_1[11:6] | |
| D1 | [0] | 1 | 00 | pblkspol2 | Sequence #2: Start Polarity for PBLK |
| D2 | [5:0] | 6 | 3F | pblktog1_2[5:0] | Sequence #2: Toggle Position 1 for PBLK |
| D3 | [5:0] | 6 | 3F | pblktog1_2[11:6] | |
| D4 | [5:0] | 6 | 3F | pblktog2_2[5:0] | Sequence #2: Toggle Position 2 for PBLK |
| D5 | [5:0] | 6 | 3F | pblktog2_2[11:6] | |
| D6 | [0] | 1 | 01 | pblkspol3 | Sequence #3: Start Polarity for PBLK |
| D7 | [5:0] | 6 | 3F | pblktog1_3[5:0] | Sequence #3: Toggle Position 1 for PBLK |
| D8 | [5:0] | 6 | 3F | pblktog1_3[11:6] | |
| D9 | [5:0] | 6 | 3F | pblktog2_3[5:0] | Sequence #3: Toggle Position 2 for PBLK |
| DA | [5:0] | 6 | 3F | pblktog2_3[11:6] | |
| | | 0 | 00 | pblkscp0 | PBLK Sequence-Change-Position #0 (Hardcoded to 0) |
| DB | [1:0] | 2 | 02 | pblksptr0 | PBLK Sequence Pointer for SCP #0 |
| DC | [5:0] | 6 | 01 | pblkscp1[5:0] | PBLK Sequence-Change-Position #1 |
| DD | [5:0] | 6 | 00 | pblkscp1[11:6] | |
| DE | [1:0] | 2 | 01 | pblksptr1 | PBLK Sequence Pointer for SCP #1 |
| DF | [5:0] | 6 | 02 | pblkscp2[5:0] | PBLK Sequence-Change-Position #2 |
| E0 | [5:0] | 6 | 00 | pblkscp2[11:6] | |
| E1 | [1:0] | 2 | 00 | pblksptr2 | PBLK Sequence Pointer for SCP #2 |
| E2 | [5:0] | 6 | 37 | pblkscp3[5:0] | PBLK Sequence-Change-Position #3 |
| E3 | [5:0] | 6 | 03 | pblkscp3[11:6] | |
| E4 | [1:0] | 2 | 02 | pblksptr3 | PBLK Sequence Pointer for SCP #3 |

H1-H4, RG, SHP, SHD # Bits 53

| | | | | | |
|----|-------|---|----|-----------|--|
| E5 | [0] | 1 | 00 | h1pol | H1/H2 Polarity Control (0 = No Inversion, 1 = Inversion) |
| E6 | [5:0] | 6 | 00 | h1posloc | H1 Positive Edge Location |
| E7 | [5:0] | 6 | 20 | h1negloc | H1 Negative Edge Location |
| E8 | [2:0] | 3 | 03 | h1drv | H1 Drive Strength (0 = OFF, 1 = 3.5 mA, 2 = 7 mA, 3 = 10.5 mA, 4 = 14 mA, 5 = 17.5 mA, 6 = 21 mA, 7 = 24.5 mA) |
| E9 | [2:0] | 3 | 03 | h2drv | H2 Drive Strength |
| EA | [2:0] | 3 | 03 | h3drv | H3 Drive Strength |
| EB | [2:0] | 3 | 03 | h4drv | H4 Drive Strength |
| EC | [0] | 1 | 00 | rgpol | RG Polarity Control (0 = No Inversion, 1 = Inversion) |
| ED | [5:0] | 6 | 00 | rgposloc | RG Positive Edge Location |
| EE | [5:0] | 6 | 10 | rgnegloc | RG Negative Edge Location |
| EF | [2:0] | 3 | 02 | rgdrv | RG Drive Strength (0 = OFF, 1 = 3.5 mA, 2 = 7 mA, 3 = 10.5 mA, 4 = 14 mA, 5 = 17.5 mA, 6 = 21 mA, 7 = 24.5 mA) |
| F0 | [5:0] | 6 | 24 | shpposloc | SHP (Positive) Edge Sampling Location |
| F1 | [5:0] | 6 | 00 | shdposloc | SHD (Positive) Edge Sampling Location |

| Address | Bit Content | Width | Default Value | Register Name | Register Description |
|-------------------------------|--------------|--|---------------|----------------|--|
| AFE Register Breakdown | | | | | |
| oprmode | [7:0] | | 8'h0 | | Serial Address: 8'h00 {oprmode[5:0]}, 8'h01 {oprmode[7:6]} |
| | [1:0] | 2'h0 2'h1 2'h2 2'h3 | | powerdown[1:0] | Full Power Fast Recovery Reference Standby Total Shutdown |
| | [2] | | | disblack | Disable Black Loop Clamping (High Active) |
| | [3] | | | test mode | Test Mode—Should Be Set Low |
| | [4] | | | test mode | Test Mode—Should Be Set High |
| | [5] | | | test mode | Test Mode—Should Be Set Low |
| | [6] | | | test mode | Test Mode—Should Be Set Low |
| | [7] | | | test mode | Test Mode—Should Be Set Low |
| ctlmode | [5:0] | | 6'h0 | | Serial Address: 8'h06 {ctlmode[5:0]} |
| | [2:0] | 3'h0 3'h1 3'h2 3'h3 3'h4 3'h5 3'h6 3'h7 | | ctlmode[2:0] | Off Mosaic Separate VD Selected/Mosaic Interlaced Mosaic Repeat Three-Color Three-Color II Four-Color Four-Color II |
| | [3] | | | enablepxga | Enable PxGA (High Active) |
| | [4] | 1'h0 1'h1 | | outputlat | Latch Output Data on Selected DOUT Edge Leave Output Latch Transparent |
| | [5] | 1'h0 1'h1 | | tristateout | ADC Outputs Are Driven ADC Outputs Are Three-Stated |

PRECISION TIMING HIGH SPEED TIMING GENERATION

The AD9847 generates flexible high speed timing signals using the *Precision Timing* core. This core is the foundation for generating the timing used for both the CCD and the AFE, the reset gate RG, horizontal drivers H1–H4, and the SHP/SHD sample clocks. A unique architecture makes it routine for the system designer to optimize image quality by providing precise control over the horizontal CCD readout and the AFE correlated double sampling.

Timing Resolution

The *Precision Timing* core uses a $1\times$ master clock input (CLI) as a reference. This clock should be the same as the CCD pixel clock frequency. Figure 4 illustrates how the internal timing core divides the master clock period into 48 steps or edge positions. Therefore, the edge resolution of the *Precision Timing* core is $(t_{CLI}/48)$. For more information on using the CLI input, see the Applications Information section.

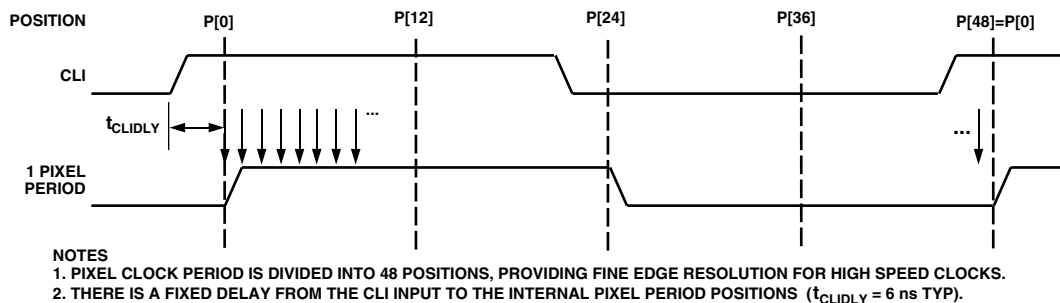


Figure 4. High Speed Clock Resolution from CLI Master Clock Input

AD9847

High Speed Clock Programmability

Figure 5 shows how the high speed clocks RG, H1–H4, SHP, and SHD are generated. The RG pulse has programmable rising and falling edges and may be inverted using the polarity control. The horizontal clocks H1 and H3 have programmable rising and falling edges and polarity control. The H2 and H4 clocks are always inverses of H1 and H3, respectively. Table II summarizes the high speed timing registers and their parameters.

The edge location registers are 6 bits wide, but there are only 48 valid edge locations available. Therefore, the register values are mapped into four quadrants, with each quadrant containing 12 edge locations. Table III shows the correct register values for the corresponding edge locations. Figure 6 shows the range and default locations of the high speed clock signals.

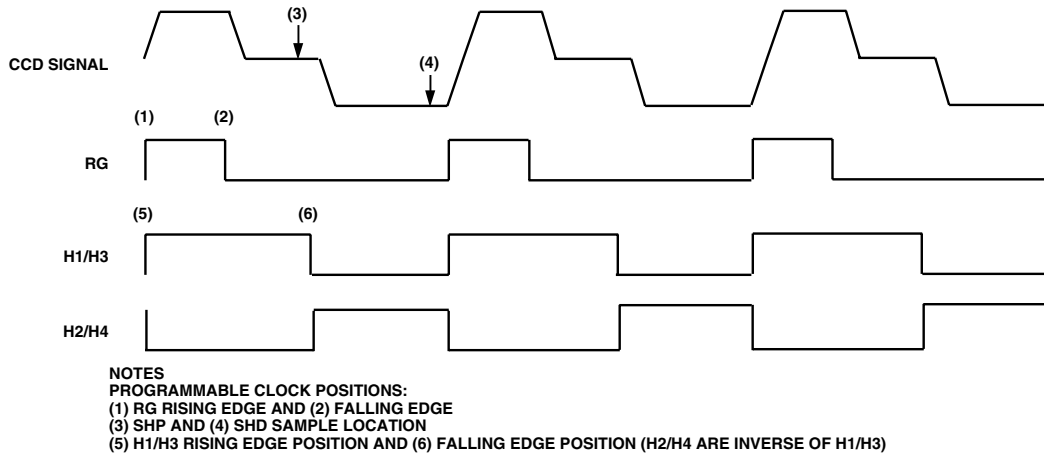


Figure 5. High Speed Clock Programmable Locations

Table II. H1–H4, RG, SHP, SHD Timing Parameters

| Register Name | Length | Range | Description |
|---------------|--------|--------------------|---|
| POL | 1b | High/Low | Polarity Control for H1, H3, and RG (0 = No Inversion, 1 = Inversion) |
| POSLOC | 6b | 0–47 Edge Location | Positive Edge Location for H1, H3, and RG |
| NEGLOC | 6b | 0–47 Edge Location | Negative Edge Location for H1, H3, and RG |
| SHD | 6b | 0–47 Edge Location | Sample Location for SHP, SHD |
| DRV | 3b | 0–7 Current Steps | Drive Current for H1–H4 and RG Outputs (3.5 mA per Step) |

Table III. Precision Timing Edge Locations

| Quadrant | Edge Location (Decimal) | Register Value (Decimal) | Register Value (Binary) |
|----------|-------------------------|--------------------------|-------------------------|
| I | 0 to 11 | 0 to 11 | 000000 to 001011 |
| II | 12 to 23 | 16 to 27 | 010000 to 011011 |
| III | 24 to 35 | 32 to 43 | 100000 to 101011 |
| IV | 36 to 47 | 48 to 59 | 110000 to 111011 |

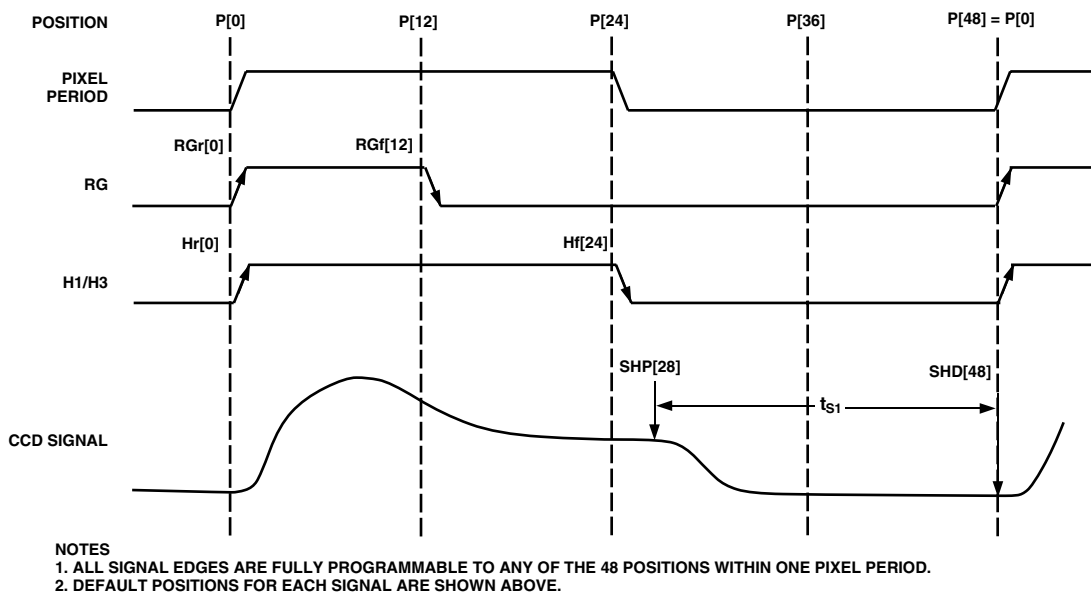


Figure 6. High Speed Clock Default and Programmable Locations

H-Driver and RG Outputs

In addition to the programmable timing positions, the AD9847 features on-chip output drivers for the RG and H1–H4 outputs. These drivers are powerful enough to directly drive the CCD inputs. The H-driver current can be adjusted for optimum rise/fall time into a particular load by using the DRV registers. The RG drive current is adjustable using the RGDRV register. Each 3-bit DRV register is adjustable in 3.5 mA increments, with the minimum setting of 0 equal to OFF or three-state and the maximum setting of 7 equal to 24.5 mA.

As shown in Figure 7, the H2/H4 outputs are inverses of H1/H3. The internal propagation delay resulting from the signal inversion is less than 1 ns, which is significantly less than the typical rise time driving the CCD load. This results in a H1/H2 crossover voltage at approximately 50% of the output swing. The crossover voltage is not programmable.

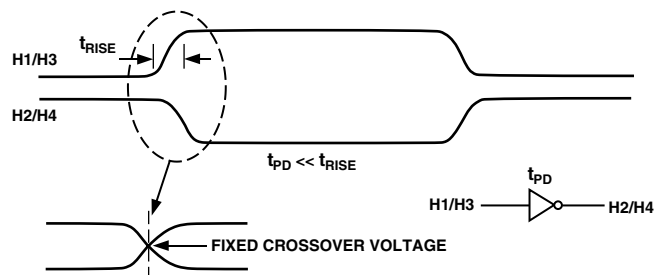


Figure 7. H-Clock Inverse Phase Relationship

Digital Data Outputs

The AD9847 data output phase is programmable using the DOUTPHASE register. Any edge from 0 to 47 may be programmed, as shown in Figure 8.

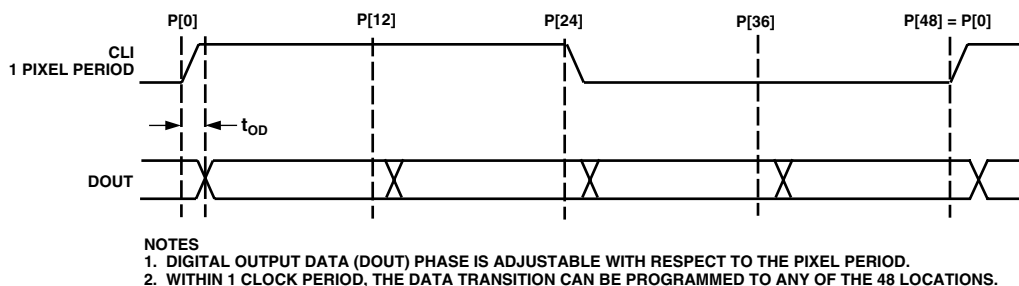


Figure 8. Digital Output Phase Adjustment

AD9847

HORIZONTAL CLAMPING AND BLANKING

The AD9847's horizontal clamping and blanking pulses are fully programmable to suit a variety of applications. As with the vertical timing generation, individual sequences are defined for each signal and are then organized into multiple regions during image readout. This allows the dark pixel clamping and blanking patterns to be changed at each stage of the readout, in order to accommodate different image transfer timing and high speed line shifts.

Individual CLPOB, CLPDM, and PBLK Sequences

The AFE horizontal timing consists of CLPOB, CLPDM, and PBLK, as shown in Figure 9. These three signals are independently programmed using the registers in Table IV. SPOL is the start polarity for the signal, and TOG1 and TOG2 are the first

and second toggle positions of the pulse. All three signals are active low and should be programmed accordingly. Up to four individual sequences can be created for each signal.

Individual HBLK Sequences

The HBLK programmable timing shown in Figure 10 is similar to CLPOB, CLPDM, and PBLK. However, there is no start polarity control. Only the toggle positions are used to designate the start and the stop positions of the blanking period. Additionally, there is a polarity control, HBLKMASK, that designates the polarity of the horizontal clock signals H1–H4 during the blanking period. Setting HBLKMASK high will set H1 = H3 = low and H2 = H4 = high during the blanking, as shown in Figure 11. Up to four individual sequences are available for HBLK.

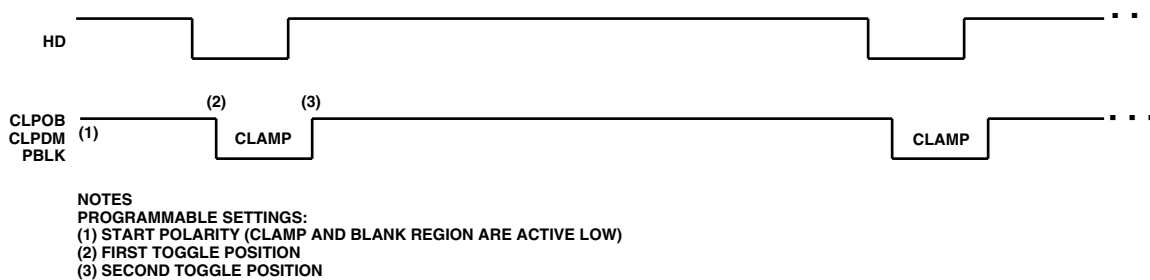


Figure 9. Clamp and Preblank Pulse Placement

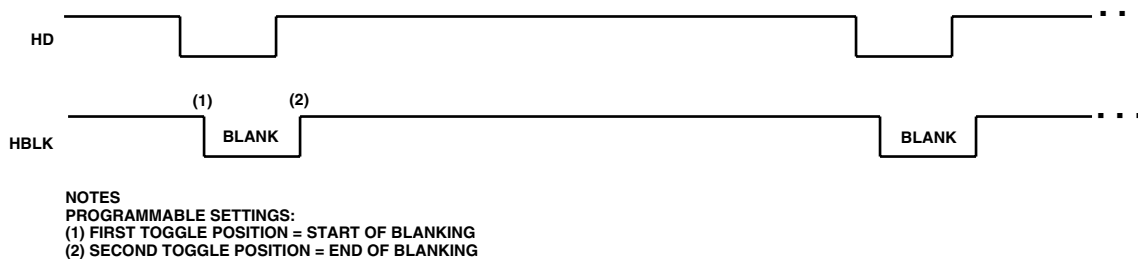


Figure 10. Horizontal Blanking (HBLK) Pulse Placement

Table IV. CLPOB, CLPDM, PBLK Individual Sequence Parameters

| Register Name | Length | Range | Description |
|---------------|--------|-----------------------|--|
| SPOL | 1b | High/Low | Starting Polarity of Clamp and Blanking Pulses for Sequences 0–3 |
| TOG1 | 12b | 0–4095 Pixel Location | First Toggle Position within the Line for Sequences 0–3 |
| TOG2 | 12b | 0–4095 Pixel Location | Second Toggle Position within the Line for Sequences 0–3 |

Table V. HBLK Individual Sequence Parameters

| Register Name | Length | Range | Description |
|---------------|--------|-----------------------|---|
| HBLKMASK | 1b | High/Low | Masking Polarity for H1 for Sequences 0–3 (0 = H1 Low, 1 = H1 High) |
| HBLKTOG1 | 12b | 0–4095 Pixel Location | First Toggle Position within the Line for Sequences 0–3 |
| HBLKTOG2 | 12b | 0–4095 Pixel Location | Second Toggle Position within the Line for Sequences 0–3 |

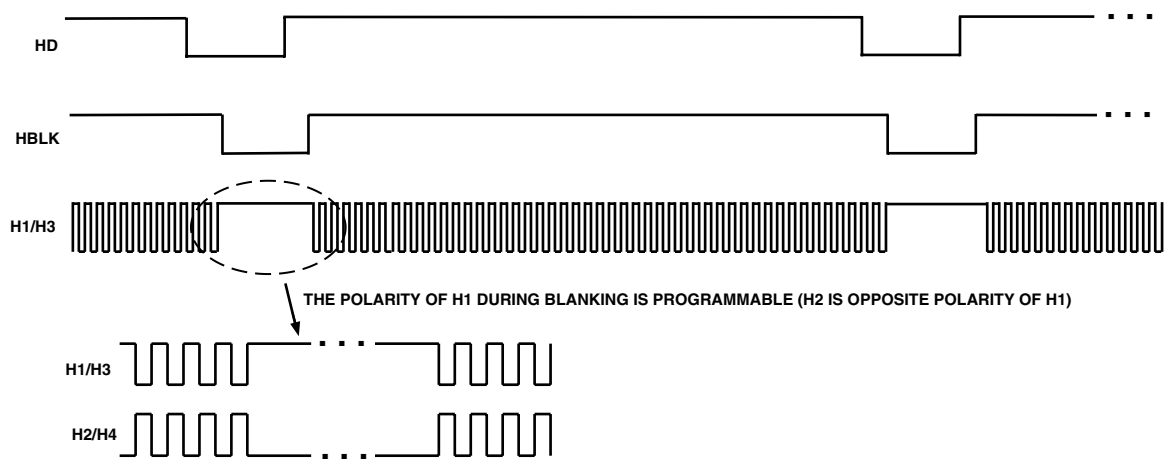


Figure 11. HBLK Masking Control

Horizontal Sequence Control

The AD9847 uses sequence change positions (SCP) and sequence pointers (SPTR) to organize the individual horizontal sequences. Up to four SCPs are available to divide the readout into four separate regions, as shown in Figure 12. The SCP 0 is always hard-coded to line 0, and SCP1–3 are register programmable. During each region bounded by the SCP, the SPTR registers designate which sequence is used by each signal. CLPOB, CLPDM,

PBLK, and HBLK each have a separate set of SCP. For example, CLPOBSCP1 will define Region 0 for CLPOB, and in that region any of the four individual CLPOB sequences may be selected with the CLPOBSPTR registers. The next SCP defines a new region, and in that region each signal can be assigned to a different individual sequence. The sequence control registers are summarized in Table VI.

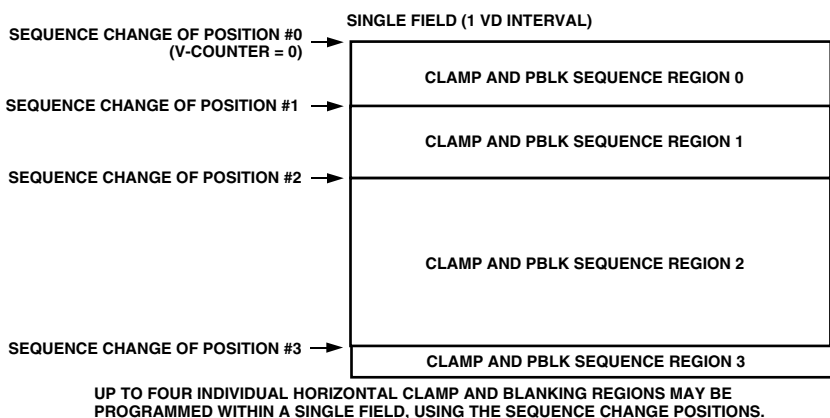


Figure 12. Clamp and Blanking Sequence Flexibility

Table VI. Horizontal Sequence Control Parameters for CLPOB, CLPDM, PBLK, and HBLK

| Register Name | Length | Range | Description |
|---------------|--------|---------------------|--|
| SCP1–SCP3 | 12b | 0–4095 Line Number | CLAMP/BLANK SCP to Define Horizontal Regions 0–3 |
| SPTR0–SPTR3 | 2b | 0–3 Sequence Number | Sequence Pointer for Horizontal Regions 0–3 |

AD9847

H-Counter Synchronization

The H-Counter reset occurs on the sixth CLI rising edge following the HD falling edge. The PxGA steering is synchronized with the reset of the internal H-Counter (see Figure 13).

POWER-UP PROCEDURE

Recommended Power-Up Sequence

When the AD9847 is powered up, the following sequence is recommended (refer to Figure 14 for each step).

1. Turn on power supplies for AD9847.
2. Apply the master clock input CLI, VD, and HD.
3. The Precision Timing core must be reset by writing a “0” to the TGCORE_RSTB Register (Address x026) followed by writing a “1” to the TGCORE_RSTB Register. This will start the internal timing core operation. Next, initialize the internal

4. circuitry by first writing “110101” or “53” decimal to the INITIAL1 Register (Address x020). Finally, write “000100” or “4” decimal to the INITIAL2 Register (Address x00F).
4. Write a “1” to the PREVENTUPDATE Register (Address x019). This will prevent the updating of the serial register data.
5. Write to the desired registers to configure high speed timing and horizontal timing.
6. Write a “1” to the OUT_CONT Register (Address x016). This will allow the outputs to become active after the next VD/HD rising edge.
7. Write a “0” to the PREVENTUPDATE Register (Address x019). This will allow the serial information to be updated at the next VD/HD falling edge.
8. The next VD/HD falling edge allows register updates to occur, including OUT_CONT, which enables all clock outputs.

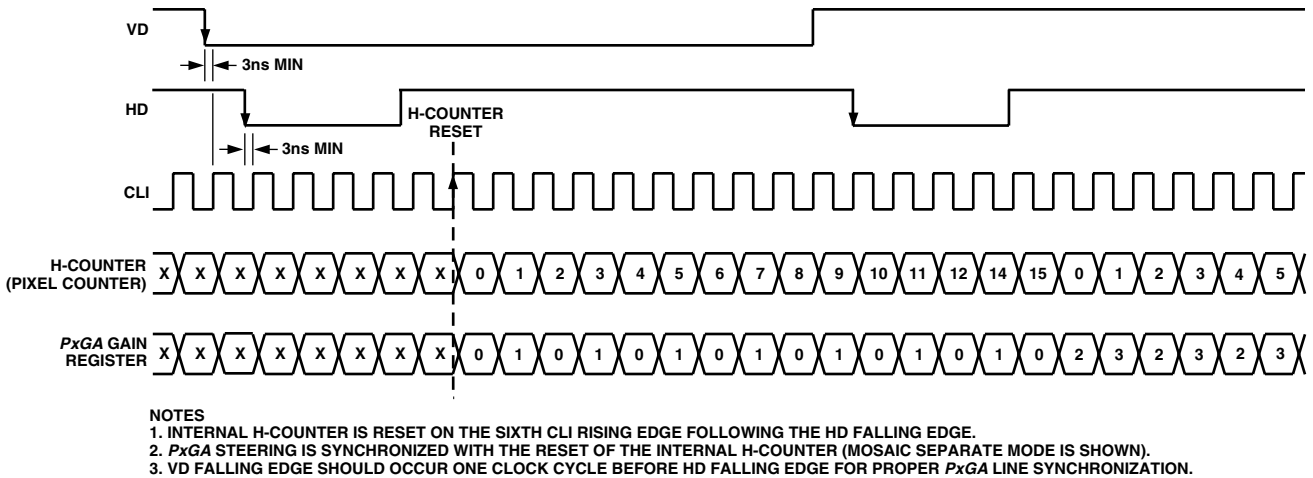


Figure 13. H-Counter Synchronization

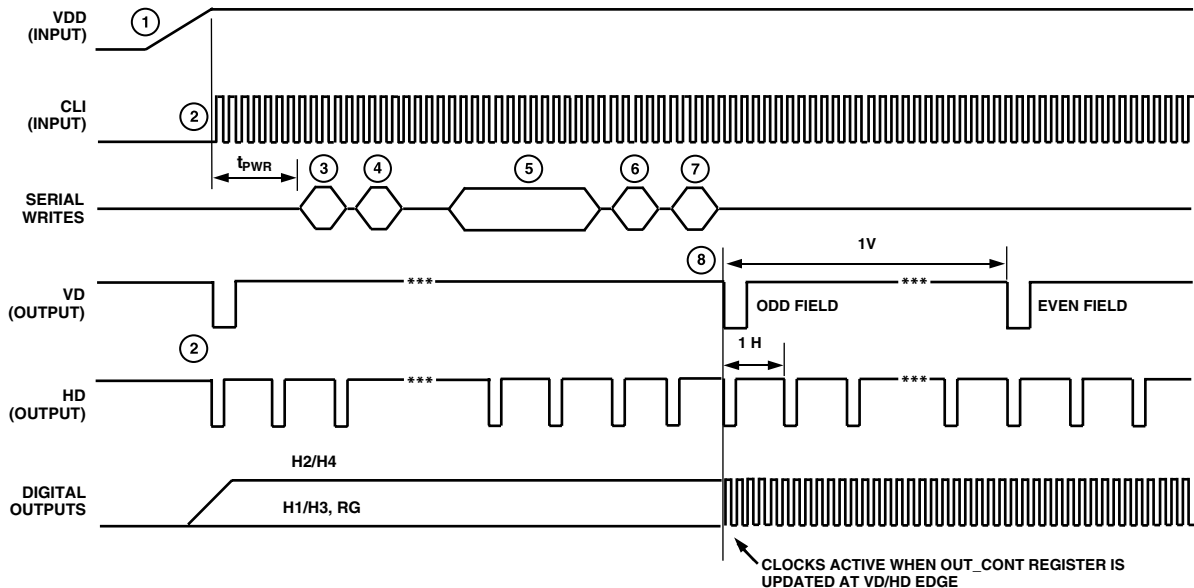


Figure 14. Recommended Power-Up Sequences

ANALOG FRONT END DESCRIPTION AND OPERATION

The AD9847 signal processing chain is shown in Figure 15. Each processing step is essential in achieving a high quality image from the raw CCD pixel data.

DC Restore

To reduce the large dc offset of the CCD output signal, a dc-restore circuit is used with an external $0.1\ \mu\text{F}$ series coupling capacitor. This restores the dc level of the CCD signal to approximately $1.5\ \text{V}$, to be compatible with the $3\ \text{V}$ analog supply of the AD9847.

Correlated Double Sampler

The CDS circuit samples each CCD pixel twice to extract the video information and reject low frequency noise. The timing shown in Figure 6 illustrates how the two internally generated CDS clocks, SHP and SHD, are used to sample the reference level and data level of the CCD signal, respectively. The placement of the SHP and SHD sampling edges is determined by the setting of the SHPOSLOC and SHDPOSLOC registers located at Addresses $0x\text{F0}$ and $0x\text{F1}$, respectively. Placement of these two clock signals is critical in achieving the best performance from the CCD.

Input Clamp

A line-rate input clamping circuit is used to remove the CCD's optical black offset. This offset exists in the CCD's shielded black reference pixels. The AD9847 removes this offset in the input stage to minimize the effect of a gain change on the system black level, usually called the "gain step."

Another advantage of removing this offset at the input stage is to maximize system headroom. Some area CCDs have large black level offset voltages, which, if not corrected at the input stage, can significantly reduce the available headroom in the internal circuitry when higher VGA gain settings are used.

Horizontal timing examples are shown on the last page of the Applications Information section. It is recommended that the CLPDM pulse be used during valid CCD dark pixels. CLPDM may be used during the optical black pixels, either together with CLPOB or separately. The CLPDM pulse should be a minimum of four pixels wide.

PxGA

The *PxGA* provides separate gain adjustment for the individual color pixels. A programmable gain amplifier with four separate values, the *PxGA* has the capability to "multiplex" its gain value on a pixel-to-pixel basis (see Figure 17). This allows lower output color pixels to be gained up to match higher output color pixels. Also, the *PxGA* may be used to adjust the colors for white balance, reducing the amount of digital processing that is needed. The four different gain values are switched according to the Color Steering circuitry. Seven different color steering modes for different types of CCD color filter arrays are programmed in the AD9847 AFE Register, *ctlmode*, at Address $0x06$ (see Figures 16a to 16g for timing examples). For example, Mosaic Separate steering mode accommodates the popular "Bayer" arrangement of red, green, and blue filters (see Figure 18).

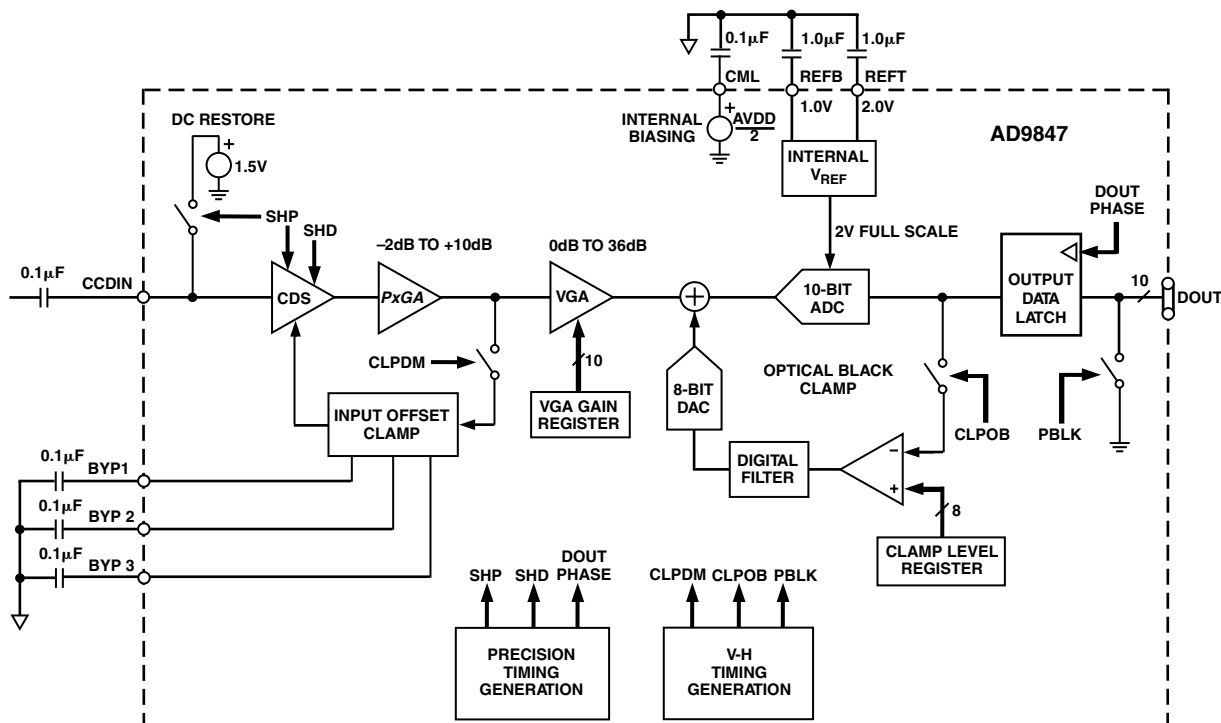
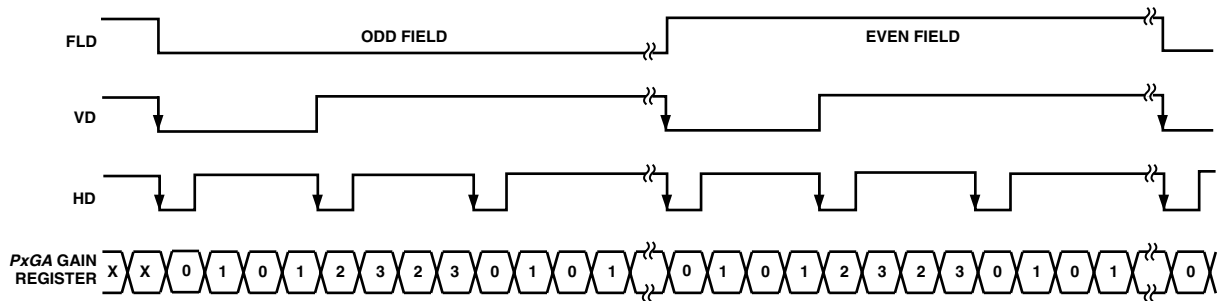
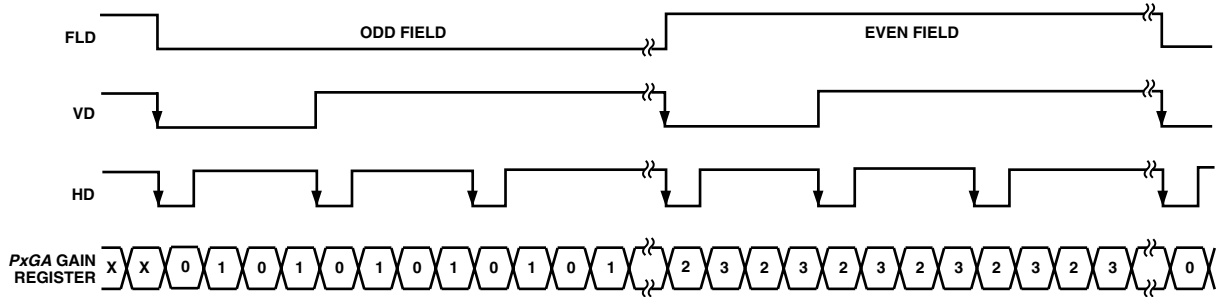


Figure 15. Analog Front End Block Diagram



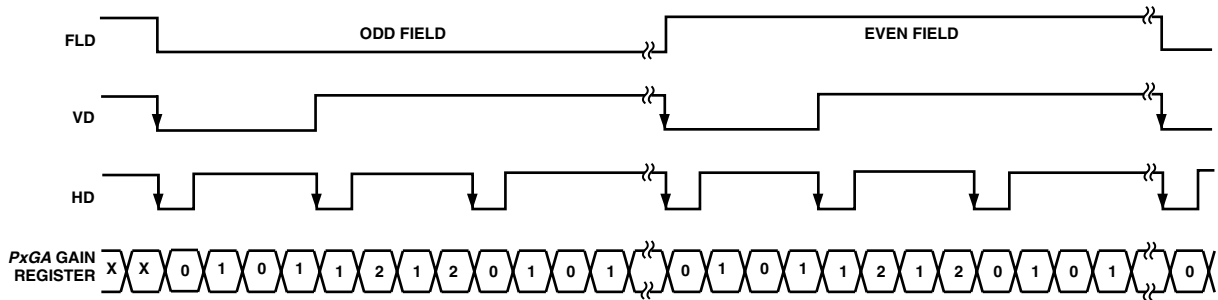
- NOTES
1. VD FALLING EDGE WILL RESET THE PxGA GAIN REGISTER STEERING TO "0101" LINE.
 2. HD FALLING EDGES WILL ALTERNATE THE PxGA GAIN REGISTER STEERING BETWEEN "0101" AND "2323" LINES.
 3. FLD STATUS IS IGNORED.

Figure 16a. Mosaic Separate Mode



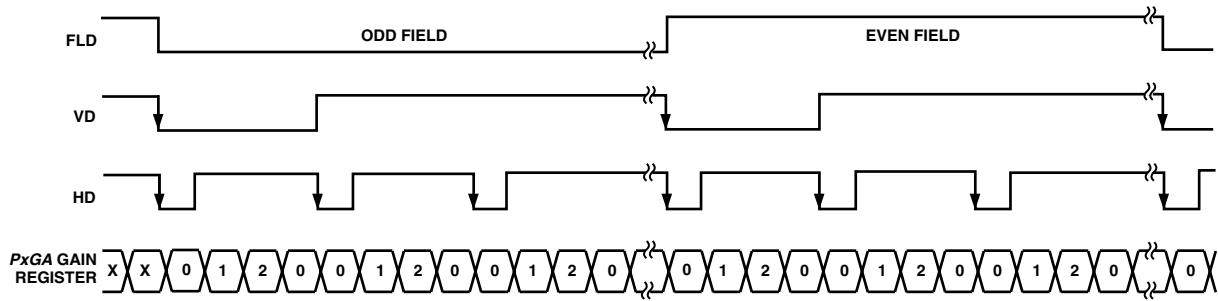
- NOTES
1. FLD RISING EDGE (START OF ODD FIELD) WILL RESET THE PxGA GAIN REGISTER STEERING TO "0101" LINE.
 2. FLD FALLING EDGE (START OF EVEN FIELD) WILL RESET THE PxGA GAIN REGISTER STEERING TO "2323" LINE.
 3. HD FALLING EDGES WILL RESET THE PxGA GAIN REGISTER STEERING TO EITHER "0" (FLD = ODD) OR "2" (FLD = EVEN).

Figure 16b. Mosaic Interlaced Mode



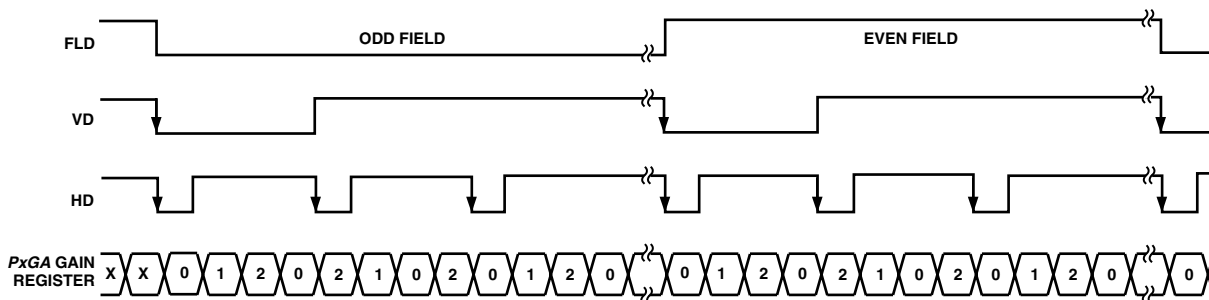
- NOTES
1. VD FALLING EDGE WILL RESET THE PxGA GAIN REGISTER STEERING TO "0101" LINE.
 2. HD FALLING EDGES WILL ALTERNATE THE PxGA GAIN REGISTER STEERING BETWEEN "0101" AND "1212" LINES.
 3. ALL FIELDS WILL HAVE THE SAME PxGA GAIN STEERING PATTERN (FLD STATUS IS IGNORED).

Figure 16c. Mosaic Repeat Mode



- NOTES
1. EACH LINE FOLLOWS "012012" STEERING PATTERN.
 2. VD AND HD FALLING EDGES WILL RESET THE PxGA GAIN REGISTER STEERING TO "0."
 3. FLD STATUS IS IGNORED.

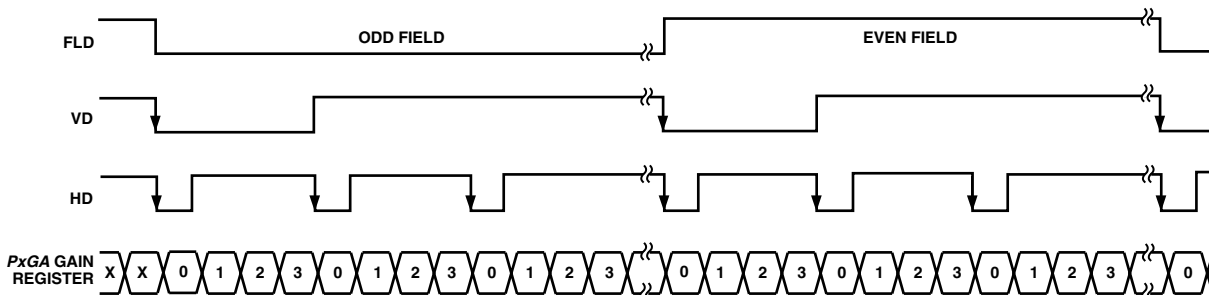
Figure 16d. Three-Color Mode



NOTES

1. VD FALLING EDGE WILL RESET THE PxGA GAIN REGISTER STEERING TO "012012" LINE.
2. HD FALLING EDGES WILL ALTERNATE THE PxGA GAIN REGISTER, STEERING BETWEEN "012012" AND "210210" LINES.
3. FLD STATUS IS IGNORED.

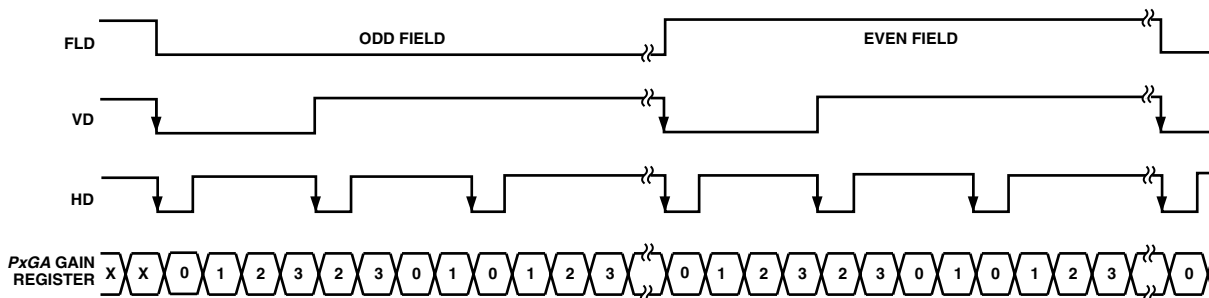
Figure 16e. Three-Color Mode II



NOTES

1. EACH LINE FOLLOWS "01230123" STEERING PATTERN.
2. VD AND HD FALLING EDGES WILL RESET THE PxGA GAIN REGISTER STEERING TO GAIN REGISTER "0."
3. FLD STATUS IS IGNORED.

Figure 16f. Four-Color Mode



NOTES

1. VD FALLING EDGE WILL RESET THE PxGA GAIN REGISTER STEERING TO "01230123" LINE.
2. HD FALLING EDGES WILL ALTERNATE THE PxGA GAIN REGISTER STEERING BETWEEN "01230123" AND "23012301" LINES.
3. FLD STATUS IS IGNORED.

Figure 16g. Four-Color Mode II

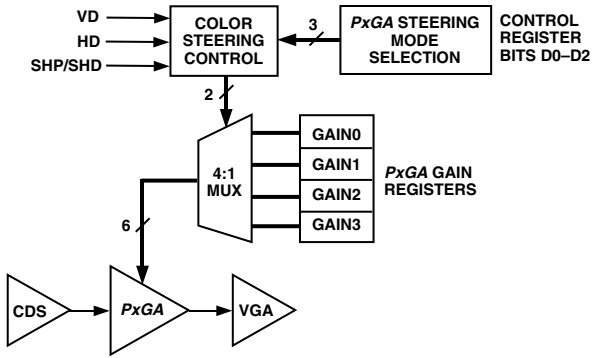


Figure 17. PxGA Block Diagram

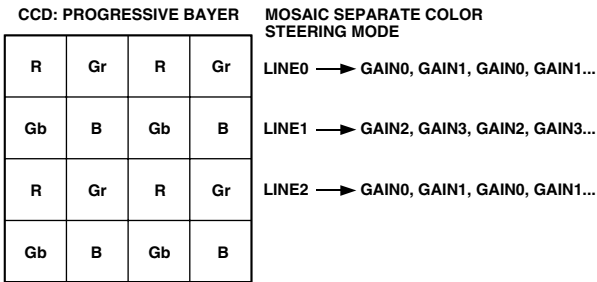


Figure 18a. CCD Color Filter Example: Progressive Scan

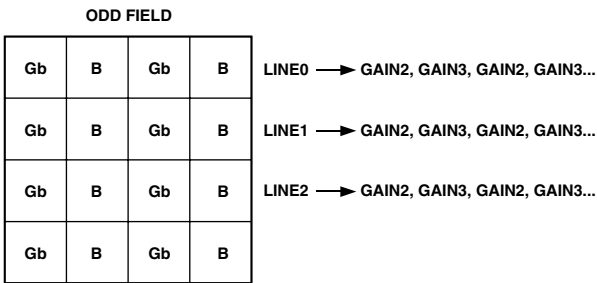
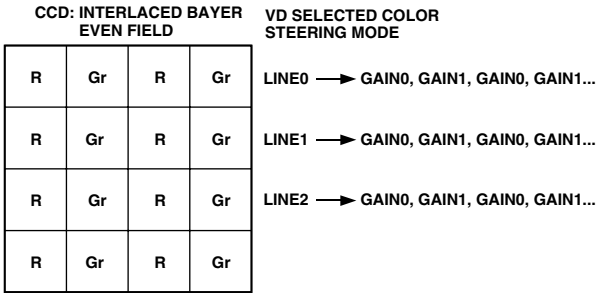


Figure 18b. CCD Color Filter Example: Interlaced

The Bayer pattern can also be interlaced, and the VD selected mode should be used with this type of CCD (see Figure 18b). The color steering performs the proper multiplexing of the R, G, and B gain values (loaded into the PxGA gain registers) and is synchronized by the user with vertical (VD) and horizontal (HD) sync pulses. For more detailed information, see the PxGA Timing section. The PxGA gain for each of the four channels varies from -2 dB to +10 dB, controlled in 64 steps through the serial interface. The PxGA gain curve is shown in Figure 19.

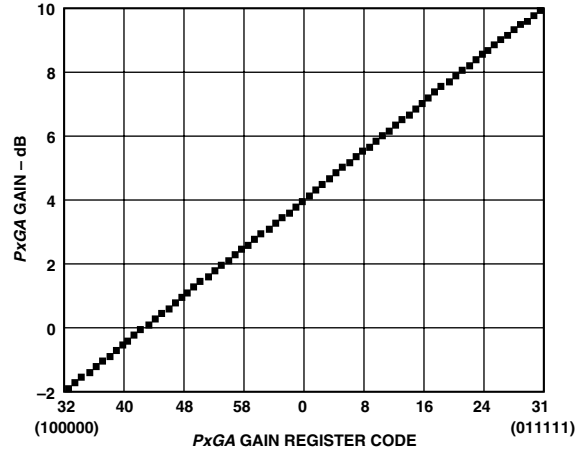


Figure 19. PxGA Gain Curve

Variable Gain Amplifier

The VGA stage provides a gain range of 2 dB to 36 dB, programmable with 10-bit resolution through the serial digital interface. Combined with 4 dB from the PxGA stage, the total gain range for the AD9847 is 6 dB to 40 dB. The minimum gain of 6 dB is needed to match a 1 V input signal with the ADC full-scale range of 2 V. When compared to 1 V full-scale systems (such as ADI's AD9803), the equivalent gain range is 0 dB to 34 dB.

The VGA gain curve is divided into two separate regions. When the VGA gain register code is between 0 and 511, the curve follows a $(1 + x)/(1 - x)$ shape, which is similar to a linear-in-dB characteristic. From code 512 to code 1023, the curve follows a linear-in-dB shape. The exact VGA gain can be calculated for any gain register value by using the following two equations:

| Code Range | Gain Equation (dB) |
|------------|--|
| 0-511 | $Gain = 20 \log_{10} \left(\frac{[658 + code]}{[658 - code]} \right) - 0.4$ |
| 512-1023 | $Gain = (0.0354)(code) - 0.04$ |

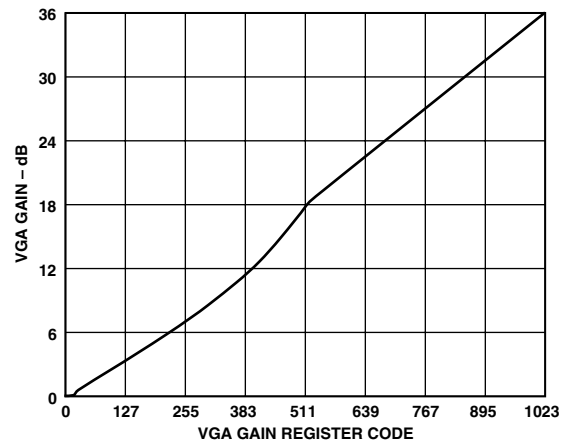


Figure 20. VGA Gain Curve (Gain from PxGA Not Included)

AD9847

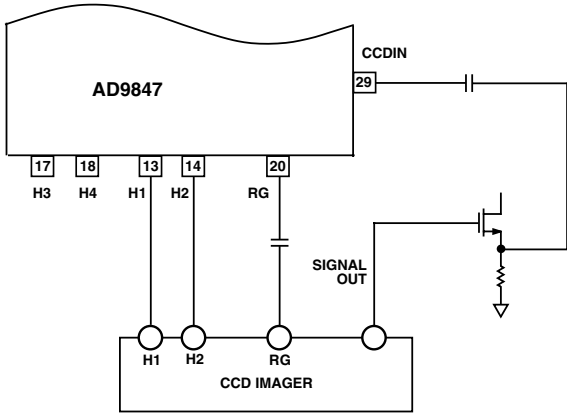


Figure 22a. CCD Connections (2 H-Clock)

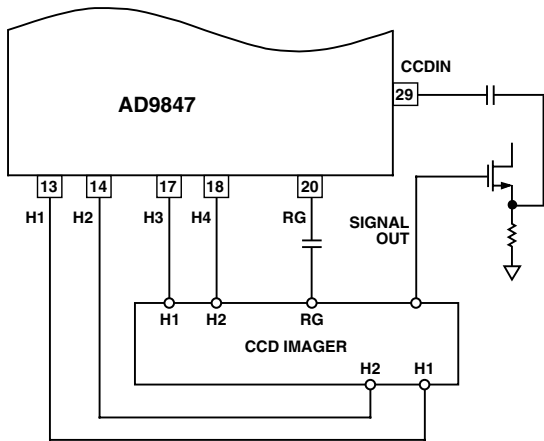


Figure 22b. CCD Connections (4 H-Clock)

Driving the CLI Input

The AD9847's master clock input (CLI) may be used in two different configurations, depending on the application. Figure 23a shows a typical dc-coupled input from the master clock source. When the dc-coupled technique is used, the master clock signal should be at standard 3 V CMOS logic levels. As shown in Figure 23b, a 1000 pF ac-coupling capacitor may be used between the clock source and the CLI input. In this configuration, the CLI input will self-bias to the proper dc voltage level of approximately 1.4 V. When the ac-coupled technique is used, the master clock signal can be as low as ± 500 mV in amplitude.

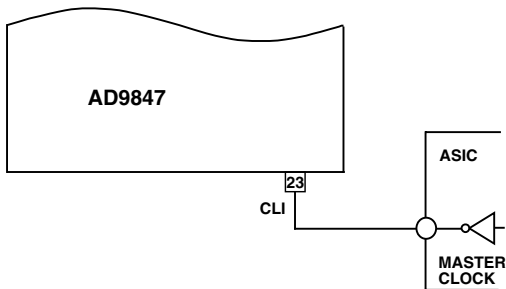


Figure 23a. CLI Connection, DC-Coupled

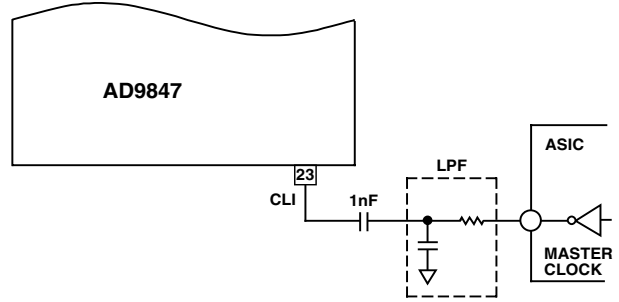


Figure 23b. CLI Connection, AC-Coupled

Internal Mode Circuit Configuration

The AD9847 may be used in internal mode using the circuit configuration of Figure 24. Internal mode uses the same circuit as Figure 21, except that the horizontal pulses (CLPOB, CLPDM, PBLK, and HBLK) are internally generated in the AD9847. These pins may be grounded when internal mode is used. Only the HD and VD signals are required from the ASIC.

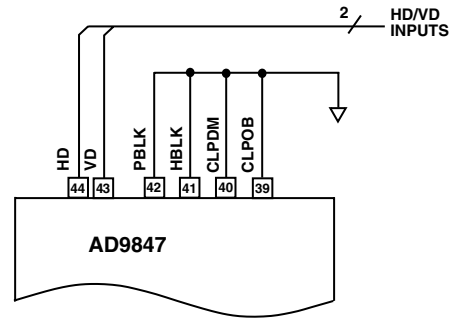


Figure 24. Internal Mode Circuit Configuration

TIMING EXAMPLES FOR DIFFERENT SEQUENCES

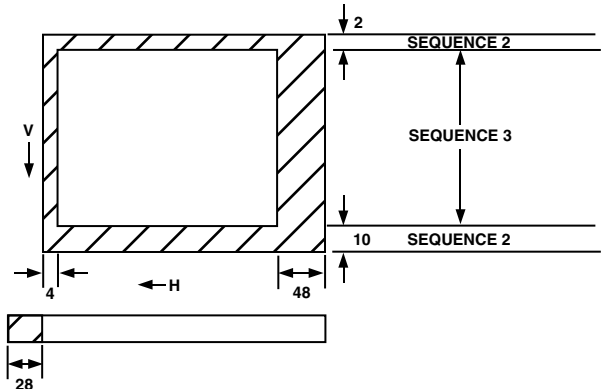


Figure 25. Typical CCD

Timing Examples (continued)

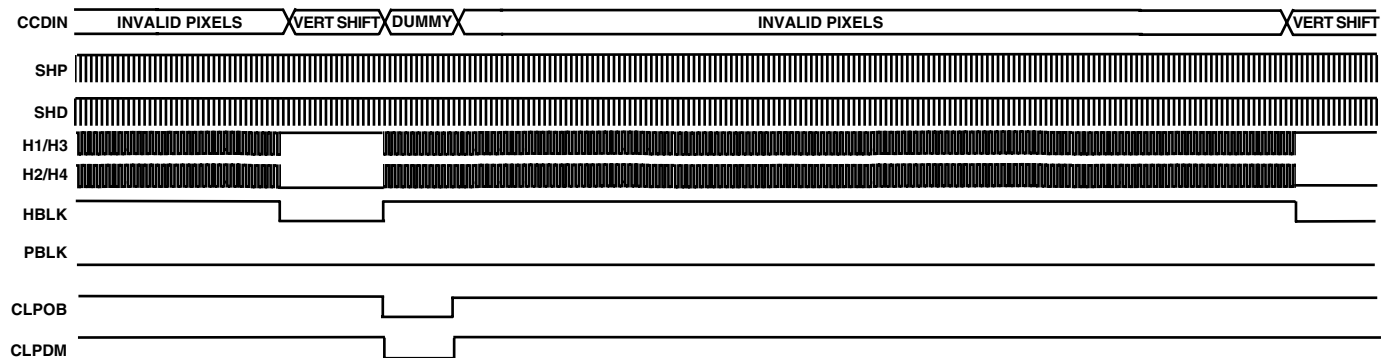


Figure 26. Sequence 1: Vertical Blanking

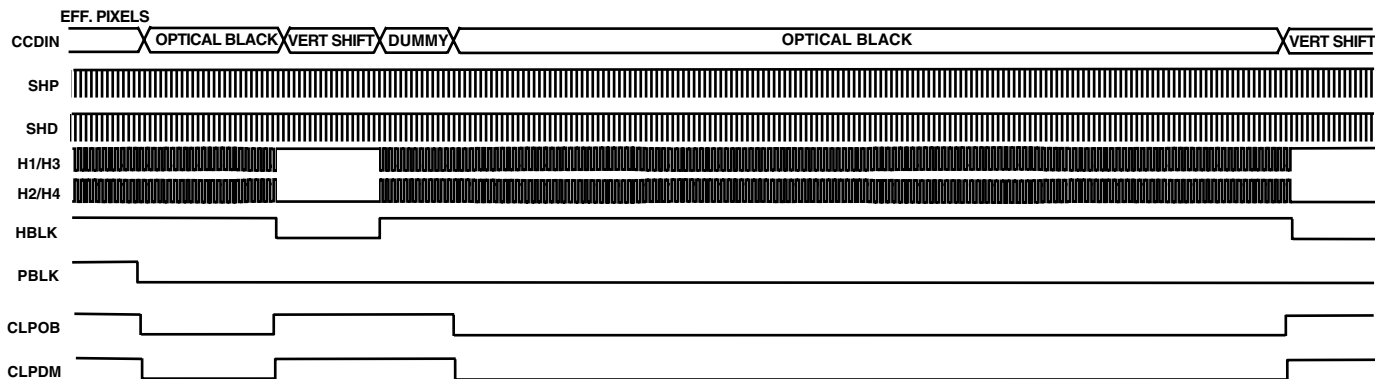


Figure 27. Sequence 2: Vertical Optical Black

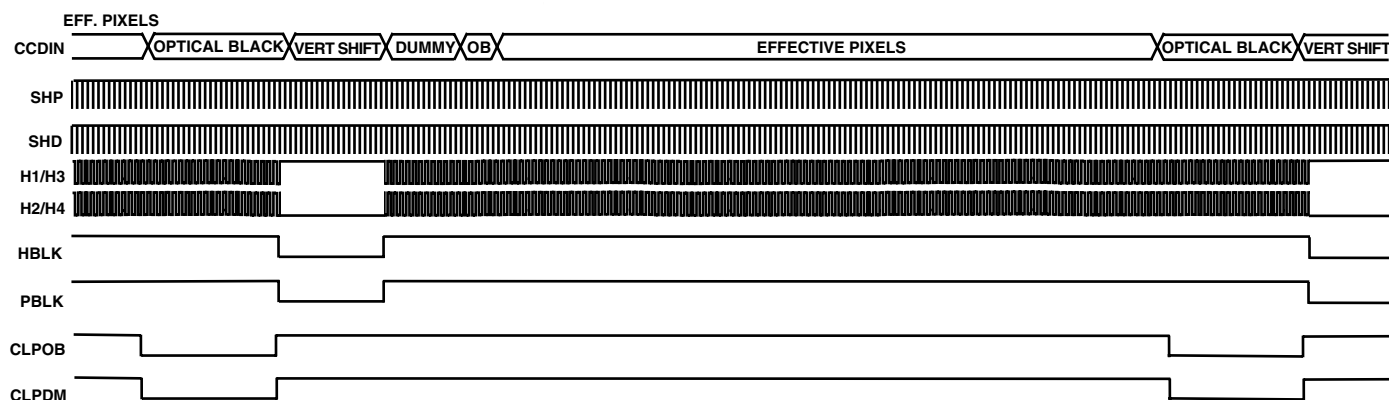
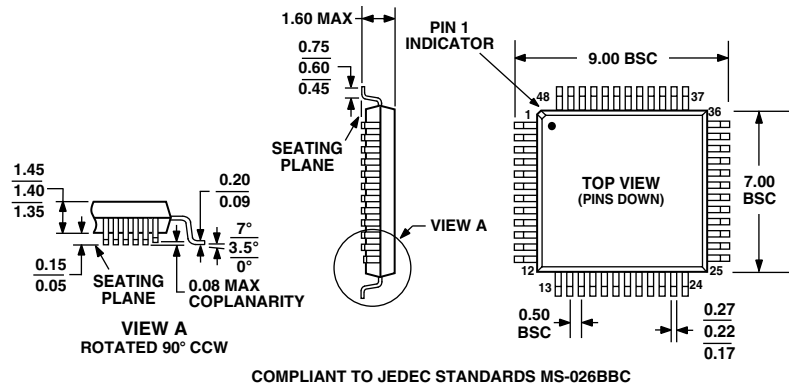


Figure 28. Sequence 3: Effective Pixels

OUTLINE DIMENSIONS

48-Lead Plastic Quad Flatpack [LQFP]
1.4 mm Thick
(ST-48)

Dimensions shown in millimeters



Revision History

| Location | Page |
|--|------|
| 1/03—Data Sheet changed from REV. 0 to REV. A. | |
| Change to PIN FUNCTION DESCRIPTIONS | 6 |
| Change to Register Description Table – HBLK # Bits 147 | 13 |
| Changes to Recommended Power Sequence section | 20 |
| Updated OUTLINE DIMENSIONS | 28 |



LittleDiode supplies new, hard to find or obsolete electronic components and semiconductors all over the world.

With over two million different components listed you are sure to find the part you need.

Feel free to visit us today at our online store:

LittleDiode.com

Looking forward to providing you with the best possible service.