National Semiconductor

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ADC1205/ADC1225 12-Bit Plus Sign μP Compatible A/D Converters

General Description

The ADC1205 and ADC1225 are CMOS, 12-bit plus sign successive approximation A/D converters. The 24-pin ADC1205 outputs the 13-bit data result in two 8-bit bytes, formatted high-byte first with sign extended. The 28-pin ADC1225 outputs a 13-bit word in parallel for direct interface to a 16-bit data bus.

Negative numbers are represented in 2's complement data format. All digital signals are fully TTL and MOS compatible.

A unipolar input (0V to 5V) can be accommodated with a single 5V supply, while a bipolar input (−5V to +5V) requires the addition of a 5V negative supply.

The ADC1205C and ADC1225C have a maximum non-linearity of 0.0224% of Full Scale.

Key Specifications

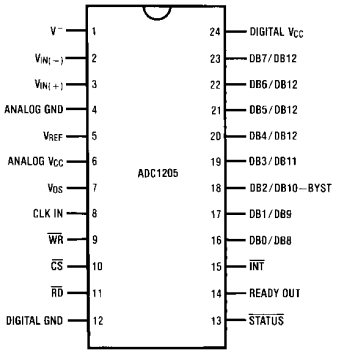
- Resolution—12 bits plus sign
- Linearity Error—±1 LSB
- Conversion Time—100 μs

Features

- Compatible with all μPs
- True differential analog voltage inputs
- 0V to 5V analog voltage range with single 5V supply
- TTL/MOS input/output compatible
- Low power—25 mW max
- Standard 24-pin or 28-pin DIP

Connection and Functional Diagrams

Dual-In-Line Package



Top View

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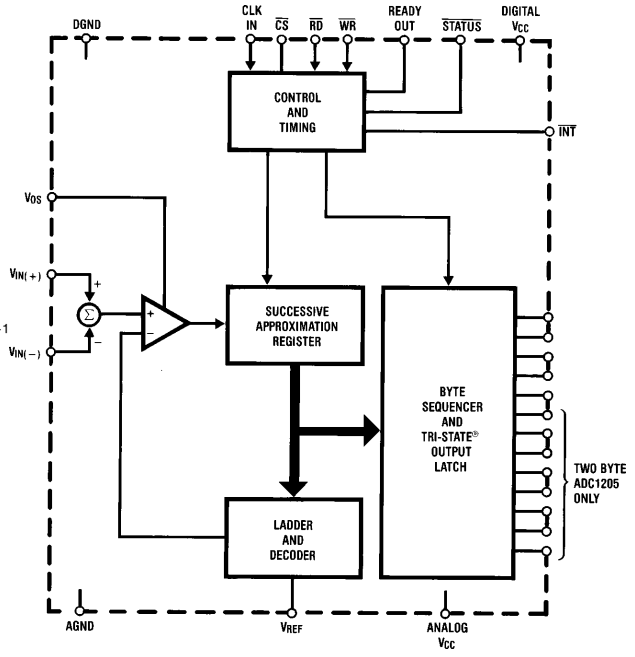

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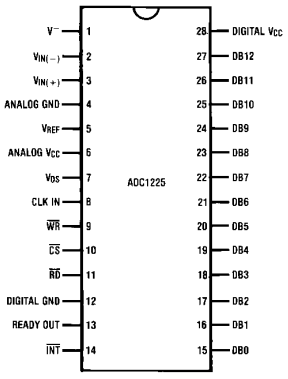
Dual-In-Line Package



Top View

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See Ordering Information

TRI-STATE® is a registered trademark of National Semiconductor Corporation.

Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (DV_{CC} and AV_{CC})	6.5V
Negative Supply Voltage (V^-)	−15V to GND
Logic Control Inputs	−0.3V to +15V
Voltage at Analog Inputs $[V_{IN(+)}, V_{IN(-)}]$	$(V^-)-0.3V$ to $V_{CC}+0.3V$
Voltage at All Outputs, V_{REF}, V_{OS}	−0.3V to $(V_{CC}+0.3)V$
Input Current per Pin	±5mA
Input Current per Package	±20mA
Storage Temperature Range	−65°C to +150°C
Package Dissipation at $T_A = 25°C$	875 mW
Lead Temp. (Soldering, 10 seconds)	300°C
ESD Susceptibility (Note 12)	800V

Operating Conditions (Notes 1 & 2)

Temperature Range	$T_{MIN} \le T_A \le T_{MAX}$
ADC1205CCJ, ADC1225CCD	$-40°C \le T_A \le +85°C$
ADC1205CCJ-1, ADC1225CCD-1	$0°C \le T_A \le 70°C$
Supply Voltage (DV_{CC} and AV_{CC})	4.5 V_{DC} to 6.0 V_{DC}
Negative Supply Voltage (V^-)	−15V to GND

Electrical Characteristics

The following specifications apply for $DV_{CC} = AV_{CC} = 5V$, $V_{REF} = 5V$, $f_{CLK} = 1.0$ MHz, $V^- = -5V$ for bipolar input range, or $V^- =$ GND for unipolar input range unless otherwise specified. Bipolar input range is defined as $-5.05V \le V_{IN(+)} \le 5.05V$; $-5.05V \le V_{IN(-)} \le 5.05V$ and $|V_{IN(+)} - V_{IN(-)}| \le 5.05V$. Unipolar input range is defined as $-0.05V \le V_{IN(+)} \le 5.05V$; $-0.05V \le V_{IN(-)} \le 5.05V$ and $|V_{IN(+)} - V_{IN(-)}| \le 5.05V$. **Boldface limits apply from T_{MIN} to T_{MAX};** all other limits $T_A = T_J = 25°C$ (Notes 3, 4, 5, 6, 7).

Parameter	Conditions	ADC1205CCJ, ADC1225CCD			ADC1205CCJ-1, ADC1225CCD-1			Limit Units
		Typ (Note 8)	Tested Limit (Note 9)	Design Limit (Note 10)	Typ (Note 8)	Tested Limit (Note 9)	Design Limit (Note 10)	
CONVERTER CHARACTERISTICS								
Linearity Error ADC1205CCJ, ADC1225CCD ADC1205CCJ-1, ADC1225CCD-1	Unipolar Input Range (Note 11)		**±1**			 ±1	 **±1**	 LSB LSB
Unadjusted Zero Error	Unipolar Input Range		**±2**			±2	**±2**	LSB
Unadjusted Positive and Negative Full-Scale Error	Unipolar Input Range		**±30**			±30	**±30**	LSB
Negative Full-Scale Error	Unipolar Input Range, Full Scale Adj. to Zero			**±½**			**±½**	LSB
Linearity Error ADC1205CCJ, ADC1225CCD ADC1205CCJ-1, ADC1225CCD-1	Bipolar Input Range (Note 11)		**±2**			 ±2	 **±2**	 LSB LSB
Unadjusted Zero Error	Bipolar Input Range		**±2**			±2	**±2**	LSB
Unadjusted Positive and Negative Full-Scale Error	Bipolar Input Range		**±30**			±30	**±30**	LSB
Negative Full-Scale Error	Bipolar Input Range, Full Scale Adj. to Zero		**±2**			±2	**±2**	LSB
Maximum Gain Temperature Coefficient		6		**15**	6		**15**	ppm/°C
Maximum Offset Temperature Coefficient		0.5		**1.5**	0.5		**1.5**	ppm/°C
Minimum V_{REF} Input Resistance		4.0	**2**		4.0	2	**2**	kΩ
Maximum V_{REF} Input Resistance		4.0	**8**		4.0	8	**8**	kΩ

Electrical Characteristics (Continued)

The following specifications apply for $DV_{CC} = AV_{CC} = 5V$, $V_{REF} = 5V$, $f_{CLK} = 1.0$ MHz, $V^- = -5V$ for bipolar input range, or $V^- =$ GND for unipolar input range unless otherwise specified. Bipolar input range is defined as $-5.05V \le V_{IN(+)} \le 5.05V$; $-5.05V \le V_{IN(-)} \le 5.05V$ and $|V_{IN(+)} - V_{IN(-)}| \le 5.05V$. Unipolar input range is defined as $-0.05V \le V_{IN(+)} \le 5.05V$; $-0.05V \le V_{IN(-)} \le 5.05V$ and $|V_{IN(+)} - V_{IN(-)}| \le 5.05V$. **Boldface limits apply from T_{MIN} to T_{MAX};** all other limits $T_A = T_J = 25°C$ (Notes 3, 4, 5, 6, 7).

Parameter	Conditions	ADC1205CCJ, ADC1225CCD			ADC1205CCJ-1, ADC1225CCD-1			Limit Units
		Typ (Note 8)	Tested Limit (Note 9)	Design Limit (Note 10)	Typ (Note 8)	Tested Limit (Note 9)	Design Limit (Note 10)	
CONVERTER CHARACTERISTICS (Continued)								
Minimum Analog Input Voltage	Unipolar Input Range		**GND-0.05**			GND-0.05	**GND-0.05**	V
	Bipolar Input Range		**$-V_{CC}-0.05$**			$-V_C-0.05$	**$-V_{CC}-0.05$**	V
Maximum Analog Input Voltage	Unipolar Input Range		**$V_{CC}+0.05$**			$V_{CC}+0.05$	**$V_{CC}+0.05$**	V
	Bipolar Input Range	**$V_{CC}+0.05$**				$V_{CC}+0.05$	**$V_{CC}+0.05$**	V
DC Common-Mode Error		±1/8	±1/2		±1/8	±1/2	±1/2	LSB
Power Supply Sensitivity	$AV_{CC}=DV_{CC}=5V\pm5\%$, $V^-=-5V\pm5\%$							
Zero Error			±3/4			±3/4	±3/4	LSB
Positive and Negative Full-Scale Error			±3/4			±3/4	±3/4	LSB
Linearity Error			±1/4			±1/4	±1/4	LSB
DIGITAL AND DC CHARACTERISTICS								
$V_{IN(1)}$, Logical "1" Input Voltage (Min)	$V_{CC}=5.25V$, All Inputs except CLK IN		**2.0**			2.0	**2.0**	V
$V_{IN(0)}$, Logical "0" Input Voltage (Max)	$V_{CC}=4.75V$, All Inputs except CLK IN		**0.8**			0.8	**0.8**	V
$I_{IN(1)}$, Logical "1" Input Current (Max)	$V_{IN}=5V$	0.005	**1**		0.005		**1**	**μA**
$I_{IN(0)}$, Logical "0" Input Current (Max)	$V_{IN}=0V$	−0.005	**−1**		−0.005		**−1**	**μA**
V_T^+ (Min), Minimum Positive-Going Threshold Voltage	CLK IN	3.1	**2.7**		3.1	2.7	**2.7**	V
V_T^+ (Max), Maximum Positive-Going Threshold Voltage	CLK IN	3.1	**3.5**		3.1	3.5	**3.5**	V
V_T^- (Min), Minimum Negative-Going Threshold Voltage	CLK IN	1.8	**1.4**		1.8	1.4	**1.4**	V
V_T^- (Max), Maximum Negative-Going Threshold Voltage	CLK IN	1.8	**2.1**		1.8	2.1	**2.1**	V
V_H(Min), Minimum Hysteresis $[V_T^+(Min)-V_T^-(Max)]$	CLK IN	1.3	**0.6**		1.3	0.6	**0.6**	V
V_H(Max), Maximum Hysteresis $[V_T^+(Max)-V_T^-(Min)]$	CLK IN	1.3	**2.1**		1.3	2.1	**2.1**	V

Electrical Characteristics (Continued)

The following specifications apply for $DV_{CC} = AV_{CC} = 5V$, $V_{REF} = 5V$, $f_{CLK} = 1.0$ MHz, $V^- = -5V$ for bipolar input range, or $V^- =$ GND for unipolar input range unless otherwise specified. Bipolar input range is defined as $-5.05V \le V_{IN(+)} \le 5.05V$; $-5.05V \le V_{IN(-)} \le 5.05V$ and $|V_{IN(+)} - V_{IN(-)}| \le 5.05V$. Unipolar input range is defined as $-0.05V \le V_{IN(+)} \le 5.05V$; $-0.05V \le V_{IN(-)} \le 5.05V$ and $|V_{IN(+)} - V_{IN(-)}| \le 5.05V$. **Boldface limits apply from T_{MIN} to T_{MAX};** all other limits $T_A = T_J = 25°C$ (Notes 3, 4, 5, 6, 7).

Parameter	Conditions	ADC1205CCJ, ADC1225CCD			ADC1205CCJ-1, ADC1225CCD-1			Limit Units
		Typ (Note 8)	Tested Limit (Note 9)	Design Limit (Note 10)	Typ (Note 8)	Tested Limit (Note 9)	Design Limit (Note 10)	
DIGITAL AND DC CHARACTERISTICS (Continued)								
$V_{OUT(1)}$, Logical "1" Output Voltage (Min)	$V_{CC} = 4.75V$ $I_{OUT} = -360\ \mu A$ $I_{OUT} = -10\ \mu A$		**2.4** **4.5**			2.4 4.5	**2.4** **4.5**	V V
$V_{OUT(0)}$, Logical "0" Output Voltage (Max)	$V_{CC} = 4.75V$ $I_{OUT} = 1.6$ mA		**0.4**			0.4	**0.4**	V
I_{OUT}, TRI-STATE Output Leakage Current (Max)	$V_{OUT} = 0V$ $V_{OUT} = 5V$	−0.01 0.01	**−3** **3**		−0.01 0.01	−0.3 0.3	**−3** **3**	μA μA
I_{SOURCE}, Output Source Current (Min)	$V_{OUT} = 0V$	−12	**−6.0**		−12	−7.0	**−6.0**	mA
I_{SINK}, Output Sink Current (Min)	$V_{OUT} = 5V$	16	**8.0**		16	9.0	**8.0**	mA
DI_{CC}, DV_{CC} Supply Current (Max)	$f_{CLK} = 1$ MHz, $\overline{CS} = 1$	1	**3**		1	2.5	**3**	mA
AI_{CC}, AV_{CC} Supply Current (Max)	$f_{CLK} = 1$ MHz, $\overline{CS} = 1$	1	**3**		1	2.5	**3**	mA
I^-, V^- Supply Current (Max)	$f_{CLK} = 1$ MHz, $\overline{CS} = 1$	10	**100**		10	100	**100**	μA

AC Electrical Characteristics

The following specifications apply for $DV_{CC} = AV_{CC} = 5.0V$, $t_r = t_f = 20$ ns and $T_A = 25°C$ unless otherwise specified.

Parameter		Conditions	Typ (Note 8)	Tested Limit (Note 9)	Design Limit (Note 10)	Limit Units
f_{CLK}, Clock Frequency	MIN MAX		1.0 1.0	0.3 1.5		MHz MHz
Clock Duty Cycle	MIN MAX				40 60	% %
T_C, Conversion Time	MIN MAX MIN MAX	 $f_{CLK} = 1.0$ MHz $f_{CLK} = 1.0$ MHz			108 109 108 109	$1/f_{CLK}$ $1/f_{CLK}$ μs μs
$t_{W(\overline{WR})L}$, $\overline{WR}$ Pulse Width	MAX		220		350	ns
t_{ACC}, Access Time (Delay from Falling Edge of $\overline{RD}$ to Output Data Valid) (Max)		$C_L = 100$ pF	210		340	ns
t_{1H}, t_{0H}, TRI-STATE Control (Delay from Rising Edge of $\overline{RD}$ to Hi-Z State) (Max)		$R_L = 2k$, $C_L = 100$ pF	170		290	ns
$t_{PD(READYOUT)}$, $\overline{RD}$ or $\overline{WR}$ to READYOUT Delay (Max)			250		400	ns
$t_{PD(INT)}$, $\overline{RD}$ or $\overline{WR}$ to Reset of $\overline{INT}$ (Max)			250		400	ns

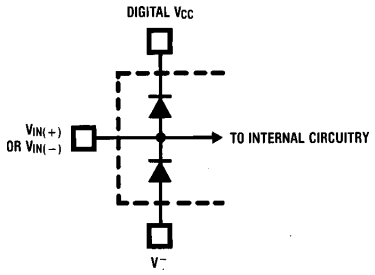
Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its specified operating ratings.

Note 2: All voltages are measured with respect to ground, unless otherwise specified.

Note 3: A parasitic zener diode exists internally from AV_{CC} and DV_{CC} to ground. This parasitic zener has a typical breakdown voltage of 7 V_{DC}.

AC Electrical Characteristics (Continued)

Note 4: Two on-chip diodes are tied to each analog input as shown below.



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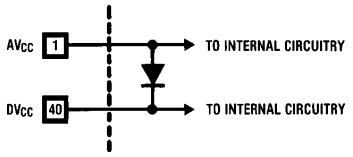
Errors in the A/D conversion can occur if these diodes are forward biased more than 50 mV. This means that if AV_{CC} and DV_{CC} are minimum (4.75 V_{DC}) and V^- is minimum ($-4.75V_{DC}$), full-scale must be $\leq 4.8V_{DC}$.

Note 5: A diode exists between analog V_{CC} and digital V_C.



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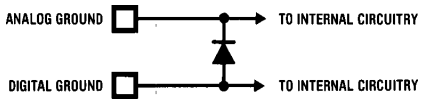
To guarantee accuracy, it is required that the AV_{CC} and DV_{CC} be connected together to a power supply with separate bypass filters at each V_{CC} pin.

Note 6: A diode exists between analog ground and digital ground.



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To guarantee accuracy, it is required that the analog ground and digital ground be connected together externally.

Note 7: Accuracy is guaranteed at $f_{CLK} = 1.0$ MHz. At higher clock frequencies accuracy may degrade.

Note 8: Typicals are at 25°C and represent most likely parametric norm.

Note 9: Tested and guaranteed to National's AOQL (Average Outgoing Quality Level).

Note 10: Guaranteed, but not 100% production tested. These limits are not used to calculate outgoing quality levels.

Note 11: Linearity error is defined as the deviation of the analog value, expressed in LSBs, from the straight line which passes through positive full scale and zero, after adjusting zero error. (See *Figures 1b* and *1c*).

Note 12: Human body model; 100 pF discharged through a 1.5 kΩ resistor.

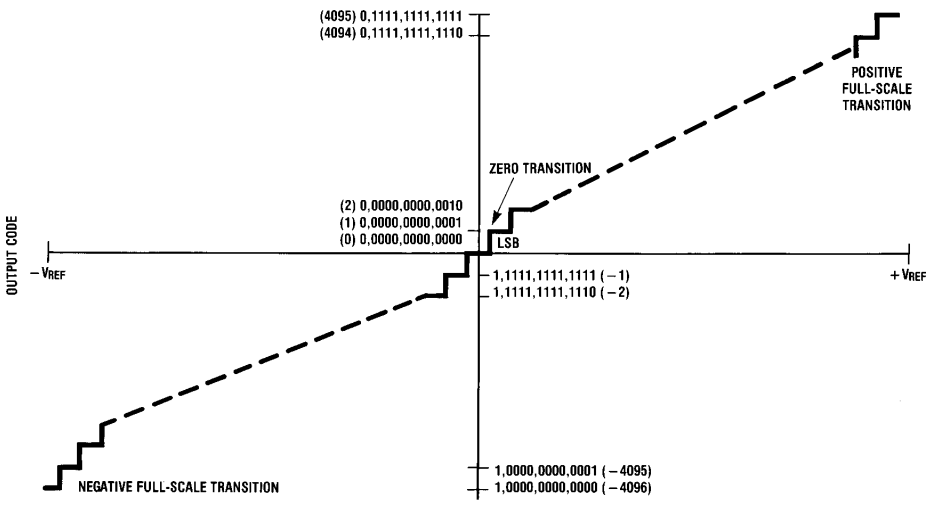

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FIGURE 1a. Transfer Characteristic

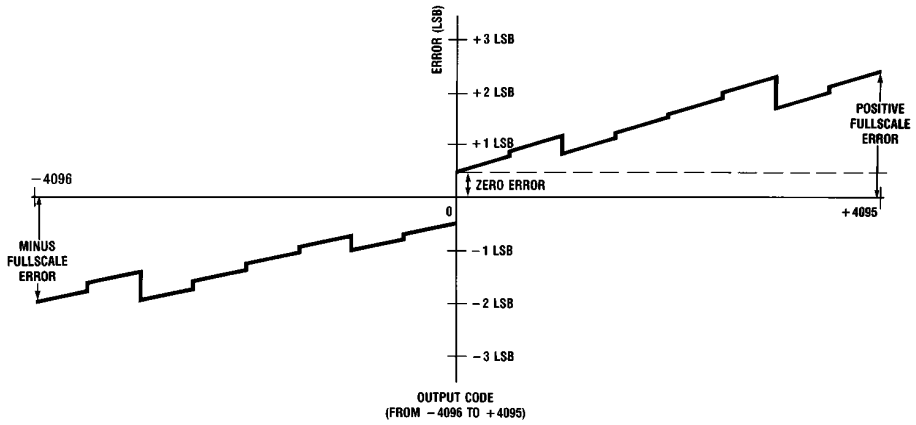

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FIGURE 1b. Simplified Error Curve vs. Output Code Without Zero and Fullscale Adjustment

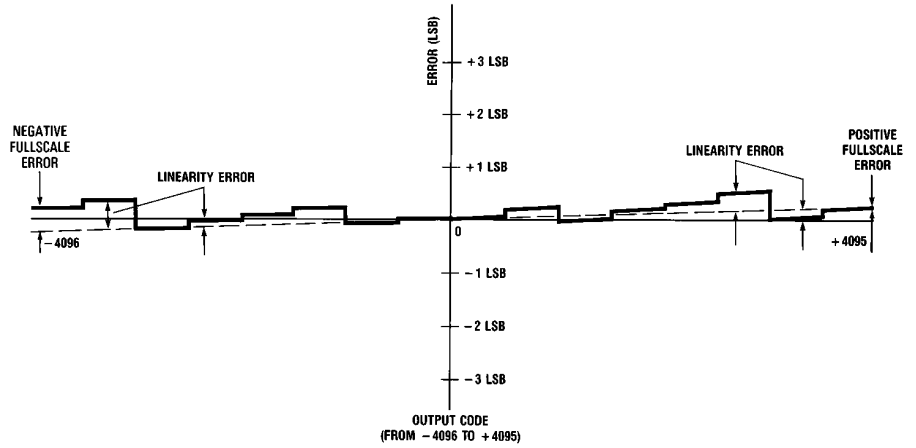

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FIGURE 1c. Simplified Error Curve vs. Output Code after Zero/Fullscale Adjustment

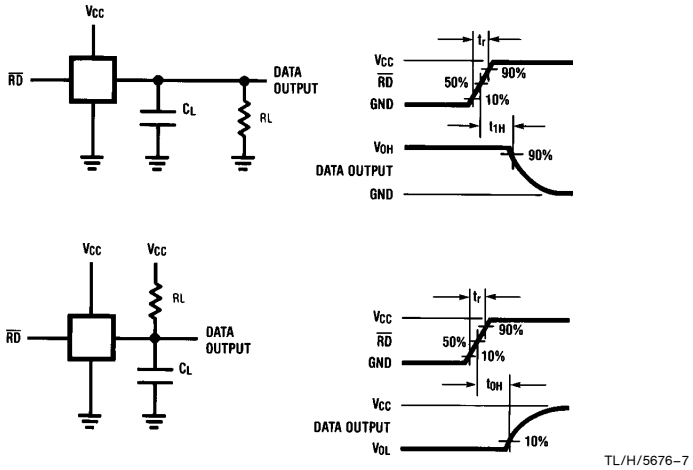

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FIGURE 2. TRI-STATE Test Circuits and Waveforms

Timing Diagrams

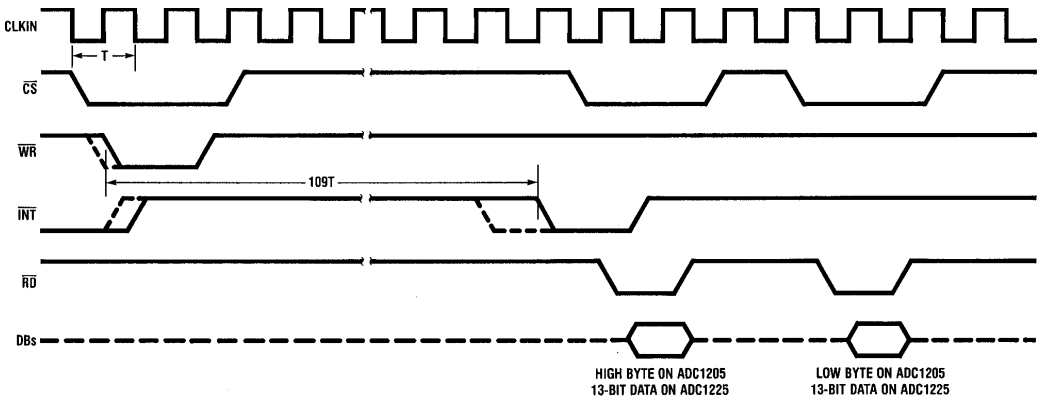

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FIGURE 3. Timing Diagram

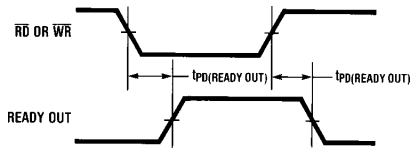

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FIGURE 4. Ready Out

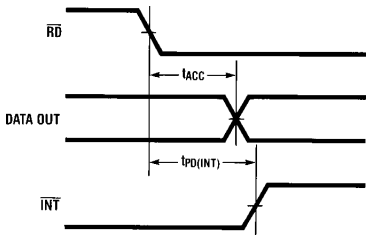

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FIGURE 5. Data Out

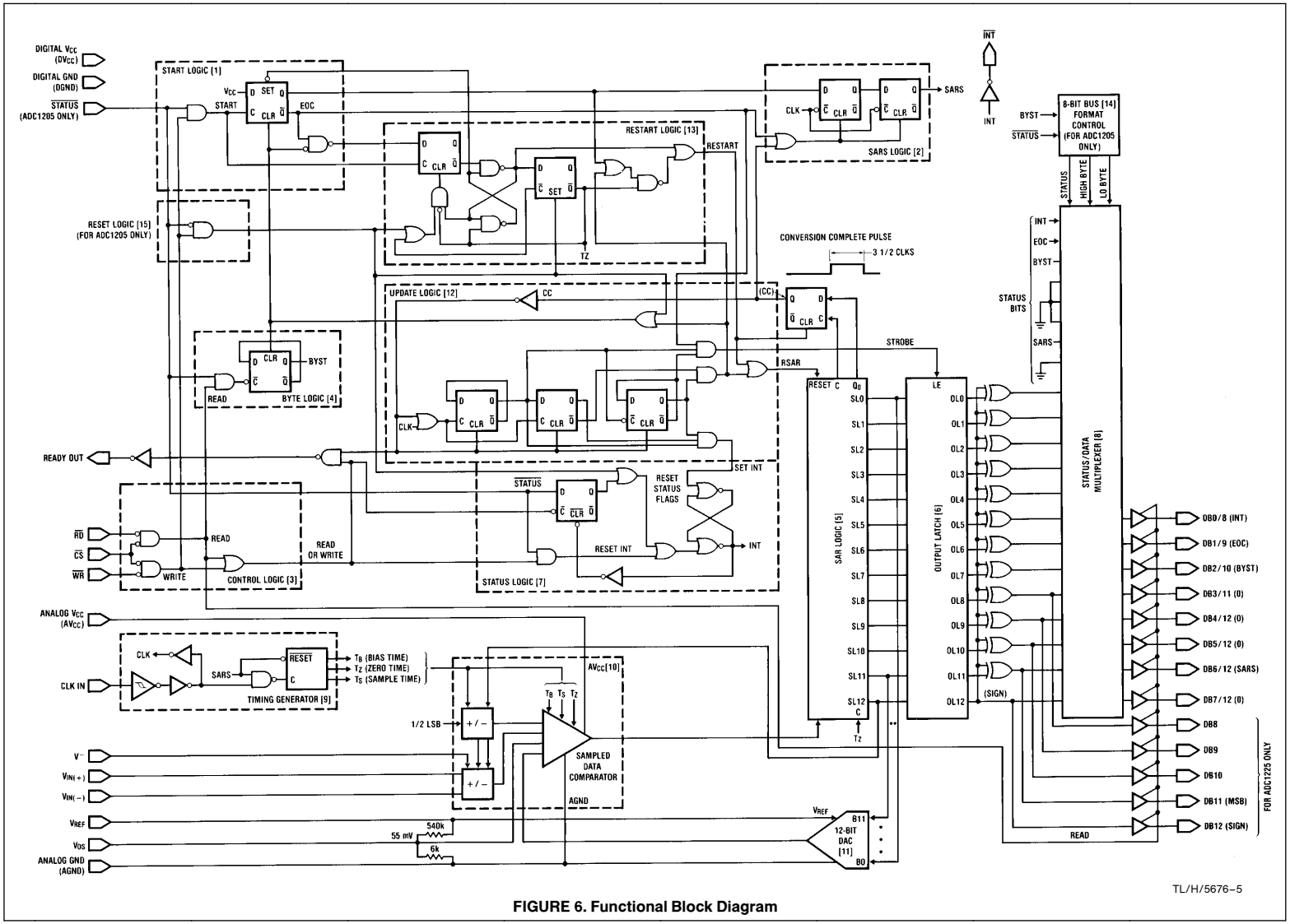

FIGURE 6. Functional Block Diagram

Functional Description

1.0 THE A/D CONVERSION

1.1 STARTING A CONVERSION

When using the ADC1225 or ADC1205 with a microprocessor, starting an A-to-D conversion is like writing to an external memory location. The $\overline{WR}$ and $\overline{CS}$ lines are used to start the conversion. The simplified logic (*Figure 6*) shows that the falling edge of $\overline{WR}$ with $\overline{CS}$ low clocks the D-type flip-flop and initiates the conversion sequence. A new conversion can therefore be restarted before the end of the previous sequence. $\overline{INT}$ going low indicates the conversion's end.

1.2 THE CONVERSION PROCESS (Numbers designated by [ ] refer to portions of *Figure 6*.)

The SARS LOGIC [2] controls the A-to-D conversion process. When 'sars' goes high the clock (clk) is gated to the TIMING GENERATOR [9]. One of the outputs of the TIMING GENERATOR, T_Z, provides the clock for the Successive Approximation Register, SAR LOGIC [5]. The T_Z clock rate is 1/8 of the CLK IN frequency.

Inputs to the 12-BIT DAC [11] and control of the SAMPLED DATA COMPARATOR [10] sign logic are provided by the SAR LOGIC. The first step in the conversion process is to set the sign to positive (logic '0') and the input of the DAC to 000 (HEX notation). If the differential input, $V_{IN(+)} - V_{IN(-)}$, is positive the sign bit will remain low. If it is negative the sign bit will be set high. Differential inputs of only a few hundred microvolts are enough to provide full logic swings at the output of the SAMPLED DATA COMPARATOR.

The sign bit indicates the polarity of the differential input. If it is set high, the negative input must have been greater than the positive input. By reversing the polarity of the differential input, $V_{IN(+)}$ and $V_{IN(-)}$ are interchanged and the DAC sees the negative input as positive. The input polarity reversal is done digitally by changing the timing on the input sampling switches of the SAMPLED DATA COMPARATOR. Thus, with almost no additional circuitry, the A/D is extended from a unipolar 12-bit to a bipolar 12-bit (12-bit plus sign) device.

After determining the input polarity, the conversion proceeds with the successive approximation process. The SAR LOGIC successively tries each bit of the 12-BIT DAC. The most significant bit (MSB), B11, has a weight of 1/2 of V_{REF}. The next bit, B10, has a weight of 1/4 V_{REF}. Each successive bit is reduced in weight by a factor of 2 which gives the least significant bit (LSB) a weight of 1/4096 V_{REF}.

When the MSB is tried, the comparator compares the DAC output, $V_{REF}/2$, to the analog input. If the analog input is greater than $V_{REF}/2$ the comparator tells the SAR LOGIC to set the MSB. If the analog input is less than $V_{REF}/2$ the comparator tells the SAR LOGIC to reset the MSB. On the next bit-test the DAC output will either be 3/4 V_{REF} or 1/4 V_{REF} depending on whether the MSB was set or not. Following this sequence through for each successive bit will approximate the analog input to within 1-bit (one part in 4096).

On completion of the LSB bit-test the conversion-complete flip-flop (CC) is set, signifying that the conversion is finished. The end-of-conversion (EOC) and interrupt ($\overline{INT}$) lines are not changed at this time. Some internal housekeeping tasks must be completed before the outside world is notified that the conversion is finished.

Setting CC enables the UPDATE LOGIC [12]. This logic controls the transfer of data from the SAR LOGIC to the OUTPUT LATCH [6] and resets the internal logic in preparation for a new conversion. This means that when EOC goes high, a new conversion can be immediately started since the internal logic has already been reset. In the same way, data is transferred to the OUTPUT LATCH prior to issuing an interrupt. This assures that data can be read immediately after $\overline{INT}$ goes low.

2.0 READING THE A/D

The ADC 1225 makes all thirteen bits of the conversion result available in parallel. Taking $\overline{CS}$ and $\overline{RD}$ low enables the TRI-STATE® output buffers. The conversion result is represented in 2's complement format.

The ADC1205 makes the conversion result available in two eight-bit bytes. The output format is 2's complement with extended sign. Data is right justified and presented high byte first. With $\overline{CS}$ low and $\overline{STATUS}$ high, the high byte (DB12–DB8) will be enabled on the output buffers the first time $\overline{RD}$ goes low. When $\overline{RD}$ goes low a second time, the low byte (DB7–DB0) will be enabled. On each read operation, the 'byst' flip-flop is toggled so that on successive reads alternate bytes will be available on the outputs. The 'byst' flip-flop is always reset to the high byte at the end of a conversion. Table 1 below shows the data bit locations on the ADC1205.

The ADC1205's $\overline{STATUS}$ pin makes it possible to read the conversion status and the state of the 'byst' flip-flop. With $\overline{RD}$, $\overline{STATUS}$ and $\overline{CS}$ low, this information appears on the data bus. The 'byst' status appears on pin 18 (DB2/DB10). A low output on pin 18 indicates that the next data read will be the high byte. A high output indicates that the next data read will be the low byte. A high status bit on pin 22 (DB6/DB12) indicates that the conversion is in progress. A high output appears on pin 17 (DB1/DB9) when the conversion is completed and the data has been transferred to the output latch. A high output on pin 16 (DB0/DB8) indicates that the conversion has been completed and the data is ready to read. This status bit is reset when a new conversion is initiated, data is read, or status is read. When reading status or a conversion result, $\overline{STATUS}$ should always change states at least 600 ns before $\overline{RD}$ goes low. If the conversion status information is not needed, the $\overline{STATUS}$ pin should be hardwired to V^+. Table 2 summarizes the meanings of the four status bits.

TABLE I. Data Bit Locations, ADC1205

HIGH BYTE	DB12	DB12	DB12	DB12	DB11	DB10	DB9	DB8
LOW BYTE	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0

TABLE II. Status Bit Locations and Meanings

Status Bit Location	Status Bit	Meaning	Condition to Clear Status Bit
DB6	SARS	''High'' indicates that the conversion is in progress	
DB2	BYST	''Low'' indicates that the next data read is the high byte. ''High'' indicates that the next data read is the low byte	Status write or toggle it with data read

Functional Description (Continued)

TABLE II. Status Bit Locations and Meanings
(Continued)

Status Bit Location	Status Bit	Meaning	Condition to Clear Status Bit
DB1	EOC	''High'' indicates that the conversion is completed and data is transferred to the output latch.	
DB0	INT	''High'' indicates that it is the end of the conversion and the data is ready to read	Data read or status read or status write

3.0 INTERFACE

3.1 RESET OF INTERRUPT

$\overline{INT}$ goes low at the end of the conversion and indicates that data is transferred to the output latch. By reading data, $\overline{INT}$ will be reset to high on the leading edge of the first read ($\overline{RD}$ going low). $\overline{INT}$ is also reset on the leading (falling) edge of $\overline{WR}$ when starting a conversion.

3.2 READY OUT

To simplify the hardware connection to high speed microprocessors, a READY OUT line is provided. This allows the A-to-D to insert a wait state in the μP's read cycle. The equivalent circuit and the timing diagram for READY OUT is shown in *Figures 7* and *8*.

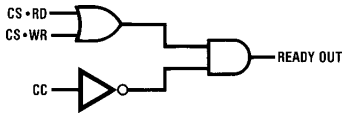

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FIGURE 7. READY OUT Equivalent Circuit

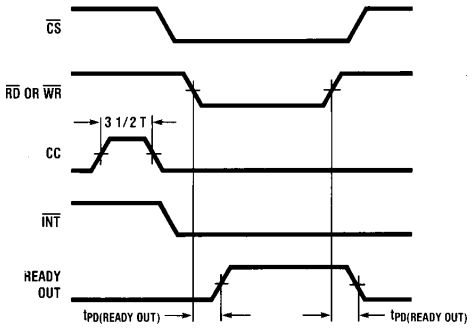

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FIGURE 8. READY OUT Timing Diagram

3.3 RESETTING THE A/D

All the internal logic can be reset, which will abort any conversion in process and reset the status bits. The reset function is achieved by performing a status write ($\overline{CS}$, $\overline{WR}$ and $\overline{STATUS}$ are low).

3.4 ADDITIONAL TIMING AND INTERFACE OPTIONS

ADC1225

1. $\overline{WR}$ and $\overline{RD}$ can be tied together with $\overline{CS}$ low continuously or strobed. The previous conversion's data will be available when the $\overline{WR}$ and $\overline{RD}$ are low as shown below.

One drawback is that, since the conversion is started on the falling edge and the data read on the rising edge of $\overline{WR}/\overline{RD}$, the first data access will have erroneous information depending on the power-up state of the internal output latches.

If the $\overline{WR}/\overline{RD}$ strobe is longer than the conversion time, $\overline{INTR}$ will never go low to signal the end of a conversion. The conversion will be completed and the output latches will be updated. In this case the READY OUT signal can be used to sense the end of the conversion since it will go low when the output latches are being updated.

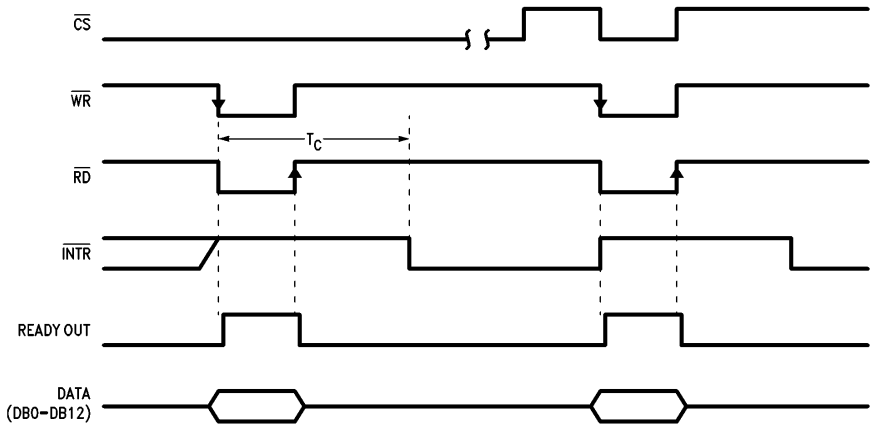

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FIGURE 9

Functional Description (Continued)

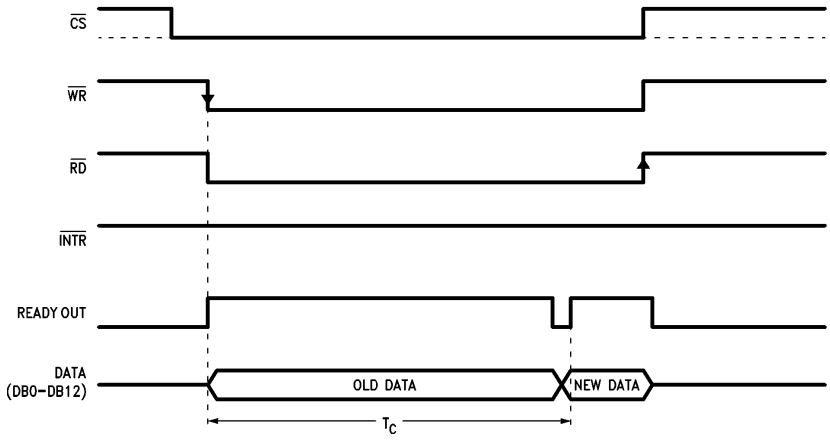

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FIGURE 10

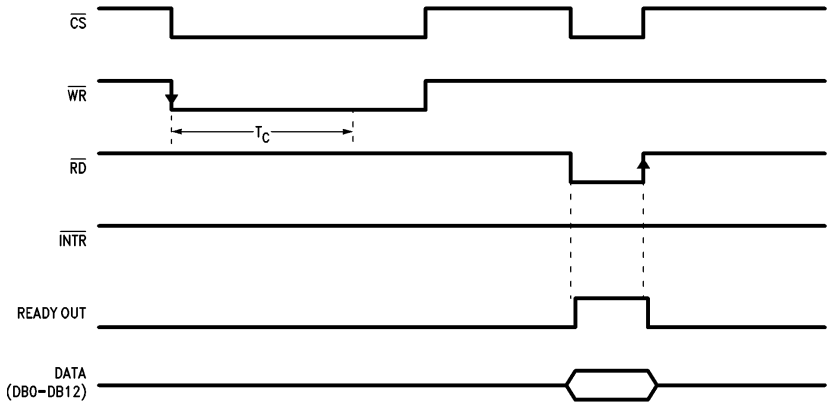

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FIGURE 11

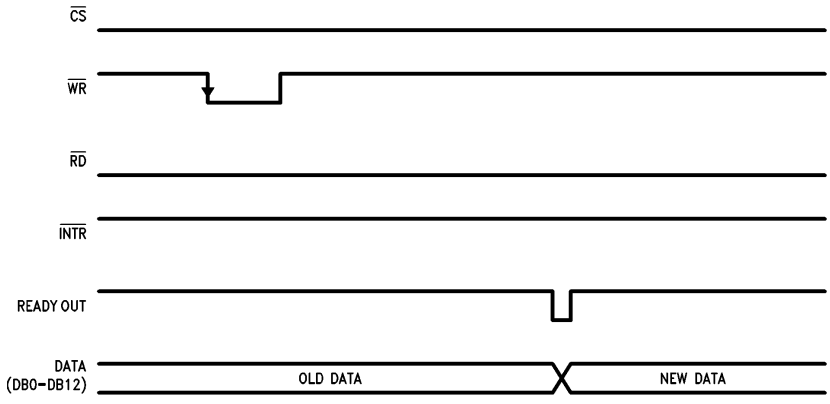

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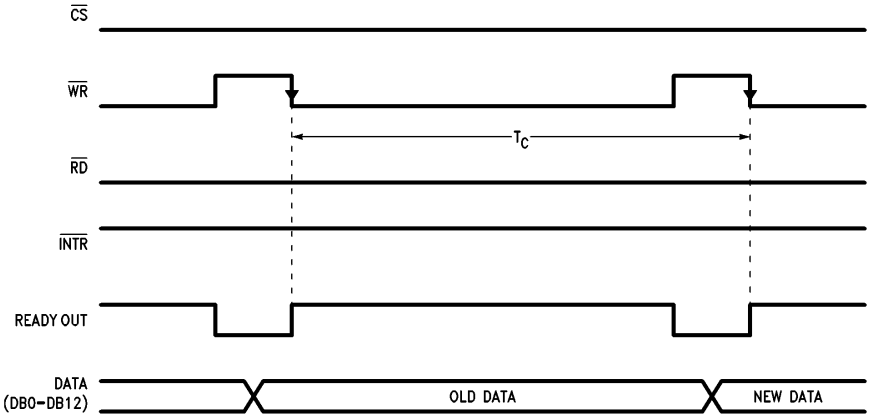
FIGURE 12

Functional Description (Continued)



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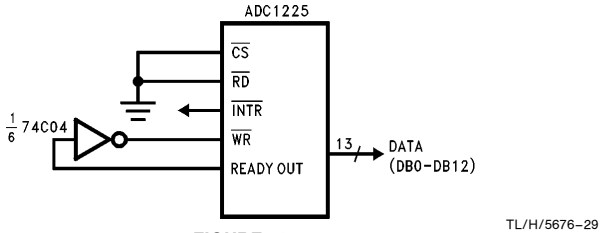

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FIGURE 13

When using this method of conversion only one strobe is necessary and the rising edge of $\overline{WR}$/$\overline{RD}$ can be used to read the current conversion results. These methods reduce the throughput time of the conversion since the $\overline{RD}$ and $\overline{WR}$ cycles are combined.

2. With the standard timing $\overline{WR}$ pulse width longer than the conversion time a conversion is completed but the $\overline{INTR}$ will never go low to signal the end of a conversion. The output latches will be updated and valid information will be available when the $\overline{RD}$ cycle is accomplished.

3. Tying $\overline{CS}$ and $\overline{RD}$ low continuously and strobing $\overline{WR}$ to initiate a conversion will also yield valid data. The $\overline{INTR}$ will never go low to signal the end of a conversion and the digital outputs will always be enabled, so using $\overline{INTR}$ to strobe the $\overline{WR}$ line for a continuous conversion cannot be done with this part.

A simple stand-alone circuit can be accomplished by driving $\overline{WR}$ with the inverse of the READY OUT signal using a simple inverter as shown below.

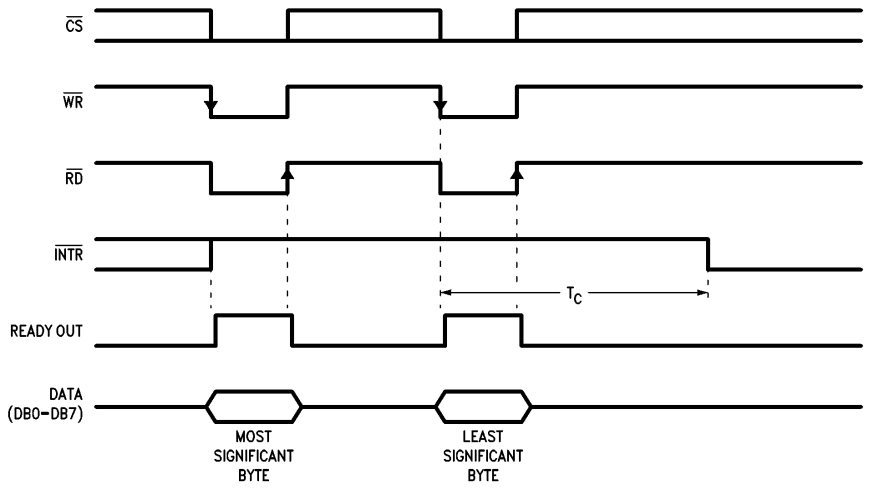

FIGURE 14

TL/H/5676–30

Functional Description (Continued)

ADC1205

Case 1 would be the only one that would appy to the ADC1205 since two $\overline{RD}$ strobes are necessary to retrieve the 13 bits of information on the 8 bit data bus. Simultaneously strobing $\overline{WR}$ and $\overline{RD}$ low will enable the most significant byte on DB0–DB7 and start a conversion. Pulsing $\overline{WR}/\overline{RD}$ low before the end of this conversion will enable the least significant byte of data on the outputs and restart a conversion.

4.0 REFERENCE VOLTAGE

The voltage applied to the reference input of the converter defines the voltage span of the analog inputs (the difference between $V_{IN(+)}$ and $V_{IN(-)}$, over which 4096 positive output codes and 4096 negative output codes exist. The A-to-D can be used in either ratiometric or absolute reference applications. V_{REF} must be connected to a voltage source capable of driving the reference input resistance (typically 4 kΩ).

In a ratiometric system, the analog input voltage is proportional to the voltage used for the A/D reference. When this voltage is the system power supply, the V_{REF} pin can be tied to V_{CC}. This technique relaxes the stability requirement of the system reference as the analog input and A/D reference move together maintaining the same output code for a given input condition.

For absolute accuracy, where the analog input varies between very specific voltage limits, the reference pin can be biased with a time and temperature stable voltage source. In general, the magnitude of the reference voltage will require an initial adjustment to null out full-scale errors.

5.0 THE ANALOG INPUTS

5.1 DIFFERENTIAL VOLTAGE INPUTS AND COMMON MODE REJECTION

The differential inputs of the ADC1225 and ADC1205 actually reduce the effects of common-mode input noise, i.e., signals common to both $V_{IN(+)}$ and $V_{IN(-)}$ inputs (60 Hz is most typical). The time interval between sampling the "+" and "−" input is 4 clock periods. Therefore, a change in the common-mode voltage during this short time interval may cause conversion errors. For a sinusoidal common-mode signal the error would be:

$$V_{ERROR(MAX)} = V_{PEAK}\,(2\pi\, f_{CM})\,\frac{4}{f_{CLK}}$$

where f_{CM} is the frequency of the common-mode signal, V_{PEAK} is its peak voltage value and f_{CLK} is the converter's clock frequency. In most cases V_{ERROR} will not be significant. For a 60 Hz common-mode signal to generate a ¼ LSB error (300 μV) with the converter running at 1 MHz its peak value would have to be 200mV.

5.2 INPUT CURRENT

Due to the sampling nature of the analog inputs, short duration spikes of current enter the "+" input and exit the "−" input at the leading clock edges during the actual conversion. These currents decay rapidly and do not cause errors as the internal comparator is strobed at the end of a clock period.

5.3 INPUT BYPASS CAPACITORS

Bypass capacitors at the inputs will average the current spikes mentioned in 5.2 and cause a DC current to flow through the output resistance of the analog signal source. This charge pumping action is worse for continuous conversions with the $V_{IN(+)}$ input voltage at full-scale. For continuous conversions with a 1 MHz clock frequency and the $V_{IN(+)}$ input at 5V, the average input current is approximately 5 μA. For this reason bypass capacitors should not be used at the analog inputs for high resistance sources (R_{SOURCE} 100 Ω).

If input bypass capacitors are necessary for noise filtering and high source resistance is desirable to minimize capacitor size, the detrimental effects of the voltage drop across this input resistance, due to the average value of the input current, can be minimized with a full-scale adjustment while the given source resistance and input bypass capacitor are both in place. This is effective because the average value of the input current is a linear function of the differential input voltage.

5.4 INPUT SOURCE RESISTANCE

Large values of source resistance where an input bypass capacitor is not used, will not cause errors as the input currents settle out prior to the comparison time. If a low pass filter is required in the system, use a low valued series resistor ($R \leq 100\ \Omega$) for a passive RC section or add an op amp RC active low pass filter. For low source resistance applications, ($R_{SOURCE} \leq 100\ \Omega$) a 0.001 μF bypass capacitor at the inputs will prevent pickup due to series lead inductance of a long wire. A 100 Ω series resistor can be used to isolate this capacitor – both the R and C are placed outside the feedback loop – from the output of an op amp, if used.

5.5 NOISE

The leads to the analog inputs should be kept as short as possible to minimize input noise coupling. Both noise and undesired digital clock coupling to these inputs can cause errors. Input filtering can be used to reduce the effects of these sources, but careful note should be taken of sections 5.3 and 5.4 if this route is taken.

6.0 POWER SUPPLIES

Noise spikes on the V_{CC} supply line can cause conversion errors as the comparator will respond to this noise. Low inductance tantalum capacitors of 1 μF or greater are recommended for supply bypassing. Separate bypass caps should be placed close to the DV_{CC} and AV_{CC} pins. If an unregulated voltage source is available in the system, a separate LM340LAZ-5.0 voltage regulator for the A-to-D's V_{CC} (and other analog circuitry) will greatly reduce digital noise on the supply line.

7.0 ERRORS AND REFERENCE VOLTAGE ADJUSTMENTS

7.1 ZERO ADJUST

The zero error of the A/D converter relates to the location of the first riser of the transfer function and can be measured by grounding the $V_{IN(-)}$ input and applying a small magnitude positive voltage to the $V_{IN(+)}$ input. Zero error is the difference between the actual DC input voltage necessary to just cause an output digital code transition from all zeroes to 0,0000,0000,0001 and the ideal ½ LSB value (½ LSB = 0.61 mV for $V_{REF} = 5\ V_{DC}$). Zero error can be adjusted as shown in *Figure 15*. $V_{IN(+)}$ is forced to 0.61 mV, and $V_{IN(-)}$ is forced to 0V. The potentiometer is adjusted until the digital output code changes from all zeroes to 0,000,0000,0001.

Functional Description (Continued)

A simpler, although slightly less accurate, approach is to ground $V_{IN(+)}$ and $V_{IN(-)}$, and adjust for all zeros at the output. Error will be well under ½ LSB if the adjustment is done so that the potentiometer is "centered" within the 0,000,000 range. A positive voltage at the V_{OS} input will reduce the output code. The adjustment range is +4 to −30 LSB.

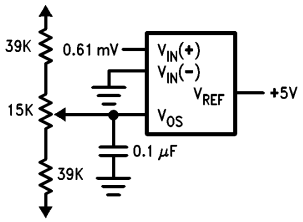

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FIGURE 15. Zero Adjust Circuit

7.2 POSITIVE AND NEGATIVE FULL-SCALE ADJUSTMENT

Unipolar Inputs

Apply a differential input voltage which is 1.5 LSB below the desired analog full-scale voltage (V_F) and adjust the magnitude of the V_{REF} input so that the output code is just changing from 0,1111,1111,1110 to 0,1111,1111,1111.

Bipolar Inputs

Do the same procedure outlined above for the unipolar case and then change the differential input voltage so that the digital output code is just changing from 1,0000,0000,0001 to 1,0000,0000,0000. Record the differential input voltage, V_X. the ideal differential input voltage for that transition should be;

$$\left(-V_F + \frac{V_F}{8192}\right)$$

Calculate the difference between Vx and the ideal voltage;

$$\Delta = V_X - \left(-V_F + \frac{V_F}{8192}\right)$$

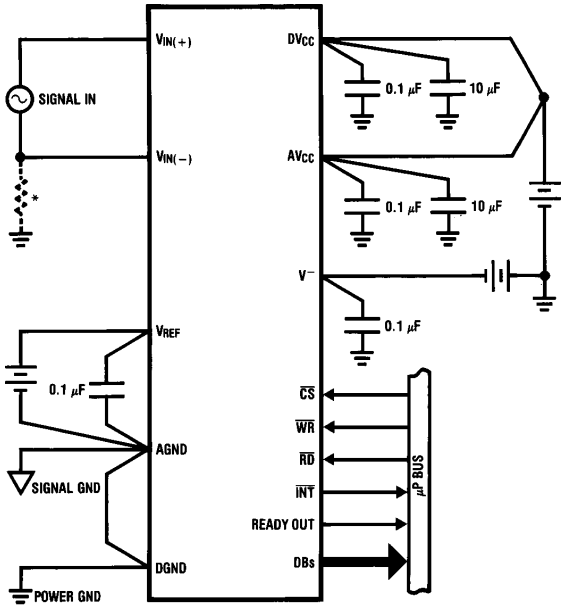
Then apply a differential input voltage of;

$$\left(V_X - \frac{\Delta}{2}\right)$$

and adjust the magnitude of V_{REF} so the digital output code is just changing from 1,0000,0000,0001 to 1,0000,0000,0000. That will obtain the positive and negative full-scale transition with symmetrical minimum error.

Typical Applications

*Input must have some current return path to signal ground



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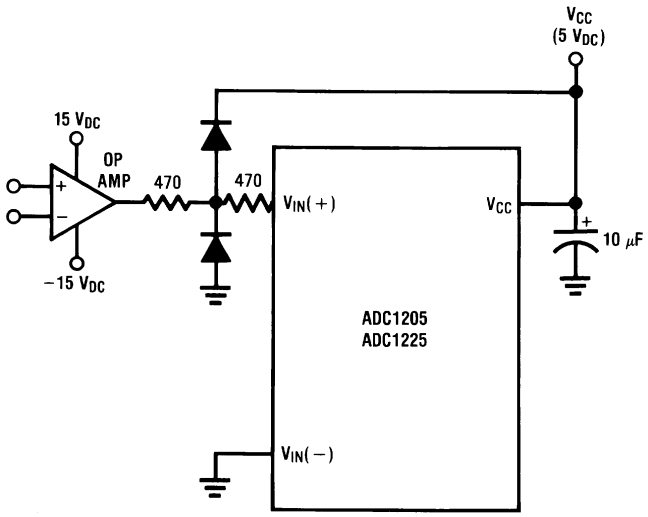
Typical Applications (Continued)

Protecting the Input



Diodes are 1N914

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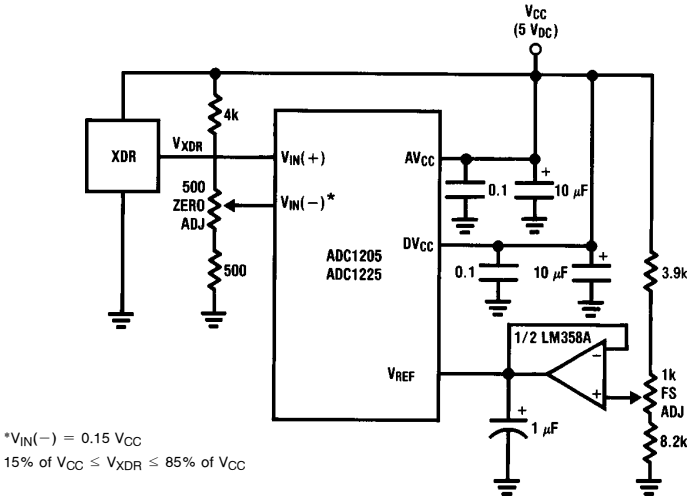
Operating with Ratiometric Transducers



*$V_{IN}(-) = 0.15\ V_{CC}$

15% of $V_{CC} \leq V_{XDR} \leq 85\%$ of V_{CC}

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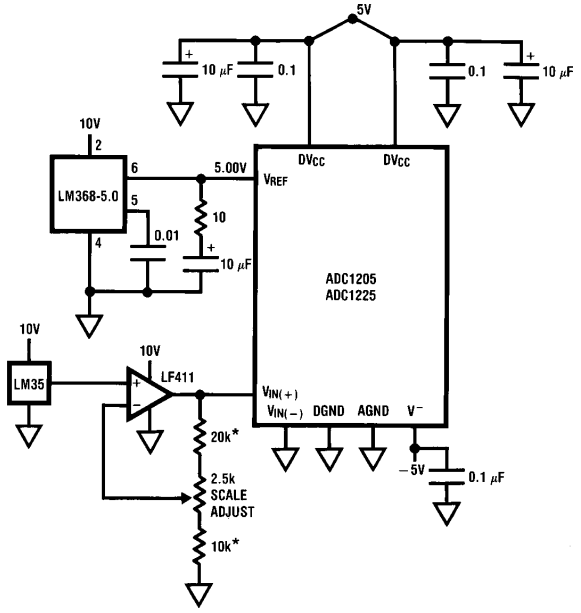
Typical Applications (Continued)

Bipolar Input Temperature Converter



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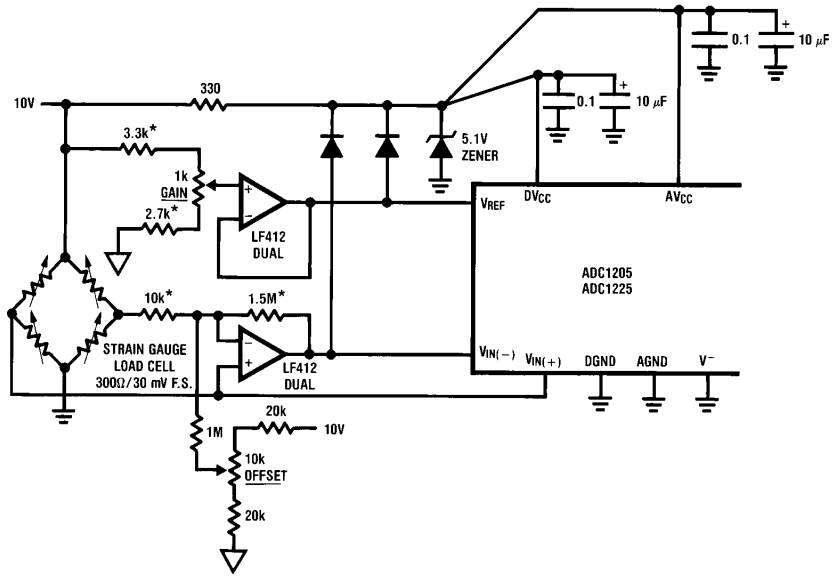
+150 to −55°C with 0.04°C resolution

Note: * resistors are 1% metal film types

Strain Gauge Converter with .025% Resolution and Single Power Supply



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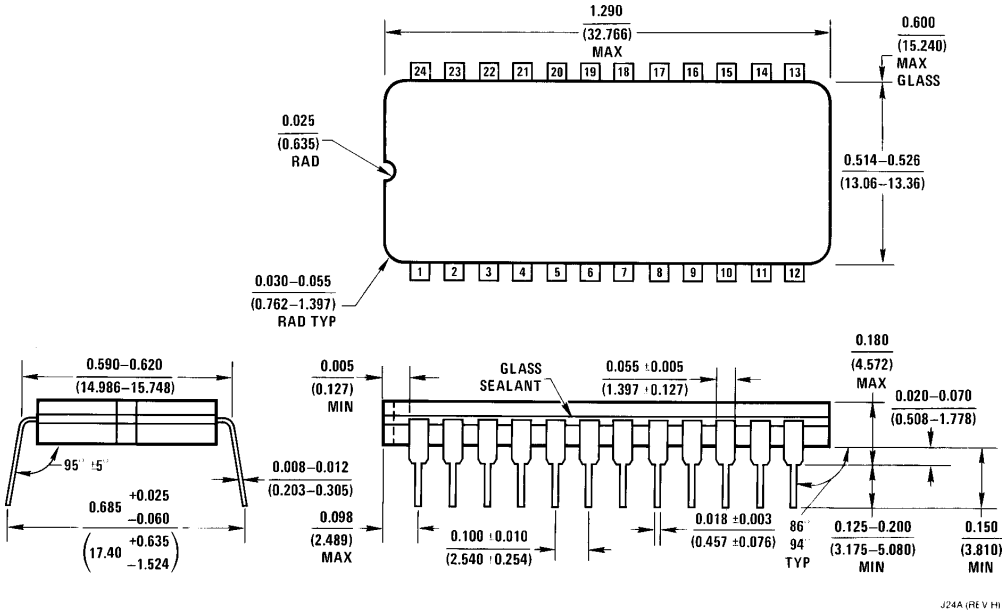
Note: 1) * resistors are 1% metal film types

2) LF412 power +10V and ground

Ordering Information

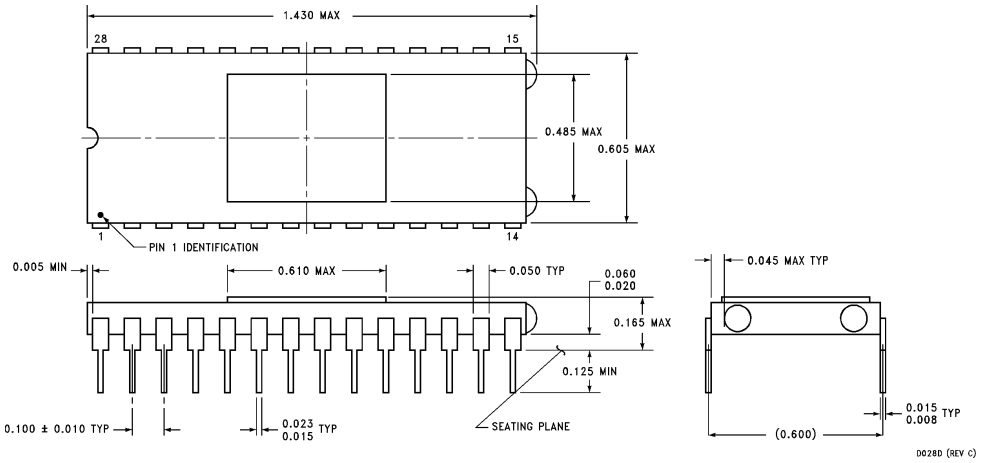
Temperature Range		0°C to 70°C		−40°C to +85°C	
Non-Linearity	0.024%	ADC1205CCJ-1	ADC1225CCD-1	ADC1205CCJ	ADC1225CCD
Package Outline		J24A	D28D	J24A	D28D

Physical Dimensions inches (millimeters)



Ceramic Dual-In Line Package (J)
Order Number ADC1205CCJ-1 or ADC1205CCJ
NS Package Number J24A

Physical Dimensions inches (millimeters) (Continued)



Ceramic Dual-In-Line Package (D)
Order Number ADC1225CCD-1 or ADC1225CCD
NS Package Number D28D

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