High Accuracy Ultralow I_Q, 300 mA, anyCAP® Low Dropout Regulator

ADP3333

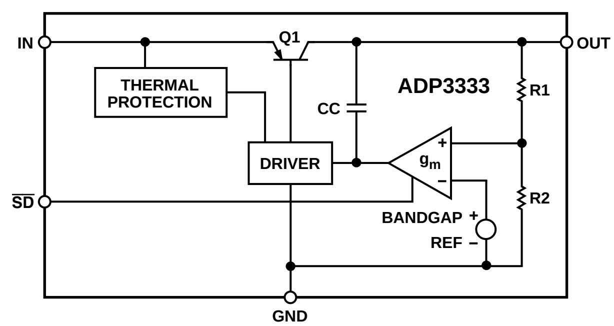
FEATURES

- High Accuracy Over Line and Load: ±0.8% @ 25°C, ±1.8% Over Temperature
- Ultralow Dropout Voltage: 230 mV (Max) @ 300 mA
- Requires Only C_O = 1.0 µF for Stability
- anyCAP = Stable with Any Type of Capacitor (Including MLCC)
- Current and Thermal Limiting
- Low Noise
- Low Shutdown Current: < 1 µA
- 2.6 V to 12 V Supply Range
- –40°C to +85°C Ambient Temperature Range
- Ultrasmall 8-Lead MSOP Package

APPLICATIONS

- Cellular Phones
- PCMCIA Cards
- Personal Digital Assistants (PDAs)
- DSP/ASIC Supplies

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

ADP3333 is a member of the ADP333x family of precision low dropout anyCAP voltage regulators. Pin-compatible with the MAX8860, the ADP3333 operates with a wider input voltage range of 2.6 V to 12 V and delivers a load current up to 300 mA. ADP3333 stands out from other conventional LDOs with a novel architecture and an enhanced process that enables it to offer performance advantages over its competition. Its patented design requires only a 1.0 µF output capacitor for stability. This device is insensitive to output capacitor Equivalent Series Resistance (ESR), and is stable with any good quality capacitor, including ceramic (MLCC) types for space-restricted applications. ADP3333 achieves exceptional accuracy of ±0.8% at room temperature and ±1.8% over temperature, line and load variations. The dropout voltage of ADP3333 is only 140 mV (typical) at 300 mA. This device also includes a safety current limit, thermal overload protection and a shutdown feature. In shutdown mode, the ground current is reduced to less than 1 µA. The ADP3333 has ultralow quiescent current, 70 µA (typ) in light load situations.

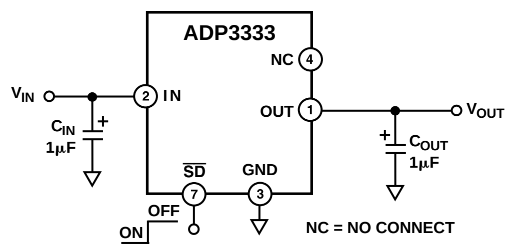


Figure 1. Typical Application Circuit

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REV. 0

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ADP3333–SPECIFICATIONS[1] (V_{IN} = 6.0 V, C_{IN} = C_{OUT} = 1.0 µF, T_J = –40°C to +125°C, unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
OUTPUT						
Voltage Accuracy[2]	V_{OUT}	V_{IN} = V_{OUTNOM} 0.3 V to 12 V	0.8		0.8	%
		I_L = 0.1 mA to 300 mA				
		T_J = 25°C				
		V_{IN} = V_{OUTNOM} 0.3 V to 12 V	–1.8		+1.8	%
		I_L = 0.1 mA to 300 mA				
Line Regulation[2]		V_{IN} = V_{OUTNOM} 0.3 V to 12 V		0.04		mV/V
		T_J = 25°C				
Load Regulation		I_L = 0.1 mA to 300 mA		0.04		mV/mA
		T_J = 25°C				
Dropout Voltage	V_{DROP}	V_{OUT} = 98% of V_{OUTNOM}				
		I_L = 300 mA		140	230	mV
		I_L = 200 mA		105	185	mV
		I_L = 0.1 mA		30		mV
Peak Load Current	I_{LDPK}	V_{IN} = V_{OUTNOM} + 1 V		600		mA
Output Noise	V_{NOISE}	f = 10 Hz–100 kHz, C_L = 10 µF		45		µV rms
		I_L = 300 mA				
GROUND CURRENT						
In Regulation	I_{GND}	I_L = 300 mA		2.0	5.5	mA
		I_L = 300 mA, T_J = 25°C		2.0	4.3	mA
		I_L = 300 mA, T_J = 85°C		1.5	3.3	mA
		I_L = 200 mA		1.4		mA
		I_L = 10 mA		200	275	µA
		I_L = 0.1 mA		70	100	µA
In Dropout	I_{GND}	V_{IN} = V_{OUTNOM} – 100 mV		70	190	µA
		I_L = 0.1 mA,				
		V_{IN} = V_{OUTNOM} – 100 mV		70	160	µA
		I_L = 0.1 mA, T_J = 0°C to 125°C				
In Shutdown	I_{GNDSD}	$\overline{SD}$ = 0 V, V_{IN} = 12 V		0.01	1	µA
SHUTDOWN						
Threshold Voltage	$V_{\overline{THSD}}$	ON	2.0			V
		OFF			0.4	V
$\overline{SD}$ Input Current	$I_{\overline{SD}}$	$0 \le \overline{SD} \le 12$ V		0.85	7	µA
		$0 \le \overline{SD} \le 5$ V		0.8	4.5	µA
Output Current In Shutdown	$I_{\overline{OSD}}$	T_J = 25°C V_{IN} = 12 V		0.01	1	µA
		T_J = 125°C V_{IN} = 12 V		0.01	1	µA

NOTES
[1]Application stable with no load.
[2]V_{IN} = 2.6 V for models with $V_{OUTNOM} \le 2.3$ V.
Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

Input Supply Voltage . . . . –0.3 V to +16 V
Shutdown Input Voltage . . . . –0.3 V to +16 V
Power Dissipation . . . . Internally Limited
Operating Ambient Temperature Range . . . . –40°C to +85°C
Operating Junction Temperature Range . . . –40°C to +125°C
θ_{JA} (4-layer) . . . . 158°C/W
θ_{JA} (2-layer) . . . . 220°C/W
Storage Temperature Range . . . . –65°C to +150°C
Lead Temperature (Soldering, 10 sec) . . . . 300°C
Vapor Phase (60 sec) . . . . 215°C
Infrared (15 sec) . . . . 220°C

*This is a stress rating only; operation beyond these limits can cause the device to be permanently damaged.

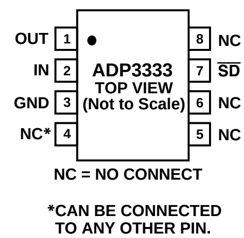
PIN FUNCTION DESCRIPTIONS

Pin	Mnemonic	Function
1	OUT	Output of the Regulator. Bypass to ground with a 1.0 µF or larger capacitor.
2	IN	Input pin. Bypass to ground with a 1.0 µF or larger capacitor.
3	GND	Ground Pin
4–6, 8	NC	No Connect
7	$\overline{SD}$	Active Low Shutdown Pin. Connect to ground to disable the regulator output. When shutdown is not used, his pin should be connected to the input pin

ORDERING GUIDE

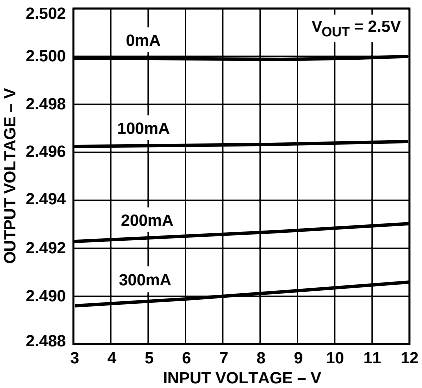
Model	Output Voltage	Package Option	Branding Information
ADP3333ARM-1.5	1.5 V	RM-8 (MSOP-8)	LKA
ADP3333ARM-1.8	1.8 V	RM-8 (MSOP-8)	LKB
ADP3333ARM-2.5	2.5 V	RM-8 (MSOP-8)	LKC
ADP3333ARM-2.77	2.77 V	RM-8 (MSOP-8)	LKD
ADP3333ARM-3	3 V	RM-8 (MSOP-8)	LKE
ADP3333ARM-3.15	3.15 V	RM-8 (MSOP-8)	LKF
ADP3333ARM-3.3	3.3 V	RM-8 (MSOP-8)	LKG
ADP3333ARM-5	5 V	RM-8 (MSOP-8)	LKH

PIN CONFIGURATION

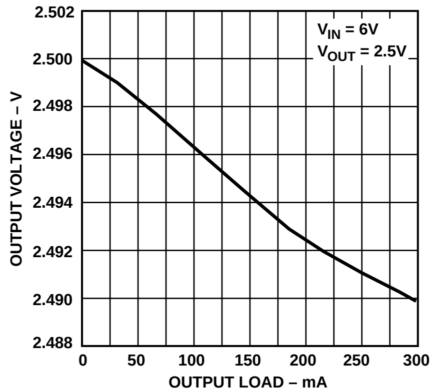


CAUTION

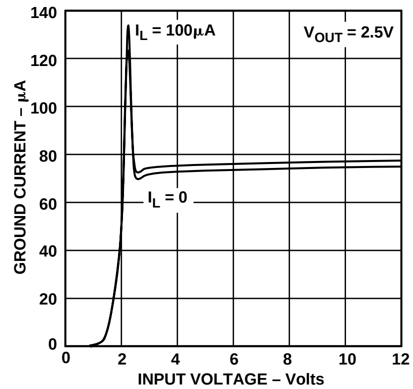
ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADP3333 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high-energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



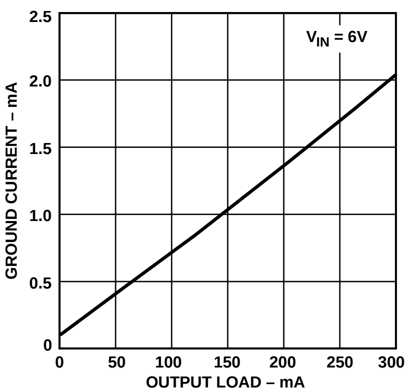
TPC 1. Line Regulation Output Voltage vs. Supply Voltage



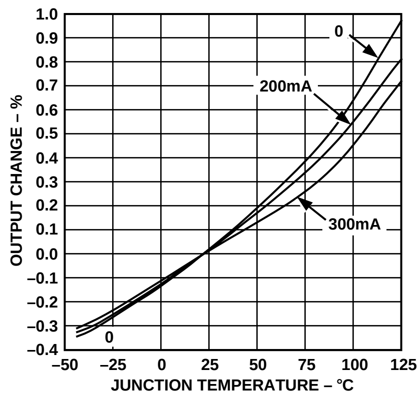
TPC 2. Output Voltage vs. Load Current



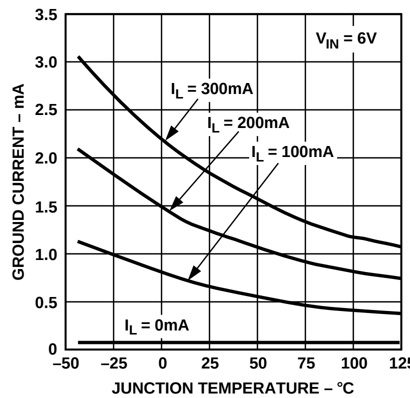
TPC 3. Ground Current vs. Supply Voltage



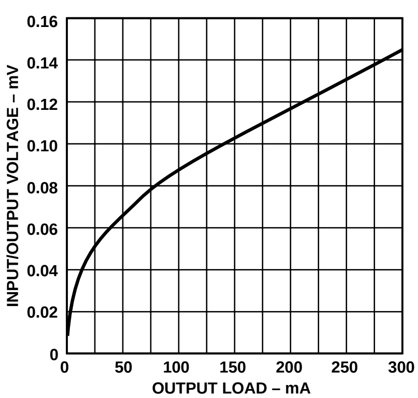
TPC 4. Ground Current vs. Load Current



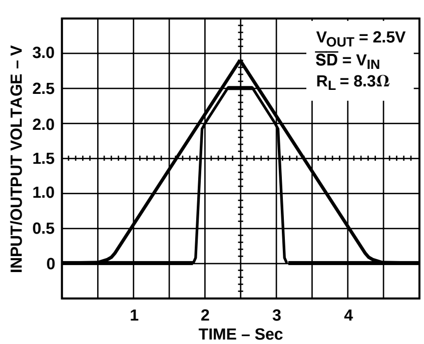
TPC 5. Output Voltage Variation % vs. Junction Temperature



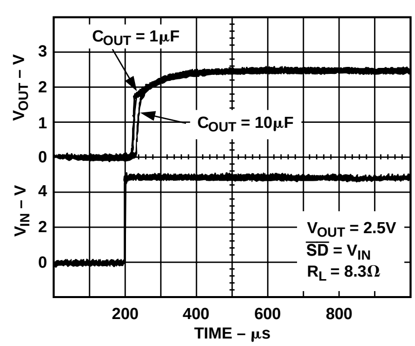
TPC 6. Ground Current vs. Junction Temperature



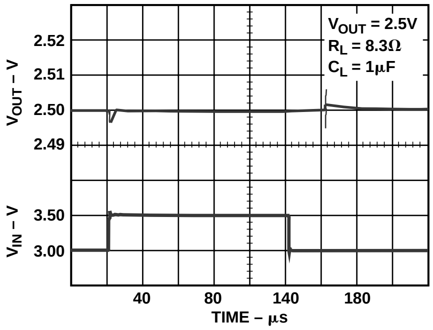
TPC 7. Dropout Voltage vs. Output Current



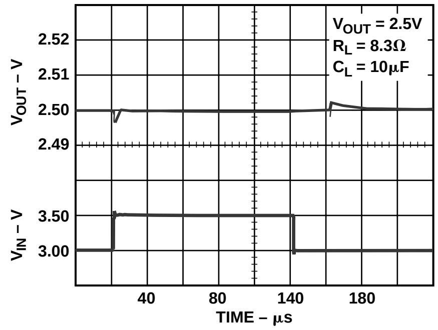
TPC 8. Power-Up/Power-Down



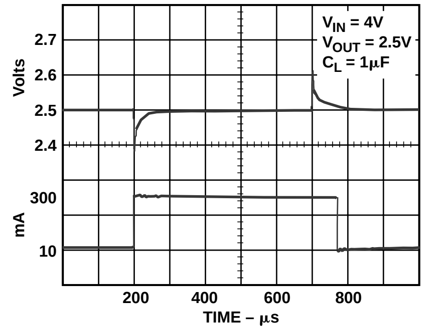
TPC 9. Power-Up Response



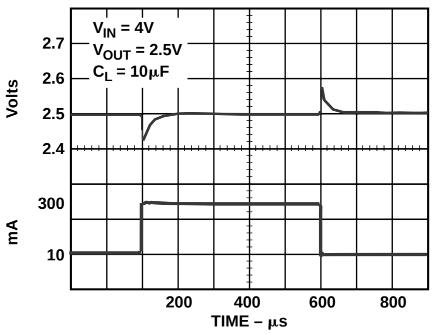
TPC 10. Line Transient Response



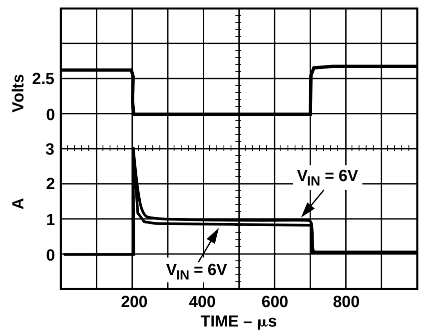
TPC 11. Line Transient Response



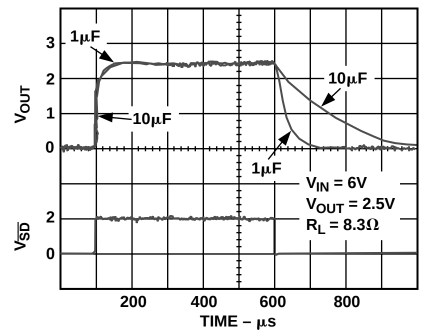
TPC 12. Load Transient Response



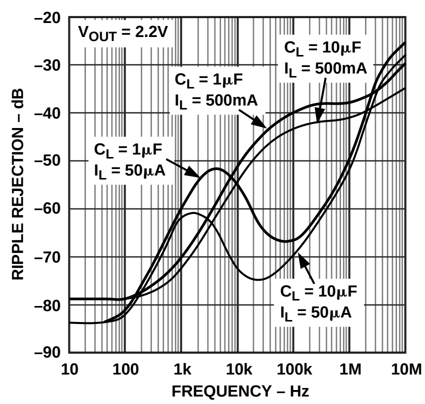
TPC 13. Load Transient Response



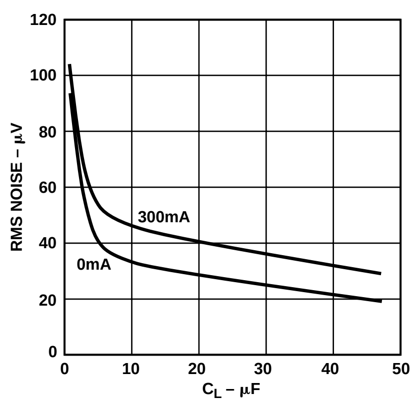
TPC 14. Short Circuit Current



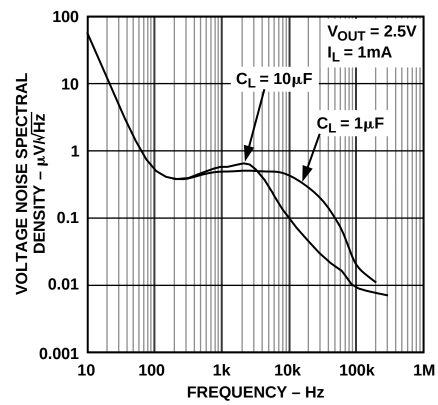
TPC 15. Turn ON-Turn OFF Response



TPC 16. Power Supply Ripple Rejection



TPC 17. RMS Noise vs. C_L (10 Hz–100 kHz)



TPC 18. Output Noise Density

THEORY OF OPERATION

The new anyCAP LDO ADP3333 uses a single control loop for regulation and reference functions see (Figure 2). The output voltage is sensed by a resistive voltage divider consisting of R1 and R2 which is varied to provide the available output voltage option. Feedback is taken from this network by way of a series diode (D1) and a second resistor divider (R3 and R4) to the input of an amplifier.

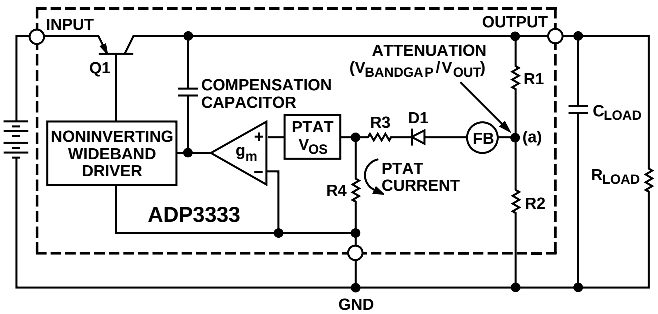


Figure 2. Functional Block Diagram

A very high gain error amplifier is used to control this loop. The amplifier is constructed in such a way that at equilibrium it produces a large, temperature-proportional input "offset voltage" that is repeatable and very well controlled. The temperature proportional offset voltage is combined with the complementary diode voltage to form a "virtual bandgap" voltage, implicit in the network, although it never appears explicitly in the circuit. Ultimately, this patented design makes it possible to control the loop with only one amplifier. This technique also improves the noise characteristics of the amplifier by providing more flexibility on the trade-off of noise sources that leads to a low noise design.

The R1, R2 divider is chosen in the same ratio as the bandgap voltage to the output voltage. Although the R1, R2 resistor divider is loaded by the diode D1 and a second divider consisting of R3 and R4, the values can be chosen to produce a temperature stable output. This unique arrangement specifically corrects for the loading of the divider so that the error resulting from base current loading in conventional circuits is avoided.

The patented amplifier controls a new and unique noninverting driver that drives the pass transistor, Q1. The use of this special noninverting driver enables the frequency compensation to include the load capacitor in a pole splitting arrangement to achieve reduced sensitivity to the value, type and ESR of the load capacitance.

Most LDOs place very strict requirements on the range of ESR values for the output capacitor because they are difficult to stabilize due to the uncertainty of load capacitance and resistance. Moreover, the ESR value, required to keep conventional LDOs stable, changes depending on load and temperature. These ESR limitations make designing with LDOs more difficult because of their unclear specifications and extreme variations over temperature.

With the ADP3333 anyCAP LDO, this is no longer true. It can be used with virtually any good quality capacitor, with no constraint on the minimum ESR. This innovative design allows the circuit to be stable with just a small 1 µF capacitor on the output. Additional advantages of the pole splitting scheme include superior line noise rejection and very high regulator gain which leads to excellent line and load regulation. An impressive ±1.8% accuracy is guaranteed over line, load and temperature.

Additional features of the circuit include current limit and thermal shutdown.

APPLICATION INFORMATION

Capacitor Selection

Output Capacitor

The stability and transient response of the LDO is a function of the output capacitor. The ADP3333 is stable with a wide range of capacitor values, types and ESR (anyCAP). A capacitor as low as 1.0 µF is all that is needed for stability; larger capacitors can be used if high current surges on the output are anticipated. The ADP3333 is stable with extremely low ESR capacitors (ESR » 0), such as Multilayer Ceramic Capacitors (MLCC) or OSCON. Note that the effective capacitance of some capacitor types fall below the minimum over temperature or with dc voltage. Ensure that the capacitor provides at least 1.0 µF of capacitance over temperature and dc bias.

Input Bypass Capacitor

An input bypass capacitor is not strictly required but it is recommended in any application involving long input wires or high source impedance. Connecting a 1.0 µF capacitor from the input to ground reduces the circuit's sensitivity to PC board layout and input transients. If a larger output capacitor is necessary then a larger value input capacitor is also recommended.

Output Current Limit

The ADP3333 is short circuit protected by limiting the pass transistor's base drive current. The maximum output current is limited to about 1 A. See TPC 14.

Thermal Overload Protection

The ADP3333 is protected against damage due to excessive power dissipation by its thermal overload protection circuit. Thermal protection limits the die temperature to a maximum of 165°C. Under extreme conditions (i.e., high ambient temperature and power dissipation) where the die temperature starts to rise above 165°C, the output current will be reduced until the die temperature has dropped to a safe level.

Current and thermal limit protections are intended to protect the device against accidental overload conditions. For normal operation, the device's power dissipation should be externally limited so that the junction temperature will not exceed 125°C.

Calculating Junction Temperature

Device power dissipation is calculated as follows:

$$P_D = (V_{IN} - V_{OUT})\, I_{LOAD} + (V_{IN})\, I_{GND}$$

Where I_{LOAD} and I_{GND} are load current and ground current, V_{IN} and V_{OUT} are the input and output voltages respectively.

Assuming the worst-case operating conditions are I_{LOAD} = 300 mA, I_{GND} = 2.6 mA, V_{IN} = 4.0 V and V_{OUT} = 3.0 V, the device power dissipation is:

$$P_D = (4.0\,V - 3.0\,V)\, 300\, mA + (4.2\,V)\, 2.0\, mA = 308\, mW$$

The package used on the ADP3333 has a thermal resistance of 158°C/W for 4-layer boards. The junction temperature rise above ambient will be approximately equal to:

$$T_{JA} = 0.308\, W \times 158°C / W = 48.7°C$$

So, to limit the junction temperature to 125°C, the maximum allowable ambient temperature is:

$$T_{A(MAX)} = 125°C - 48.7°C = 76.3°C$$

Shutdown Mode

Applying a high signal to the shutdown pin, or connecting it to the input pin, will turn the output ON. Pulling the shutdown pin to 0.3 V or below, or connecting it to ground, will turn the output OFF. In shutdown mode, the quiescent current is reduced to less than 1 μA.

Printed Circuit Board Layout Considerations

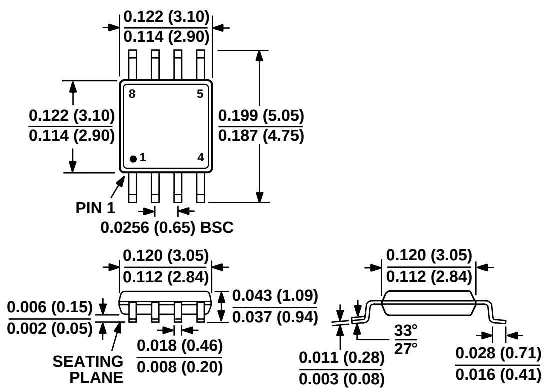
Use the following general guidelines when designing printed circuit boards:

1. Keep the output capacitor as close to the output and ground pins as possible.
2. Keep the input capacitor as close to the input and ground pins as possible.
3. PC board traces with larger cross sectional areas will remove more heat from the ADP3333. For optimum heat transfer, specify thick copper and use wide traces.
4. Connect the NC pins (Pins 5, 6, and 8) to ground for better thermal performance.
5. The thermal resistance can be decreased by approximately 10% by adding a few square centimeters of copper area to the lands connected to the pins of the LDO.
6. Use additional copper layers or planes to reduce the thermal resistance. Again, connecting the other layers to the ground and NC pins of the ADP3333 is best, but not necessary. When connecting the ground pad to other layers use multiple vias.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

8-Lead Mini/micro SOIC Package [Mini_SO] (RM-8)



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