BURR-BROWN®

ADS7870

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12-Bit ADC, MUX, PGA and Internal Reference DATA ACQUISITION SYSTEM

FEATURES

- 16-BIT DYNAMIC RANGE
- PGA GAINS: 1, 2, 4, 5, 8, 10, 16, 20V/V
- 4-CHANNEL DIFFERENTIAL/8-CHANNEL SINGLE ENDED MULTIPLEXER
- 2.048V OR 2.5V INTERNAL REFERENCE
- FAST SERIAL INTERFACE
- HIGH THROUGHPUT RATE: 52ksamples/s
- ERROR/OVERLOAD INDICATOR
- 2.7V TO 5.5V SINGLE-SUPPLY OPERATION
- 4-BIT DIGITAL I/O VIA SERIAL INTERFACE
- SSOP-28 PACKAGE

APPLICATIONS

- PORTABLE/BATTERY POWERED SYSTEMS
- LOW POWER INSTRUMENTATION
- LOW POWER CONTROL SYSTEMS
- SMART SENSOR APPLICATIONS

DESCRIPTION

The ADS7870[1] is a complete low-power data acquisition system on a single chip. It consists of a 4-channel differential/8-channel single-ended multiplexer, precision programmable gain amplifier, 12-bit successive approximation analog-to-digital converter and a precision voltage reference.

The programmable-gain amplifier provides high input impedance, excellent gain accuracy, good common-mode rejection, and low noise.

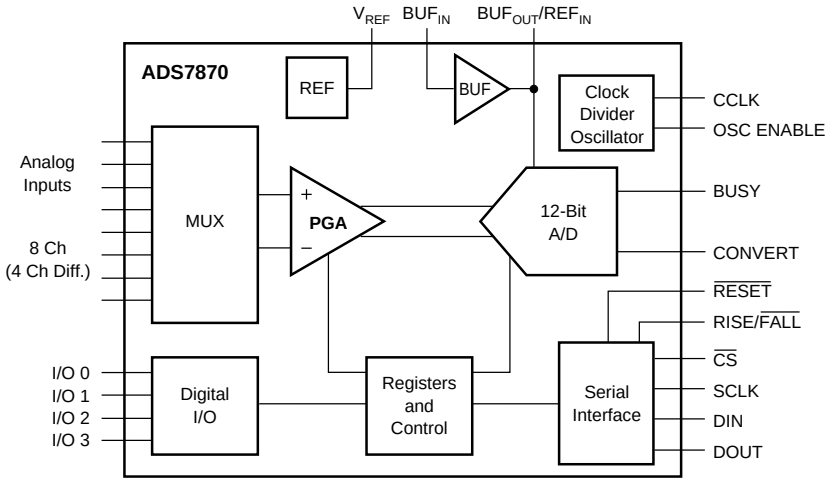
For many low-level signals, no external amplification or impedance buffering is needed between the signal source and the A/D input.

The offset voltage of the PGA is auto zeroed. Gains of 1, 2, 4, 5, 8, 10, 16 and 20V/V provide 16-bit dynamic range and allow signals as low as 125mV to produce full scale digital outputs.

The ADS7870 contains an internal reference, which is trimmed for high initial accuracy and stability vs temperature. Drift is typically 10ppm/°C. An external reference can be used in situations where multiple ADS7870s share a common reference.

The serial interface allows the use of SPI™, QSPI™, Microwire™, and 8051-family protocols, without glue logic.

NOTE: (1) Patent Pending.



International Airport Industrial Park • Mailing Address: PO Box 11400, Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd., Tucson, AZ 85706 • Tel: (520) 746-1111
Twx: 910-952-1111 • Internet: http://www.burr-brown.com/ • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

SPECIFICATIONS FOR THE TOTAL SYSTEM[1]

(See next section for specifications for each function in the ADS7870)
At T_A = +25°C, V_{DD} = +5.0V, V_{REF} = 2.5V connected to BUF_{IN} (using internal reference), 2.5MHz CCLK and 2.5MHz SCLK, unless otherwise noted.

PARAMETER	CONDITIONS	ADS7870EA MIN	ADS7870EA TYP	ADS7870EA MAX	UNITS
ANALOG INPUT CHARACTERISTICS					
Input Voltage Range (LNx inputs)	Linear Operation	–0.2		V_{DD} + 0.2	V
Input Capacitance[2]			4 to 9.7		pF
Input Impedance[2]					
Common-Mode			6		MΩ
Differential			7		MΩ
Channel-to-Channel Crosstalk	V_{IN} = 2Vp-p, 60Hz[3]		100		dB
Multiplexer Leakage Current			100		pA
STATIC ACCURACY					
Resolution			12		Bits
No Missing Codes	G = 1 to 20V/V	12			Bits
Integral Linearity Error	G = 1 to 20V/V		±1	±2.5	LSB
Differential Linearity Error	G = 1 to 20V/V		±0.5		LSB
Offset Error	G = 1 to 20V/V		±1	±6	LSB
Full Scale (Gain) Error					
Ratiometric Configuration or External Ref[4]	G = 1 to 10V/V			±0.2	%FSR
	G = 16 and 20V/V			±0.25	%FSR
Internal Reference	G = 1 to 10V/V			±0.35	%FSR
	G = 16 and 20V/V			±0.4	%FSR
DC Common-Mode Rejection, RTI	V_{IN} = –0.2V to 5.2V, G = 20 V/V	92			dB
Power Supply Rejection, RTI	V_{DD} = 5V ±10%, G = 20 V/V		86		dB
DYNAMIC CHARACTERISTICS					
Throughput Rate, Continuous Mode	One Channel			52	ksamp/s
Address Mode	Different Channels			52	ksamp/s
External Clock, CCLK[5]		0.100		20	MHz
Internal Oscillator Frequency			2.5		MHz
Serial Interface Clock (SCLK)				20	MHz
Data Set-Up Time		10			ns
Data Hold Time		10			ns
DIGITAL INPUTS					
Logic Levels					
Low Level Input Voltage, V_{IL}				0.8	V
High Level Input Voltage, V_{IH}	$V_{DD} \le 3.6V$	2			V
	$V_{DD} > 3.6V$	3			V
Low Level Input Current, I_{IL}				1	µA
High Level Input Current, I_{IH}				1	µA
DIGITAL OUTPUTS					
Data Coding	Binary Two's Complement				
V_{OL}	I_{SINK} = 5mA			0.4	V
	I_{SINK} = 16mA		0.8		V
V_{OH}	I_{SOURCE} = 0.5mA	V_{DD} – 0.4			V
	I_{SOURCE} = 5mA		4.6		V
I_{SOURCE} = 5mA, DOUT pin	High-Z State, V_{OUT} = 0V to V_{DD}			1	µA
Output Capacitance			5		pF
VOLTAGE REFERENCE					
BUF_{IN}					
Input Voltage Range	Input to Buffer Amplifier	0.9		V_{DD} – 0.2	V
Input Impedance			10^{12} || 3		Ω || pF
BUF_{OUT}/REF_{IN}[6, 7]					
Output Voltage Accuracy	V_{REF} = 2.048V and 2.5V		±0.05%	±0.25	%
vs Temperature	T_A= –40°C to 85°C		10	50	ppm/°C
Bandgap Voltage Reference			1.15		V
Short-Circuit Current			20		mA
POWER SUPPLY REQUIREMENTS					
Specified Voltage Range, V_{DD}			5		V
Operating Voltage Range		2.7		5.5	V
Power Supply Current[6]					
1kHz Sample Rate	REF and BUF On, Internal Oscillator on		0.450		mA
50kHz Sample Rate	REF and BUF On, External CCLK		1.2	1.7	mA
Power Down	REF and BUF Off			1	µA
Power Dissipation[6]					
1kHz Sample Rate	REF and BUF On, Internal Oscillator on		2.25		mW
50kHz Sample Rate	REF and BUF On, External CCLK		6	8.5	mW
Power Down	REF and BUF Off			5	µW
TEMPERATURE RANGE					
Specified Range		–40		+85	°C
Operating Range		–55		+125	°C
Storage Range		–65		+150	°C
Thermal Resistance, θ_{JA}			150		°C/W

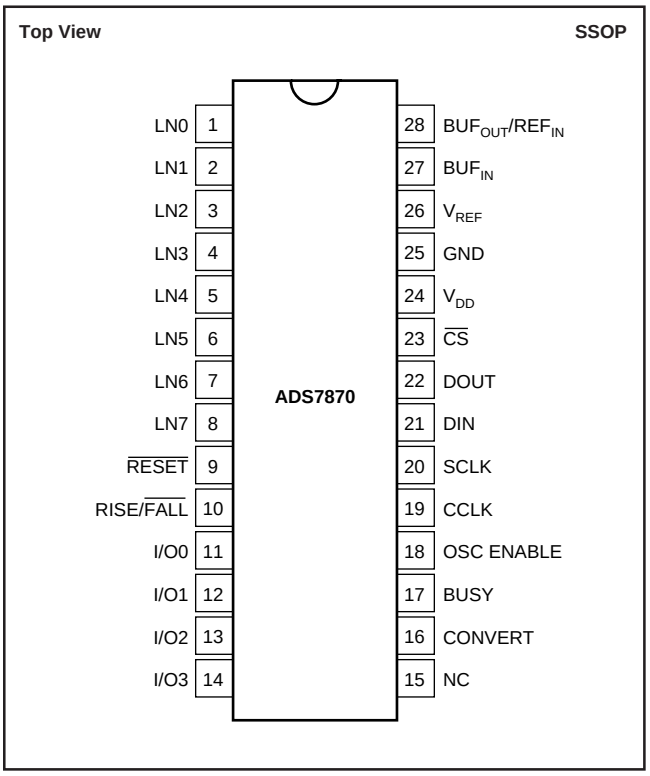
SPECIFICATIONS FOR INTERNAL FUNCTIONS[1]

(See previous section for the TOTAL DATA ACQUISITION SYSTEM)
At T_A = +25°C, V_{DD} = +5.0V, V_{REF} = 2.5V connected to BUF_{IN} (using internal reference), 2.5MHz CCLK and 2.5MHz SCLK, unless otherwise noted.

PARAMETER	CONDITIONS	ADS7870EA MIN	ADS7870EA TYP	ADS7870EA MAX	UNITS
MULTIPLEXER					
ON Resistance			500		Ω
OFF Resistance			1		GΩ
OFF Channel Leakage Current	V_{LNx} = 5.2V				
ON-Channel = 5.2V, OFF-Channel = 0V			100		pA
ON-Channel = 0V, OFF-Channel = 5.2V			100		pA
ON Channel Leakage Current	ON-Channel = 5.2V, OFF-Channel = 0V		100		pA
ON-Channel = 0V, OFF-Channel = 5.2V			100		pA
PGA AMPLIFIER					
Input Capacitance[2]			4 to 9.7		pF
Input Impedance[2]					
Common-Mode			6		MΩ
Differential			7		MΩ
Offset Voltage			100		µV
Small-Signal Bandwidth			5/Gain		MHz
Settling Time: 0.01%	G = 1		0.3		µs
	G = 20		6.4		µs
ANALOG-TO-DIGITAL CONVERTER					
DC CHARACTERISTICS					
Resolution			12		LSB
Integral Linearity Error			0.5		LSB
Differential Linearity Error			0.5		LSB
No Missing Codes			12		Bits
Offset Error	REF_{IN} = 2.5V		0.5		LSB
Full Scale (Gain) Error			0.02		%
Common-Mode Rejection, RTI of A/D			80		dB
Power Supply Rejection, RTI of ADS7870	External Reference, V_{DD} = 5V ±10%		60		dB
PGA plus A/D CONVERTER					
SAMPLING DYNAMICS	f_{CCLK} = 2.5 MHz, DF = 1				
Throughput Rate	48 CCLK cycles		52		kHz
Conversion Time	12 CCLK cycles		4.8		µs
Acquisition Time	28 CCLK cycles		9.6		µs
Auto Zero Time	8 CCLK cycles		3.2		µs
Aperture Delay	36 CCLK cycles		12.8		µs
Small Signal Bandwidth			5		MHz
Step Response			1 Complete Conversion Cycle		

NOTES:
(1) The SPECIFICATIONS FOR THE TOTAL SYSTEM are overall analog input-to-digital output specifications. The SPECIFICATIONS FOR INTERNAL FUNCTIONS indicate the performance of the individual functions in the ADS7870.
(2) The ADS7870 uses switched capacitor techniques for the programmable gain amplifier and A/D converter. A characteristic of such circuits is that the input capacitance at any selected LNx pin changes during the conversion cycle.
(3) One channel "on" with its inputs grounded. All other channels "off" with sinewave voltage applied to their inputs.
(4) Ratiometric configuration exists when the input source is configured such that changes in the reference cause corresponding changes in the input voltage. The same accuracy applies when a perfect external reference is used.
(5) The CCLK is divided by the DF value specified by the contents of register ADC CONTROL Register, bits D0 and D1 to produce DCLK. The maximum value of DCLK is 2.5MHz.
(6) REF and BUF contribute 190µA and 150µA (950µW and 750µW) respectively. At initial power-up the default condition for both REF and BUF functions is power off. They can be turned on under software control by writing a "1" to D3 and D2 of the REF/OSCILLATOR CONTROL Register.
(7) For V_{DD} < 3.0V, V_{REF} = 2.5V not usable.

PIN CONFIGURATION



ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ABSOLUTE MAXIMUM RATINGS(1)

Supply Voltage, V_{DD}	5.5V
Analog Inputs:	
Input Current, Momentary	100mA
Continuous	10mA
Input Voltage	V_{DD} + 0.5V to Gnd – 0.5V
Operating Temperature	–55°C to +125°C
Storage Temperature	–65°C to +150°C
Junction Temperature	+150°C
Lead Temperature (soldering, 10s)	+300°C

NOTE: (1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability.

PACKAGE/ORDERING INFORMATION

PRODUCT	PACKAGE	PACKAGE DRAWING NUMBER	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER(1)	TRANSPORT MEDIA
ADS7870EA	SSOP-28 Surface Mount	324	–40°C to +85°C	ADS7870EA	ADS7870EA	Rails
ADS7870EA	SSOP-28 Surface Mount	324	–40°C to +85°C	ADS7870EA	ADS7870EA/250	Tape and Reel
"	"	"	"	"	ADS7870EA/1K	Tape and Reel

NOTES: (1) Models with a slash (/) are available only in Tape and Reel in the quantities indicated (e.g., /1K indicates 1000 devices per reel). Ordering 1000 pieces of "ADS7870EA/1K" will get a single 1000-piece Tape and Reel. For detailed Tape and Reel mechanical information, refer to Appendix B of Burr-Brown IC Data Book.

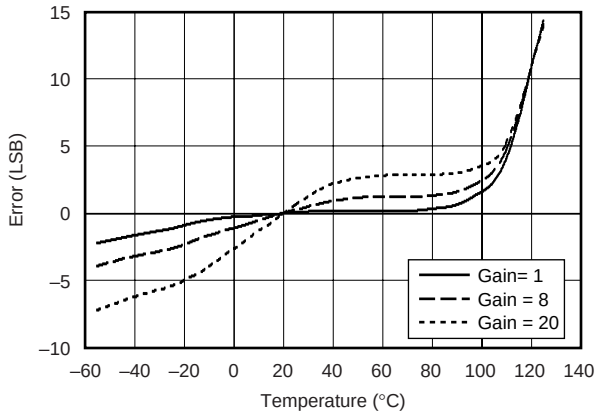
PIN ASSIGNMENTS

PIN #	NAME	I/O	DESCRIPTION
1	LN 0	Analog Input	MUX Input Line 0
2	LN 1	Analog Input	MUX Input Line 1
3	LN 2	Analog Input	MUX Input Line 2
4	LN 3	Analog Input	MUX Input Line 3
5	LN 4	Analog Input	MUX Input Line 4
6	LN 5	Analog Input	MUX Input Line 5
7	LN 6	Analog Input	MUX Input Line 6
8	LN 7	Analog Input	MUX Input Line 7
9	$\overline{\text{RESET}}$	Digital Input	Master Reset zero's all registers.
10	RISE/$\overline{\text{FALL}}$	Digital Input	Sets the active edge for SCLK. "0" sets SCLK active on falling edge. "1" sets SCLK active on rising edge.
11	I/O 0	Digital Input/Output	Digital Input or Output signal
12	I/O 1	Digital Input/Output	Digital Input or Output signal
13	I/O 2	Digital Input/Output	Digital Input or Output signal
14	I/O 3	Digital Input/Output	Digital Input or Output signal
15	NC	No Connection	Do not connect to this pin.
16	CONVERT	Digital Input	"0" to "1" transition starts a conversion cycle.
17	BUSY	Digital Output	"1" indicates converter is busy
18	OSC ENABLE	Digital Input	"0" sets CCLK as input, "1" sets CCLK as output and turns oscillator on.
19	CCLK	Digital Input/Output	If OSC ENABLE = "1" then Internal Oscillator is output to this pin. If OSC ENABLE = "0" then this is the input pin for an external conversion clock.
20	SCLK	Digital Input	Serial Data Input/Output Transfer Clock. Active edge set by the RISE/$\overline{\text{FALL}}$ pin. If RISE/$\overline{\text{FALL}}$ is low, SCLK is active on the falling edge.
21	DIN	Digital Input	Serial Data Input. In the 3-wire mode, this pin is used for serial data input. In the 2-wire mode serial data, output appears on this pin as well as the DOUT pin.
22	DOUT	Digital Output	Serial Data Output. This pin is driven when $\overline{\text{CS}}$ is low and is high impedance when $\overline{\text{CS}}$ is high. This pin behaves the same in both 3-wire and 2-wire modes.
23	$\overline{\text{CS}}$	Digital Input	Chip Select. When $\overline{\text{CS}}$ is low the serial interface is enabled. When $\overline{\text{CS}}$ is high the serial interface is disabled, the DOUT pin is high impedance, and the DIN pin is an input. The $\overline{\text{CS}}$ pin only effects the operation of the serial interface. It does not directly enable/disable the operation of the signal conversion process.
24	V_{DD}	Power	Power Supply Voltage, +2.7V to +5.5V.
25	GND	Power	Power Supply Ground.
26	V_{REF}	Analog Output	2.048V/2.5V On-Chip Voltage Reference
27	BUF_{IN}	Analog Input	Input to Reference Buffer Amplifier
28	BUF_{OUT}/REF_{IN}	Analog Output/Input	Output from Reference Buffer Amplifier and Reference Input to ADC.

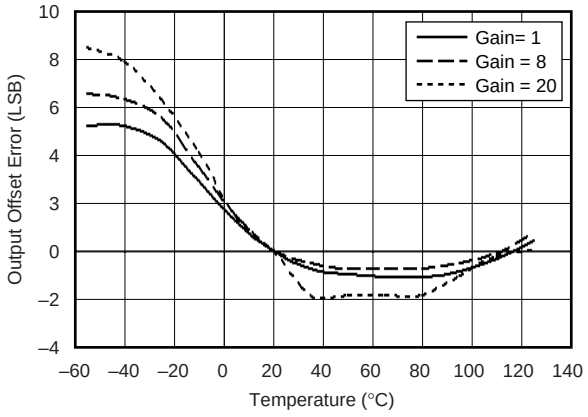
TYPICAL PERFORMANCE CURVES

At T_A = +25°C, V_{DD} = +5.0V, V_{REF} = 2.5V connected to BUF_{IN} (using internal reference), 2.5MHz CCLK and 2.5MHz SCLK, unless otherwise noted.

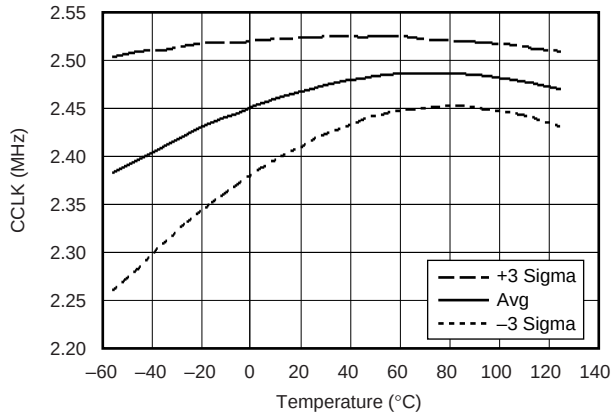
GAIN ERROR vs TEMPERATURE



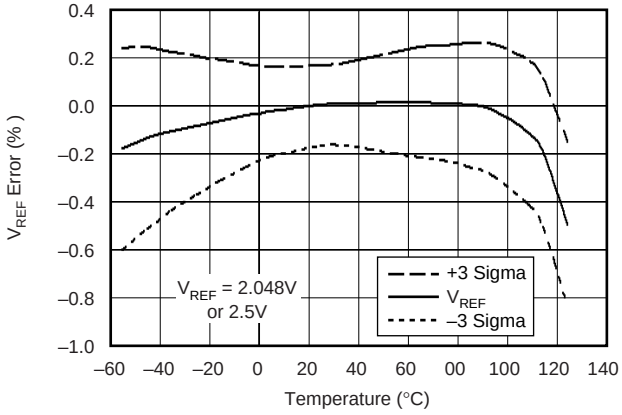
OUTPUT OFFSET ERROR vs TEMPERATURE



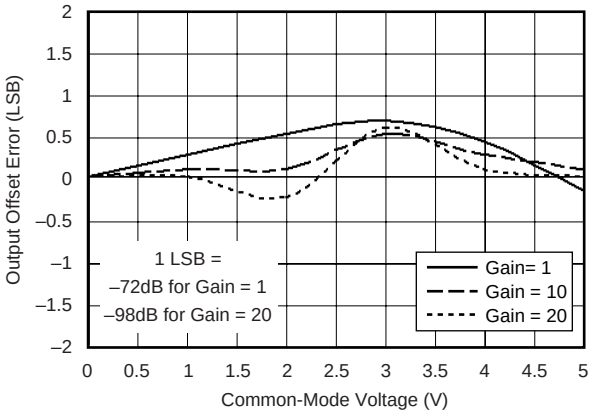
INTERNAL OSCILLATOR FREQUENCY vs TEMPERATURE



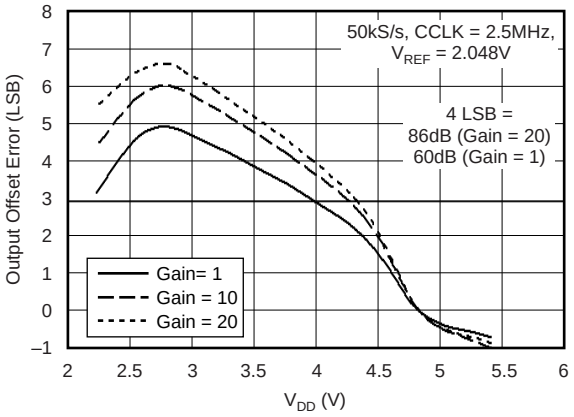
VOLTAGE REFERENCE ERROR vs TEMPERATURE



OUTPUT OFFSET ERROR vs COMMON-MODE VOLTAGE



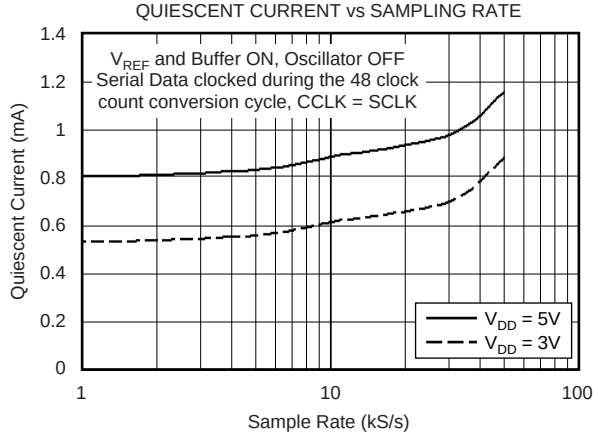
OUTPUT OFFSET ERROR vs POWER SUPPLY VOLTAGE



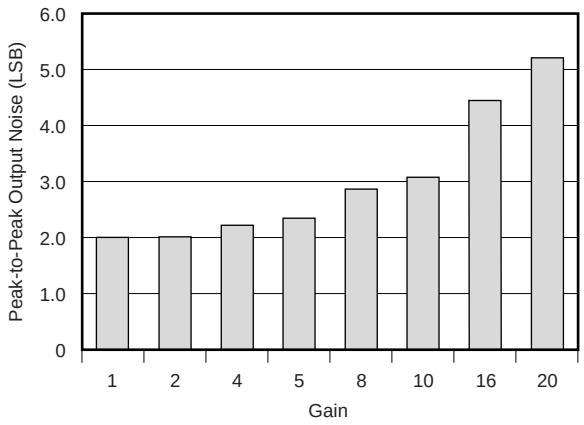
TYPICAL PERFORMANCE CURVES (cont.)

At T_A = +25°C, V_{DD} = +5.0V, V_{REF} = 2.5V connected to BUF_{IN} (using internal reference), 2.5MHz CCLK and 2.5MHz SCLK, unless otherwise noted.

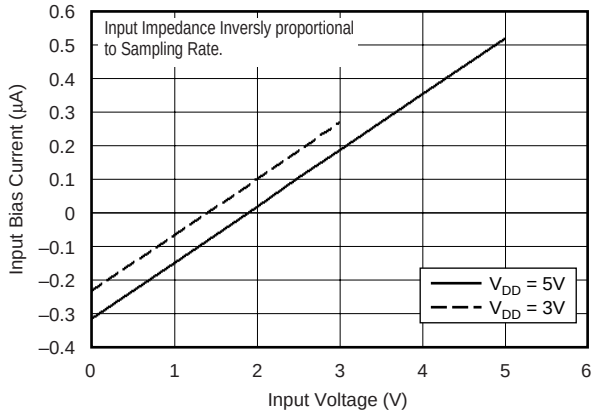
QUIESCENT CURRENT vs SAMPLING RATE



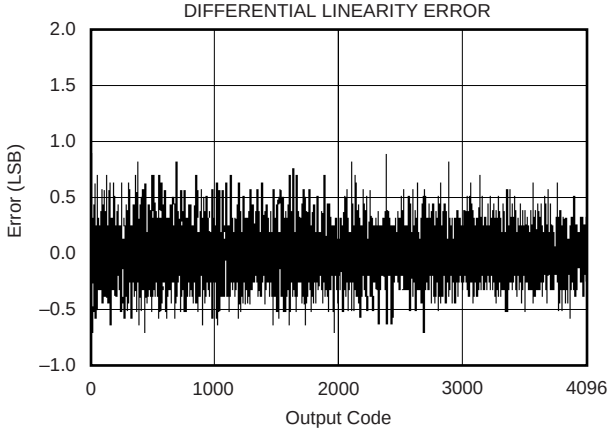
OUTPUT NOISE vs GAIN



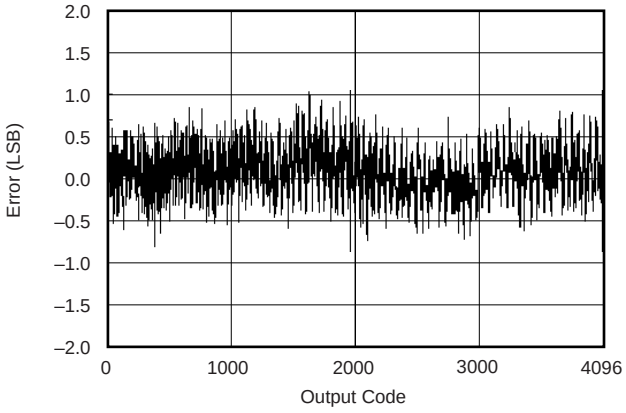
INPUT BIAS CURRENT vs INPUT VOLTAGE



DIFFERENTIAL LINEARITY ERROR



INTEGRAL LINEARITY ERROR



OVERVIEW

The ADS7870 is a complete data acquisition device composed of an input analog multiplexer (MUX), a programmable gain amplifier (PGA) and an analog-to-digital converter (A/D). Four lines of digital input/output (I/O) are also provided. Additional circuitry provides support functions including conversion clock, voltage reference, and serial interface for control and data retrieval.

Control and configuration of the ADS7870 is accomplished by command bytes written to internal registers through the serial port. Command register device control includes MUX channel selection, PGA gain, A/D start conversion command, and I/O line control. Command register configuration control includes internal voltage reference setting and oscillator control.

Operational modes and selected functions can be activated by digital inputs at corresponding pins. Pin settable configuration options include SCLK active-edge selection, master reset, and internal oscillator clock enable.

The ADS7870 has eight analog-signal input pins, LN0 through LN7. These pins are connected to a network of analog switches (the "MUX" block in Figure 1). The inputs can be configured as 8 single ended or 4 differential inputs.

The four general-purpose digital I/O pins (I/O3 through I/O0) can be made to function individually as either digital inputs or digital outputs. These pins give the user access to four digital I/O pins through the serial interface without having to run additional wires to the host controller.

The programmable gain amplifier (PGA) provides gains of 1, 2, 4, 5, 8, 10, 16, and 20V/V.

The 12-bit A/D converter in the ADS7870 is a successive approximation type. The output of the converter is 2's complement format and can be read MSB first or LSB first.

The ADS7870's internal voltage reference can be software configured for output voltages of 1.15V, 2.048V or 2.5V. The reference circuit is trimmed for high initial accuracy and low temperature drift. A separate buffer amplifier is provided to buffer the high impednace V_{REF} output.

The voltage reference, PGA, and A/D converter use the conversion clock (CCLK) and signals derived from it. CCLK can be either an input or output signal. The ADS7870 can divide the CCLK signal by a constant before it is applied to the A/D converter or PGA. This allows a higher frequency system clock to be used to control the A/D converter operation. Division factors (DF) of 1, 2, 4 and 8 are available. The signal that is actually applied to the PGA and A/D converter is DCLK, where DCLK = CCLK/DF.

The ADS7870 is designed so that its serial interface can be conveniently used with a wide variety of micro-controllers. It has four conventional serial interface pins: SCLK (serial data clock), DOUT (serial data out), DIN (serial data in, which may be set bi-directional in some applications), and $\overline{CS}$ (chip select function).

The ADS7870 has ten internal user accessible registers which are used in normal operation to configure and control the device (see Table II, Register Address Map).

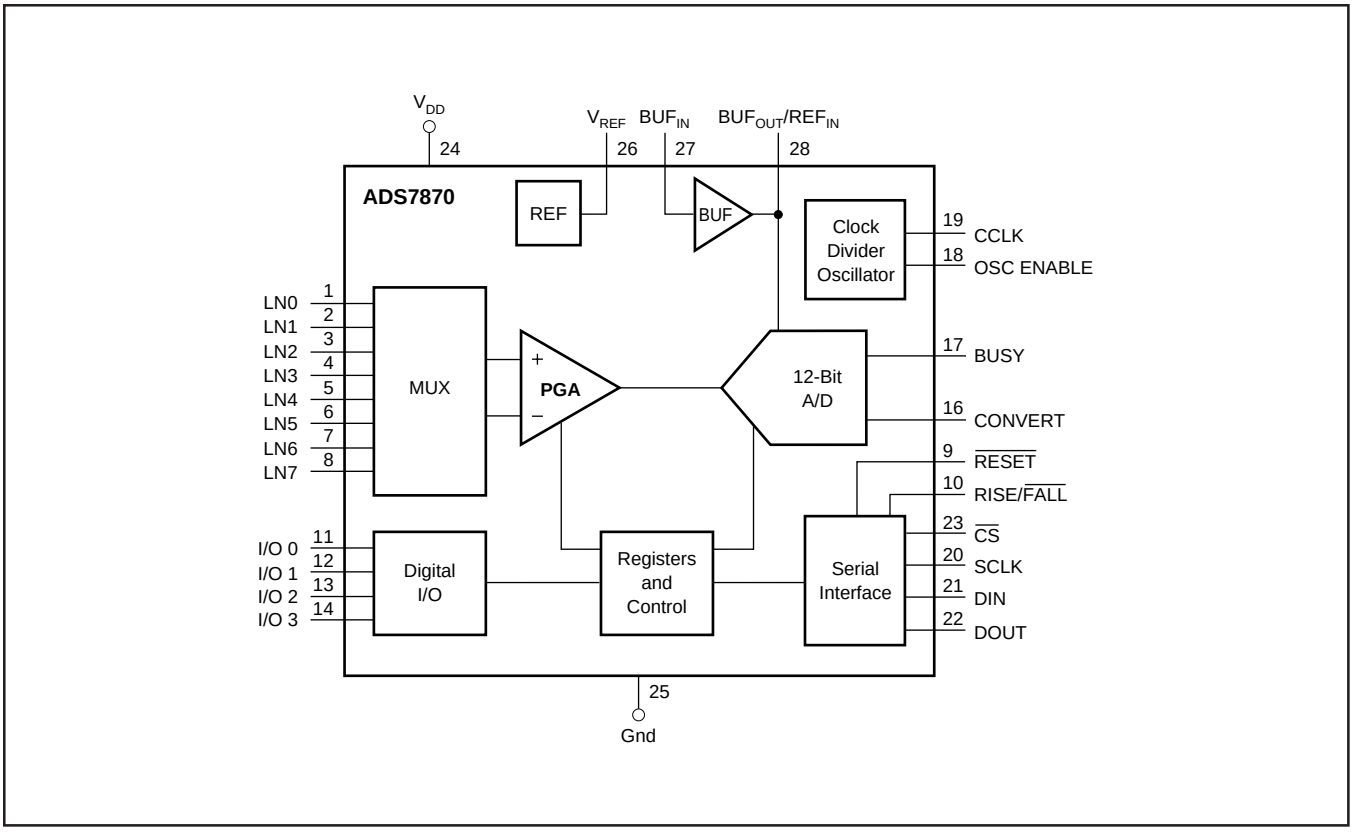


FIGURE 1. Basic Circuit Diagram.

FUNCTIONAL DESCRIPTION

MULTIPLEXER

The ADS7870 has eight analog-signal input pins, LN0 through LN7. These pins are connected to a network of analog switches (the "MUX" block in Figure 1). The switches are controlled by four bits in the Gain/Mux register.

LN0 through LN7 can be configured as 8 single ended inputs or 4 differential inputs. Some mux combination examples are shown in Figure 7. The differential polarity of the input pins can be changed with the M2 bit in the MUX address. This feature allows reversing the polarity of the conversion result without having to physically reverse the input connections to the ADS7870.

For linear operation, the input signal at any of the LN0 through LN7 pins can range between GND – 0.2V and V_{DD} + 0.2V. The polarity of the differential signal can be changed through commands written to Gain/Mux register, but each line must remain within the linear input common mode voltage range as described below.

Inputs LN0 through LN7 have ESD protection circuitry as the first active elements on the chip. These contain protection diodes connected to V_{DD} and GND that remain reverse biased under normal operation. If input voltages are expected beyond the absolute maximum voltage range it is necessary to add resistance in series with the input to limit the current to 10mA or less.

CONVERSION CLOCK

The conversion clock (CCLK) and signals derived from it are used by the voltage reference, the PGA, and the A/D converter. The PGA and the A/D use the same clock signal. These clocks are associated with the OSC ENABLE and CCLK pins as well as the OSCE and OSCR bits in the Ref/Oscillator Configuration Register (register 7). CCLK can be either an input pin or an output pin. When the OSC ENABLE pin is low (OSC ENABLE = "0"), the CCLK pin is an input and the ADS7870 uses an applied external clock for the conversion process. When OSC ENABLE = "1", the ADS7870 uses an internal 2.5MHz oscillator as the conversion clock. This clock signal appears as an output on the CCLK pin.

The ADS7870 can be programmed to divide the CCLK before it is applied to the A/D converter and PGA. This allows a higher frequency system clock, such as the SCLK, to be used synchronously to control the A/D converter operation. The frequency division constant is controlled by 2 bits (CDF1 and CDF0) in the ADC Control Register. Division factors (DF) of 1, 2, 4, and 8 are available. The signal that is actually applied to the PGA and A/D is DCLK, where DCLK = CCLK/DF.

The CCLK pin can be made either an input or an output and is convenient in situations where several ADS7870s are used in the same application. One ADS7870 can be made the conversion clock master (CCLK made an output) and all the other ADS7870s can be slaved to it (their pins made inputs). This can potentially reduce A/D conversion errors caused by clock and other systems noise.

The ADS7870 has both maximum and minimum DCLK frequency constraints (DCLK = CCLK/DF). The maximum DCLK is 2.5MHz. The minimum DCLK frequency applied to the PGA, reference and A/D is 100kHz.

VOLTAGE REFERENCE AND BUFFER AMPLIFIER

The internally generated V_{REF} of the ADS7870 is based on a band-gap voltage reference. The ADS7870 uses a unique (patent pending) switched capacitor implementation of the band-gap reference. The circuit has curvature correction for V_{REF} drift. The reference may be software configured for output voltages of 1.15V, 2.048V or 2.5V.

The amplifier inside the reference circuit has very limited output current capability. A separate buffer amplifier must be used to supply any load current. The internal buffer amplifier can supply typically up to 20mA and sink up to 20µA. The temperature compensation of the onboard reference is adjusted with the reference buffer in the circuit. Performance is specified in this configuration.

PROGRAMMABLE GAIN AMPLIFIER

The programmable gain amplifier (PGA) provides gains of 1, 2, 4, 5, 8, 10, 16, and 20V/V. The PGA is a single supply, rail-to-rail input, auto-zeroed, capacitor based instrumentation amplifier. PGA gain is set by bits G2 through G0 of Register 4.

Register 2 is a read only register that is used to report any out of range conditions at the PGA input or output during the convert cycle. The logical "OR" of these signals is available as the least significant bit of the A/D output register 0. Testing bit D0 of the A/D output register will indicate out of range conditions as described in the section which details the register contents.

A/D CONVERTER

The 12-bit A/D converter in the ADS7870 is a successive approximation type. The output of the converter is 2's complement format and can be read through the serial interface MSB first or LSB first. A plot of Output Codes vs Input Voltage is shown in Figure 2. With the input multiplexer configured for differential input the A/D output codes range from –2048 for $V_{IN} = -V_{REF}/G$ to 2047 for $V_{IN} = (+V_{REF} - 1V_{LSB})/G$. With the input multiplexer configured for single-ended inputs the A/D output codes range from 0 to 2047 for V_{IN} = 0 to $(+V_{REF} - 1V_{LSB})/G$.

CONVERSION CYCLE

A conversion cycle requires 48 DCLK cycles (DCLK = CCLK/DF). These signals are described in the Conversion Clock section that follows.

Operation of the PGA requires 36 DCLK cycles. During the PGA portion, the common mode voltage of the input source

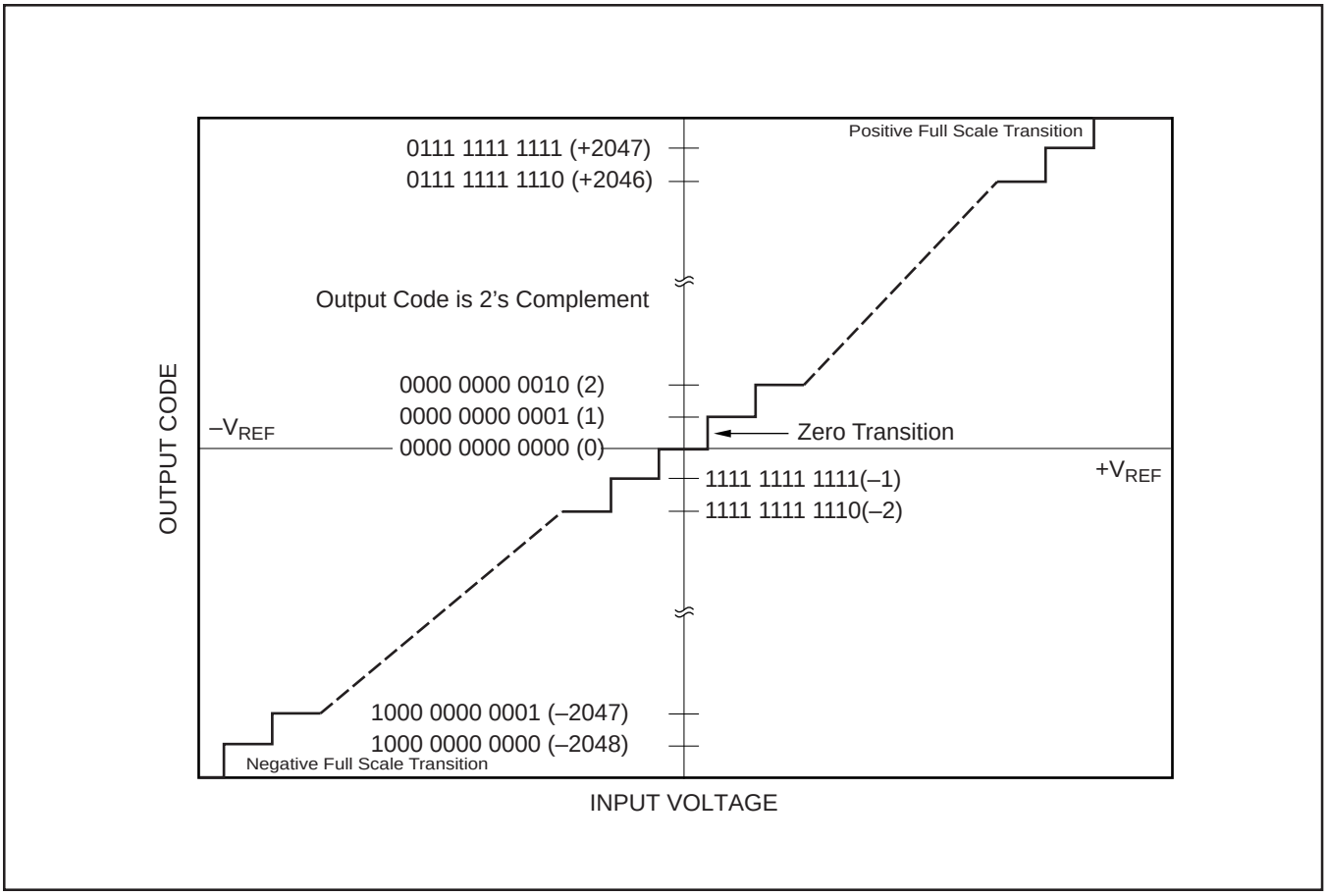


FIGURE 2. Output Codes versus Input Voltage.

is captured, the offset voltage of the PGA is auto-zeroed, and the signal is amplified. The PGA is allowed to settle to the 0.01% accuracy necessary for 12-bit, 1/2 LSB accuracy. The successive approximation conversion of the A/D converter takes the last 12 DCLK cycles.

During this clock sequence the input capacitance associated with a selected channel changes from 6pF to 9.7pF, to 6pF, to 7pF and finally to 6pF. When the ADS7870 is not converting, a channel provides a load capacitance of 4pF.

This changing of the capacitive load at a LNx pin can cause the voltage at the pin to vary on the DCLK transitions when the internal capacitors are switched in and out of the circuit. At the clock speeds associated with the ADS7870, the input pin voltages settle to final value quickly enough that the transitions are of no significance to the A/D conversion result.

Starting an A/D Conversion Cycle

There are four ways to cause the ADS7870 to perform a conversion:

1) Send a Direct Mode instruction.

2) Write to Register 4 with the CNV bit = "1".

3) Write to Register 5 with the CNV bit = "1".

4) Assert the CONVERT pin (Logic high.)

SERIAL INTERFACE

The ADS7870 communicates with microprocessors and other external circuitry through a digital serial port interface. It is compatible with a wide variety of popular micro-controllers, including Motorola 68HC11, Intel 80C51, and MicroChip PIC Series.

The serial interface consists of four primary pins, SCLK (serial bit clock), DIN (serial data input), DOUT (serial data output) and $\overline{CS}$ (chip select). SCLK synchronizes the data transfer with each bit being transmitted on the falling or rising SCLK edge as determined by the RISE/$\overline{FALL}$ pin. SDIN may also be used as a serial data output line.

Additional pins expand the versatility of the basic serial interface and allow it to be used with different micro-controllers. The RISE/$\overline{FALL}$ pin configures the ADS7870 to respond to either the rising or falling edge of SCLK for transferring serial data. The BUSY pin indicates when a conversion is in progress and may be used to generate interrupts for the micro-controller. The CONVERT pin can be used as a hardware means of causing the ADS7870 to start a conversion cycle. The $\overline{RESET}$ pin can be toggled in order to reset the ADS7870 to the power-on state. Four general purpose digital I/O pins (I/O3-I/O0) are also provided.

The ADS7870 is controlled by commands written to the serial interface as shown in Table I. This eight-bit word defines either the *direct* mode or *register* mode (see operating mode text).

Communication through the serial interface is dependent on the micro-controller providing an instruction byte followed by either additional data (for a write operation) or additional clocks to allow the ADS7870 to provide data (for a read operation). Special operating modes for reducing the instruction byte overhead for retrieving conversion results are provided.

Reset of device ($\overline{\text{RESET}}$), start of conversion (CONVERT), and oscillator enable (OSC ENABLE) can be done by signals to external pins or entries to internal registers. The actual execution of each of these commands is a logical OR function; either pin or register signal TRUE cause the function to execute. The CONVERT pin signal is an edge-triggered event, with a hold time of two DCLK periods for de-bounce.

OPERATING MODES

The ADS7870 serial interface operates based on an instruction byte followed by an action commanded by the contents of that instruction. The 8-bit instruction word is clocked into the DIN input. There are two types of instruction bytes that may be written to the ADS7870 as determined by Bit D7 of the instruction word (see Table I). These two instructions represent two different operating modes. In direct mode (Bit D7 = 1), a conversion is started. A register mode (Bit D7 = 0) instruction is followed by a Read or Write Operation to the specified register.

Direct Mode

In the direct mode a conversion is initiated by writing a single 8-bit instruction byte to the ADS7870 (Bit D7 is set to "1"). Writing the direct mode command sets the configuration of the multiplexer, selects the gain of the PGA, and starts a conversion cycle. After the last bit of the instruction byte is received, the ADS7870 performs a conversion on the selected input channel with the PGA gain set as indicated in the instruction byte.

The conversion cycle will begin on the second falling edge of CCLK after the eighth active edge of SCLK of the instruction byte. When the conversion is complete the conversion result will be stored in the A/D Output registers and is available to be clocked out of the serial interface by the controlling device using the READ operation in the Register Mode.

INSTRUCTION BYTE

	D7 (MSB)	D6	D5	D4	D3	D2	D1	D0
Start Conversion (Direct Mode)	1	G2	G1	G0	M3	M2	M1	M0
				OR				
Read/Write (Register Mode)	0	R/$\overline{\text{W}}$	16/$\overline{\text{8}}$	AS4	AS3	AS2	AS1	AS0

START CONVERSION INSTRUCTION BYTE (Direct Mode)(1)

BIT	SYMBOL	NAME	VALUE	FUNCTION
D7		Mode Select	1	Starts a Conversion Cycle (Direct Mode)
D6-D4	G2-G0	PGA Gain Select	000 001 010 011 100 101 110 111	PGA Gain = 1 (power up default condition) PGA Gain = 2 PGA Gain = 4 PGA Gain = 5 PGA Gain = 8 PGA Gain = 10 PGA Gain = 16 PGA Gain = 20
D3-D0	M3-M0	Input Channel Select	See Table III	Determines input channel selection for the requested conversion, differential or single-ended configuration.

NOTE: (1) The seven lower bits of this byte are also written to register 4, the Gain/Mux register.

READ / WRITE INSTRUCTION BYTE (Register Mode)

BIT	SYMBOL	NAME	VALUE	FUNCTION
D7		Mode Select	0	Initiates a read or write operation (Register Mode)
D6	R/$\overline{\text{W}}$	Read/Write Select	0 1	Write Operation Read Operation
D5	16/$\overline{\text{8}}$	Word Length	0 1	8-Bit Word 16-Bit Word (2 eight-bit bytes)
D4-D0	AS4-AS0	Register Address	See Table II	Determines the address of the register that is to be read from or written to.

TABLE I. Instruction Byte Addressing.

The structure of the instruction byte for direct mode is shown in Table I.

- D7: This bit is set to "1" for direct mode operation
- D6 through D4 (G2-G0): These bits control the gain of the programmable gain amplifier. PGA gains of 1, 2, 4, 5, 8, 10, 16 and 20 are available. The coding is shown in Table I.
- D3 through D0 (M3-M0): These bits configure the switches that determine the input channel selection. The input channels may be placed in either differential or single ended configurations. In the case of differential configuration, the polarity of the input signal is reversible. The coding is shown in Table III.

Note that the seven lower bits of this byte are written to register 4, the Gain/Mux register.

All other controllable ADS7870 parameters are values previously stored in their respective registers. These values are either the power-up default values or values that were previously written to one of the control registers in an Register mode operation. No additional data is required for a direct mode instruction.

Register Mode

In register mode (Bit D7 of the Instruction Byte is "0") a read or write instruction to one of the ADS7870's registers is initiated. All of the user determinable functions and features of the ADS7870 can be controlled by writing information to these registers (see Table II). Conversion results can be read from the A/D Output registers.

The Instruction Byte (see Table I) contains the address of the register for the next read/write operation, determines whether the serial communication is to be done in 8-bit or 16-bit word length, and determines whether next operation will read-from or write-to the addressed register.

The structure of the instruction byte for register mode is shown in Table I.

- D7: This bit is set to "0" for "register" mode operation.
- D6 (R/$\overline{W}$): Bit 6 of the Instruction Byte determines whether a read or write operation is performed, "1" for a read or "0" for a write.
- D5 (16/$\overline{8}$): This bit determines the word length of the read or write operation that follows, "1" for sixteen bits (two eight-bit bytes) or "0" for eight bits.
- D4 through D0 (AS4-AS0): These bits determine the address of the register that is to be read-from or written-to. See Table II for register address coding and other information.

For sixteen-bit operations, the first eight bits will be written-to/read-from the address encoded by instruction byte, bits AS4 through AS0 (Register Address). The address of the next eight bits depends on whether the Register Address for the first byte is odd or even. If it is even, then the address for the second byte will be Register Address + 1. If the Register Address is odd, then the address for the second byte is the Register Address – 1.

This arrangement allows transfer of conversion results from the two A/D Output Data registers either MS byte first or LS byte first (see Serial Interface Control Register text).

Register Summary

A summary of information about the ADS7870 addressable registers is shown in Table II. Brief descriptions of the ten user-addressable registers follow. More detailed information on the individual registers is provided in the INTERNAL USER-ACCESSIBLE REGISTERS section.

Registers 0 and 1, the A/D output data registers, contain the least significant and most significant bits (ADC0 through ADC11) of the A/D conversion result. Register 0 also contains a bit that indicates if the allowable internal voltage limits for the PGA have been exceeded (OVR).

Register 2, the PGA Valid Register, contains information that describes the nature of the problem in the event that the allowable input voltage to the PGA has been exceeded.

Register 3, the A/D Control Register, contains information regarding the serial interface; a frequency division factor used for the conversion clock function (CDF0 and CDF1) and configuration control of an automatic read back option (RBM0 and RBM1).

Register 4, the Gain/Mux Register, contains the input channel selection information (M0 through M3) and the programmable gain amplifier gain set bits (G0 through G2).

Register 5, the Digital I/O State Register, contains the state of each of the digital I/O pins (I/O3 through I/O0).

REGISTER ADDRESS					ADDR	READ/	REGISTER ADDRESS								REGISTER
AS4	AS3	AS2	AS1	AS0	N0.	WRITE	D7(MSB)	D6	D5	D4	D3	D2	D1	D0	NAME
0	0	0	0	0	0	Read	ADC3	ADC2	ADC1	ADC0	0	0	0	OVR	A/D Output Data, LS Byte
0	0	0	0	1	1	Read	ADC11	ADC10	ADC9	ADC8	ADC7	ADC6	ADC5	ADC4	A/D Output Data, MS Byte
0	0	0	1	0	2	Read	0	0	VLD5	VLD4	VLD3	VLD2	VLD1	VLD0	PGA Valid Register
0	0	0	1	1	3	R/W	0	0	0	0	RBM1	RBM0	CFD1	CFD0	A/D Control Register
0	0	1	0	0	4	R/W	CNV/BSY	G2	G1	G0	M3	M2	M1	M0	Gain/Mux Register
0	0	1	0	1	5	R/W	CNV/BSY	0	0	0	IO3	IO2	IO1	IO0	Digital I/O State Register
0	0	1	1	0	6	R/W	0	0	0	0	OE3	OE2	OE1	OE0	Digital I/O Control Register
0	0	1	1	1	7	R/W	0	0	OSCR	OSCE	REFE	BUFE	R2V	RGB	Ref/Oscillator Control Register
1	1	0	0	0	24	R/W	LSB	2W/3	8051	0	0	8501	2W/3	LSB	Serial Interface Control
1	1	1	1	1	31	Read	0	0	0	0	0	0	0	1	ID Register

TABLE II. Register Address Map.

In addition, registers 4 and 5 contain a convert/busy bit (CNV/BSY) that can be used to start a conversion via a write instruction or sense when the converter is busy with a read instruction.

Register 6, the Digital I/O Control Register, contains the information that determines whether each of the four digital I/O pins is to be an input or an output function (OE3 through OE0). This sets the mode of each I/O pin.

Register 7, the Ref/Oscillator Control Register, controls whether the internal oscillator used for the conversion clock is on or off (OSCE), whether the internal voltage reference and buffer are on or off (REFE, BUFE), and whether the reference provides 2.5V, 2.048V, or 1.15V.

Register 24, the Serial Interface Control Register, controls whether data is presented MSB or LSB first (LSB bit), whether the serial interface is configured for 2-wire or 3-wire operation (2W bit), and determines proper timing control for 8051-type microprocessor interfaces (8051 bit).

Reset

In the event that system synchronization is lost between the ADS7870 and its controller there are three ways to reset.

The entire register contents as well as the serial interface are reset on:

1) Cycle power. The power down time must be long enough to allow internal nodes to discharge.
2) Toggle the RESET pin. Minimum pulse width to reset is 50 ns.
3) Write an 8-bit byte of all zeros to register 0.

All of these actions set all internal registers to zero. This turns off the oscillator and reference. Recovery time is dependent on the size of the filter capacitor in the reference output.

If the serial interface is synchronized and waiting for an instruction then eight cycles of the SCLK with DIN zero followed by a single "1" will reset the device. The next active edge of SCLK following the "1" is the first bit of the next instruction. Cycling $\overline{CS}$ will assure that the serial interface is reset.

The serial interface is resynchronized every time the $\overline{CS}$ signal is "1". For this reason it is mandatory that $\overline{CS}$ be held low throughout any communication sequence with the ADS7870. This synchronization does not change any of the register values.

For those instances where $\overline{CS}$ cannot be cycled it is necessary to write thirty-nine "0"s followed by a "1". This string length is based on the worst case conditions to ensure that the device is synchronized.

WRITE OPERATION

To perform a write operation an instruction byte must first be written to the ADS7870 as described previously (see Table I). This instruction will determine the target register as well as the word length (8 bits or 16 bits). The $\overline{CS}$ pin must be asserted ("0") prior to the first active SCLK edge (rising or falling depending on the state of the RISE/$\overline{FALL}$ pin) that will latch the first bit of the instruction byte. The first active edge after $\overline{CS}$ must have the first bit of the instruction byte. The remaining seven bits of the instruction byte will be latched on the next seven active edges of SCLK. $\overline{CS}$ must remain low for the entire sequence. Setting $\overline{CS}$ high will resynchronize the serial interface.

When starting a conversion by setting the CNV/BSY bit in the Gain/Mux register and/or the Digital I/O register, the conversion will start on the second falling edge of CCLK after the last active SCLK edge of the write operation.

Figure 3 shows an example of an eight-bit write operation with LSB first and SCLK active on the rising edge. The double arrows indicate the SCLK transition when data is latched into its destination register. Figure 4 shows an example of the timing for a 16-bit write to an even address with LSB first and SCLK active on the rising edge. Notice that both bytes are updated to their respective registers simultaneously. Also shown is that the address (ADDR) for the write of the second byte is incremented by one since the ADDR in the instruction byte was even. For an odd ADDR, the address for the second byte would be ADDR-1.

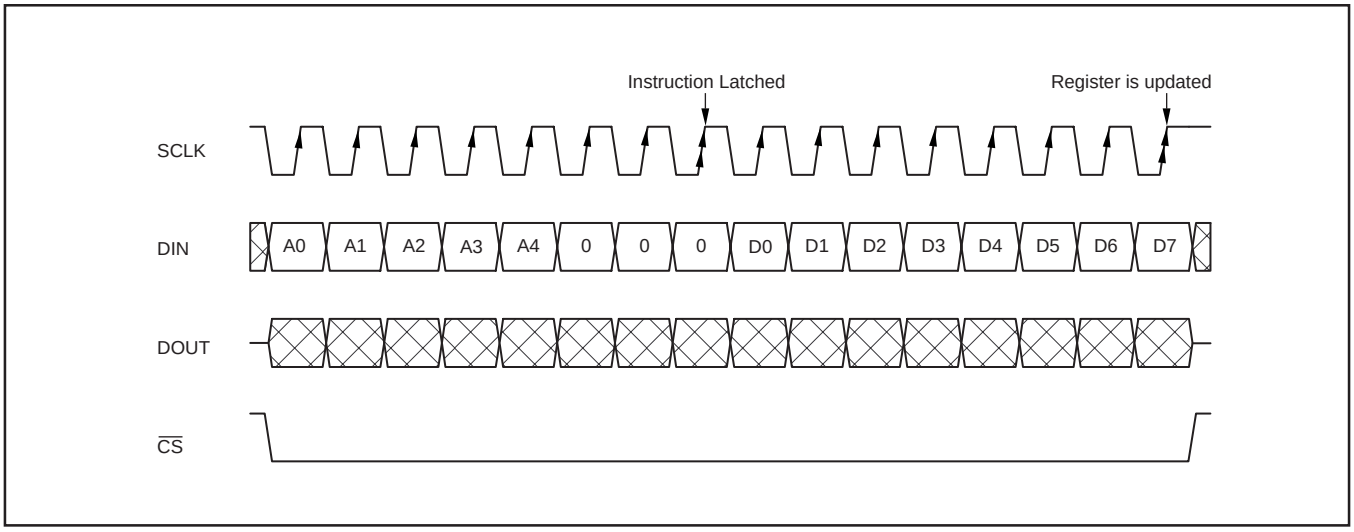


FIGURE 3. Example Timing Diagram for an 8-Bit Write Operation.

READ OPERATION

A read operation is similar to a write operation except that data flow (after the instruction byte) is from the ADS7870 to the host controller. After the instruction byte has been latched (on the eighth active edge of SCLK) the DOUT pin (and the DIN pin if in two-wire mode) will begin driving data on the next non-active edge of SCLK. This allows the host controller to have valid data on the next active edge of SCLK.

The data on DOUT (or DIN) will transition on non-active edges of SCLK. The DIN pin (two-wire mode) will cease driving data (return to high impedance) on the non-active edge of SCLK following the eighth (or sixteenth) active edge of the read data. DOUT is only high impedance when $\overline{CS}$ is not asserted. With $\overline{CS}$ high ("1"), DOUT (or DIN) is forced to high impedance mode. In general, the ADS7870 is insensitive to the idle state of the clock except that the state of SCLK may determine if the DIN is driving data or not.

Upon completion of the read operation, the ADS7870 will be ready to receive the next instruction byte. Read operations will reflect the state of the ADS7870 on the first active edge of SCLK of the data byte transferred.

Figure 5 shows an example of an eight-bit read operation with LSB first and SCLK active on the rising edge. The double rising arrows indicate when the instruction is latched. The first bit of data is sampled on the first active SCLK edge of the read portion of the instruction. The remaining bits are sampled on the next inactive SCLK edge.

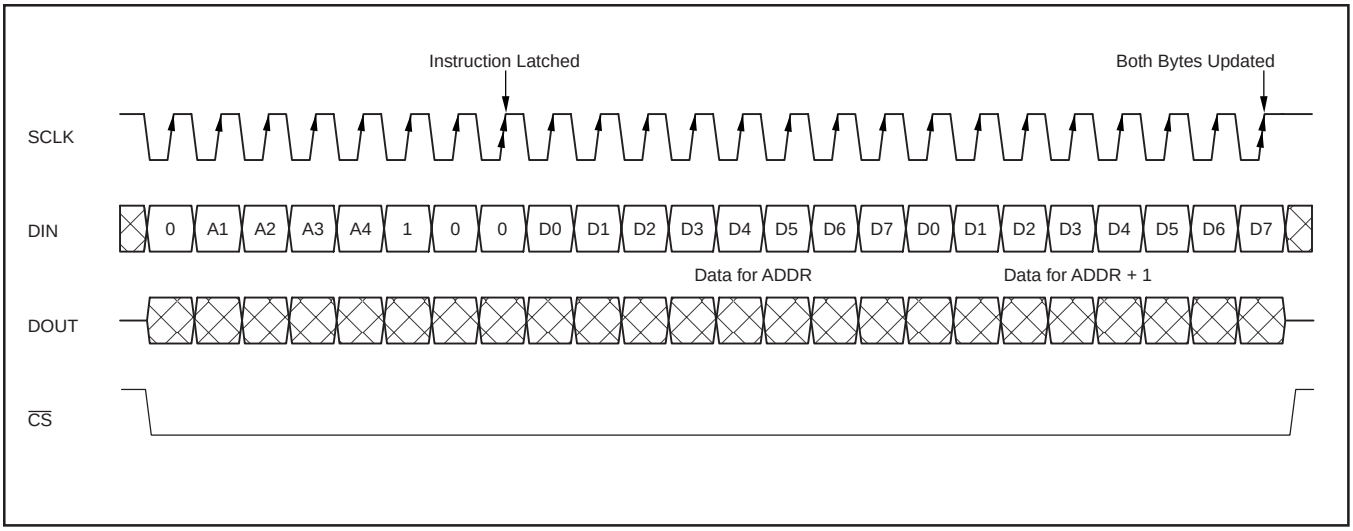


FIGURE 4. Example Timing Diagram for a 16-Bit Write Operation to an Even Address.

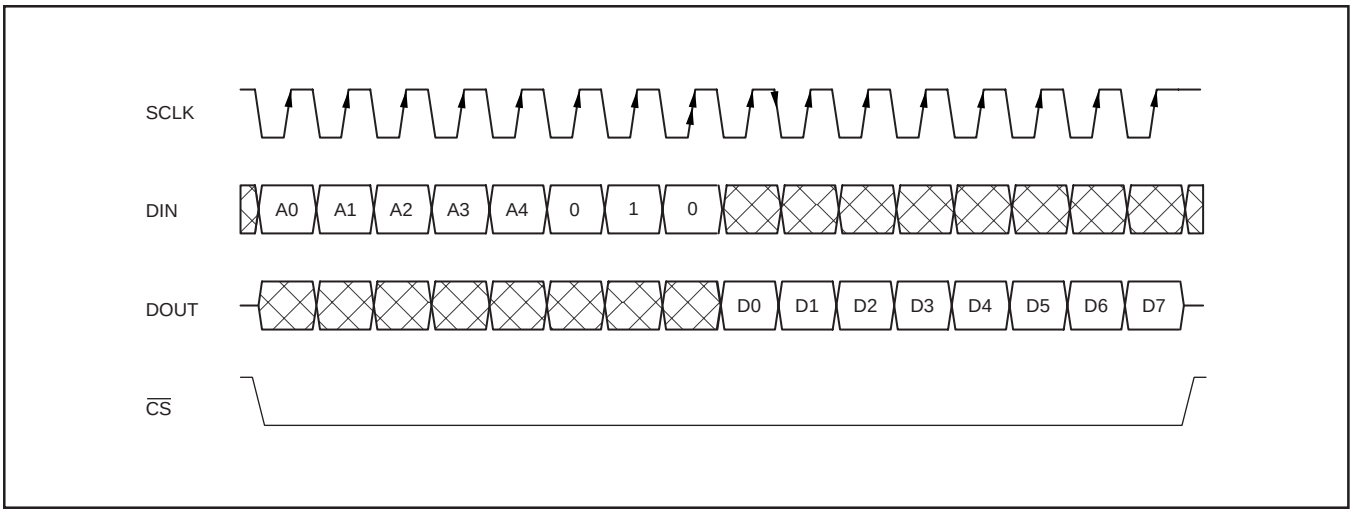


FIGURE 5. Example Timing Diagram for an 8-Bit Read Operation.

Figure 6 provides an example of a 16-bit read operation from an odd address with LSB first and SCLK active on the rising edge. The address (ADDR) for the second byte is decremented by one since the ADDR in the instruction byte is odd. For an even ADDR, the address for the second byte would be incremented by one.

MULITPLEXER ADDRESSING

The last four bits in the Instruction Byte (during a start conversion instruction) or the Gain/Mux Register (ADDR = 4) assign the mulitplexer configuration for the requested conversion. The input channels may be placed in either differential or single-ended configurations. For differential configurations, the polarity of the input signal is reversible by the state of M2 (Bit D2). In single-ended mode, all input channels are measured with respect to system ground. Figure 7 shows some examples of mulitplexer assignments and Table III provides the coding for the input channel selection.

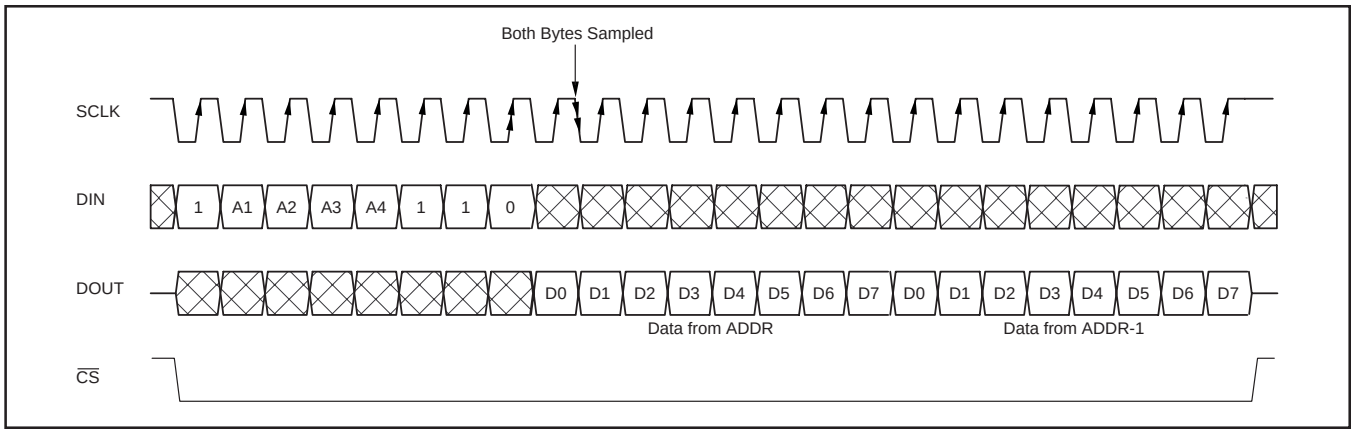


FIGURE 6. Example Timing Diagram for a 16-Bit Read from an Odd Address.

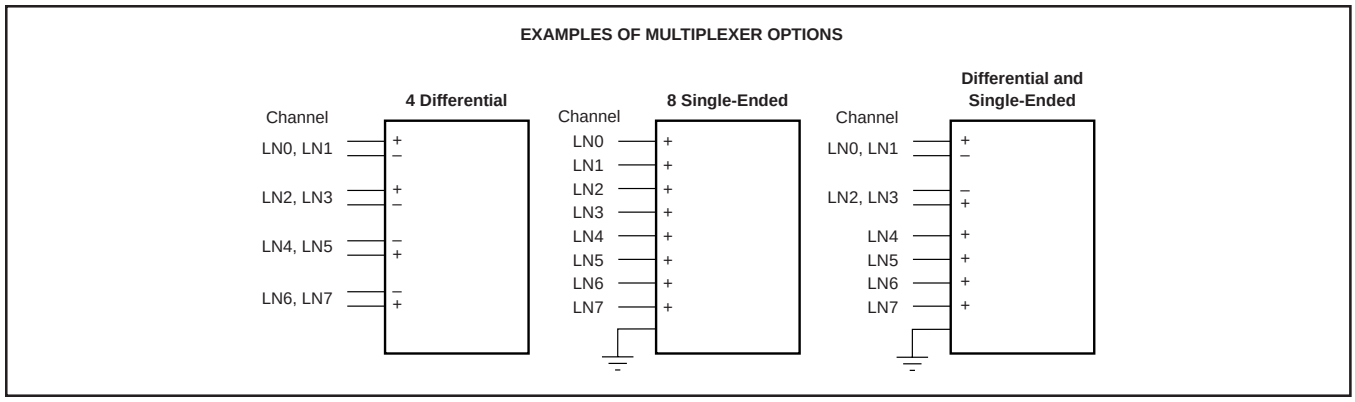


FIGURE 7. Examples of Multiplexer Options.

CODING FOR DIFFERENTIAL INPUT CHANNEL SELECT

SELECTION BITS				INPUT LINES							
M3	M2	M1	M0	LN0	LN1	LN2	LN3	LN4	LN5	LN6	LN7
0	**0**	**0**	**0**	**+**	**–**						
0	0	0	1			+	–				
0	0	1	0					+	–		
0	0	1	1							+	–
0	1	0	0	–	+						
0	1	0	1			–	+				
0	1	1	0					–	+		
0	1	1	1							–	+

CODING FOR SINGLE-ENDED INPUT CHANNEL SELECT (negative input is ground)

SELECTION BITS				INPUT LINES							
M3	M2	M1	M0	LN0	LN1	LN2	LN3	LN4	LN5	LN6	LN7
1	0	0	0	+							
1	0	0	1		+						
1	0	1	0			+					
1	0	1	1				+				
1	1	0	0					+			
1	1	0	1						+		
1	1	1	0							+	
1	1	1	1								+

Bit M3 selects either differential or single-ended mode.

If differential mode is selected, Bit M2 determines the polarity of the input channels.

Bold items are power-up default conditions.

TABLE III. Multiplexer Addressing.

INTERNAL USER-ACCESSIBLE REGISTERS

The registers in the ADS7870 are eight bits wide. Most of the registers are reserved, the ten user-accessible registers are summarized in the Register Address Map (Table I). Detailed information for each register follows. The default power-on/reset state of all bits in the registers is "0".

ADC OUTPUT REGISTERS

The A/D Output registers are read only registers located at ADDR = 0 and ADDR = 1 that contain the results of the A/D conversion, ADC11 through ADC0 (Table IV). The conversion result is in 2's complement format. The bits can be taken out of the registers MSB (D7) first or LSB (D0) first, as determined by the state of the LSB bits (D7 and D0) in the Serial Interface Control register. The ADDR = 0 register also contains the OVR bit which indicates if the internal voltage limits to the PGA have been exceeded.

PGA VALID REGISTER

The PGA Valid register (ADDR = 2) is a read only register that contains the individual results of each of the six comparators for the PGA, VLD5 through VLD0, as shown in Table V.

ADC OUTPUT REGISTERS

ADDR	D7(MSB)	D6	D5	D4	D3	D2	D1	D0
0	ADC3	ADC2	ADC1	ADC0	0	0	0	OVR
1	ADC11	ADC10	ADC9	ADC8	ADC7	ADC6	ADC5	ADC4

ADDR = 0 (LS Byte)

BIT	SYMBOL	NAME	VALUE	FUNCTION
D7-D4	ADC3-ADC0	A/D Output	(1)	Four least significant bits of conversion result.
D3-D1	—	—	0	These bits are not used and are always 0.
D0	OVR	PGA Over-Range	0	Valid conversion result
			1	An analog over-range problem has occurred in the PGA. Conversion result may be invalid. Details of the type of problem are stored in Register 2, the PGA Valid register.

ADDR = 1 (MS Byte)

BIT	SYMBOL	NAME	VALUE	FUNCTION
D7-D0	ADC11-ADC4	ADC Output	(1)	Eight most significant bits of conversion result.

NOTE: (1) Value depends on conversion result.

TABLE IV. ADC Output Registers (ADDR = 0 and ADDR = 1).

PGA VALID REGISTER

ADDR	D7(MSB)	D6	D5	D4	D3	D2	D1	D0
2	0	0	VLD5	VLD4	VLD3	VLD2	VLD1	VLD0

ADDR = 2

BIT	SYMBOL	NAME	VALUE	FUNCTION
D7-D6	—	—	0	These bits are not used and are always 0.
D5	VLD5	PGA Valid 5	0	
			1	Voltage at "–" output from the PGA has exceeded its minimum value.
D4	VLD4	PGA Valid 4	0	
			1	Voltage at "–" output from the PGA has exceeded its maximum value.
D3	VLD3	PGA Valid 3	0	
			1	Voltage at "–" input to the PGA has exceeded its allowable value.
D2	VLD2	PGA Valid 2	0	
			1	Voltage at "+" output from the PGA has exceeded its minimum value.
D1	VLD1	PGA Valid 1	0	
			1	Voltage at "+" output from the PGA has exceeded its maximum value.
D0	VLD0	PGA Valid 0	0	
			1	Voltage at "+" input to the PGA has exceeded its allowable value.

TABLE V. PGA Valid Register (ADDR = 2).

A/D CONTROL REGISTER

The A/D Control register (ADDR = 3) configures the CCLK divider and read back mode option as shown in Table VI.

Read Back Modes

RBM1 and RBM0 determine which of four possible modes is used to read the A/D conversion result from the A/D Output registers.

- Mode 0 (default mode) requires a separate read instruction to be performed in order to read the output of the A/D Output registers
- Mode 1, 2, and 3 provide for different types of automatic read-back options of the conversion results from the A/D Output registers without having to use separate read instructions:

  Mode 1: provides data MS byte first
  Mode 2: provides data LS byte first
  Mode 3: Output only the MS byte

For more information refer to the READ BACK MODE section.

Clock Divider

CFD1 and CFD0 set the CCLK divisor constant which determines the DCLK applied to the A/D, PGA and reference. The A/D and PGA operate with a maximum clock of 2.5MHz. In situations where an external clock is used to pace the conversion process it may be desirable to reduce the external clock frequency before it is actually applied to the PGA and A/D. The signal that is actually applied to the A/D and PGA is called DCLK, where DCLK = CCLK/DF (DF is the division factor determined by the CFD1 and CFD0 bits). For example, if the external clock applied to CCLK is 10MHz and DF = 4 (CFD1 = 1, CFD0 = 0), DCLK equals 2.5MHz.

GAIN/MUX REGISTER

The Gain/Mux register (ADDR = 4) contains the bits that configure the PGA gain (G2-G0) and the input channel selection (M3-M0) as shown in Table III. This register is also updated when direct mode is used to start a conversion so its bit definition is compatible with the instruction byte.

Input Channel Selection

Bits M3 through M0 configure the switches that determine the input channel selection. The input channels may be placed in either differential or single-ended configurations. In the case of differential configuration, the polarity of the input pins is reversible by the state of the M2 bit. The coding for input channels is given in Table III and examples of different input configurations are shown in Figure 7.

Convert/Busy

If the CNV/BSY bit is set to a "1" during a write operation, a conversion will start on the second falling edge of CCLK after the active edge of SCLK that latched the data into the Gain/Mux register. The CNV/BSY bit may be read with a read instruction. The CNV/BSY bit will bet set to "1" in a read operation if the ADS7870 is performing a conversion at the time the register is sampled in the read operation.

Gain Select

Bits G2 through G0 control the gain of the programmable gain amplifier. PGA gains of 1, 2, 4, 5, 8, 10, 16 and 20 are available. The coding is shown in Table VII.

DIGITAL INPUT/OUTPUT STATE REGISTER

The Digital I/O State register (ADDR = 5) contains the state of each of the four digital I/O pins. Each pin can function as a digital input (the state of the pin is set by an external signal connected to it) or a digital output (the state of the pin is set by data from a serial input to the ADS7870). The input/output functional control is established by the digital I/O mode control bits (OE3-OE0) in the Digital I/O Control register. In addition, the convert/busy bit (CNV/BSY) can be used to start a conversion via a write instruction or determine if the converter is busy by executing a read instruction.

Digital I/O State Bits

Bits D3 through D0 (I/O3-I/O0) of the Digital I/O State register are the state bits. If the corresponding mode bit makes the pin a digital input, the state bit indicates whether the external signal connected to the pin is a "1" or a "0". It is not possible to control the state of the corresponding bit with a write operation. The state of the bit is only controlled by the external signal connected to the digital I/O pin. Coding is shown in Table VIII.

ADC CONTROL REGISTER

ADDR	D7 (MSB)	D6	D5	D4	D3	D2	D1	D0
3	0	0	0	0	RBM1	RBM0	CFD1	CFD0

ADDR = 3

BIT	SYMBOL	NAME	VALUE	FUNCTION
D7-D4	—	—	0	These bits are reserved and must always be written 0.
D3-D2	RBM1-RBM0	Read Back Mode	**00** 01 10 11	**Mode 0 - Read instruction required to access ADC conversion result.** Mode 1 - Most significant byte returned first Mode 2 - Least significant byte returned first Mode 3 - Only most significant byte returned
D1-D0	CFD1-CFD0	CCLK Divide	**00** 01 10 11	**Division factor for CCLK = 1 (DCLK = CCLK)** Division factor for CCLK = 2 (DCLK = CCLK/2) Division factor for CCLK = 4 (DCLK = CCLK/4) Division factor for CCLK = 8 (DCLK = CCLK/8)

Bold items are power-up default conditions.

TABLE VI. ADC Control Register (ADDR = 3).

GAIN/MUX REGISTER

ADDR	D7 (MSB)	D6	D5	D4	D3	D2	D1	D0
4	CNV/BSY	G2	G1	G0	M3	M2	M1	M0

ADDR = 4

BIT	SYMBOL	NAME	VALUE	FUNCTION
D7	CNV/BSY	Convert/Busy	**0** 1	**Idle Mode** Busy Mode; write = start conversion
D6-D4	G2-G0	PGA Gain Select	**000** 001 010 011 100 101 110 111	**PGA Gain = 1** PGA Gain = 2 PGA Gain = 4 PGA Gain = 5 PGA Gain = 8 PGA Gain = 10 PGA Gain = 16 PGA Gain = 20
D3-D0	M3-M0	Input Channel Select	Table III	Determines input channel selection for the requested conversion, differential or single-ended configuration.

Bold items are power-up default conditions.

TABLE VII. Gain/Mux Register (ADDR = 4).

DIGITAL I/O STATE REGISTER

ADDR	D7 (MSB)	D6	D5	D4	D3	D2	D1	D0
5	CNV/BSY	0	0	0	IO3	IO2	IO1	IO0

ADDR = 5

BIT	SYMBOL	NAME	VALUE	FUNCTION
D7	CNV/BSY	Convert/Busy	**0** 1	**Idle Mode** Busy Mode; Write = Start Conversion
D6-D4	—	—	0	These bits are not used and are always 0.
D3	IO3	State for I/O3	**0** 1	**Input or Output State = 0** Input or Output State = 1
D2	IO2	State for I/O2	**0** 1	**Input or Output State = 0** Input or Output State = 1
D1	IO1	State for I/O1	**0** 1	**Input or Output State = 0** Input or Output State = 1
D0	IO0	State for I/O0	**0** 1	**Input or Output State = 0** Input or Output State = 1

Bold items are power-up default conditions.

NOTE: When the Mode Control makes a pin a Digital Input, it is not possible to control the state of the corresponding bit in the Digital I/O State register with a write operation. The state of the bit is only controlled by the external signal connected to the Digital I/O pin.

TABLE VIII. Digital I/O State Register (ADDR = 5).

The four digital I/O pins allow control of external circuitry, such as a multiplexer, or allow the digital status lines from other devices to be read without using any additional microcontroller pins. Reads from this register always reflect the state of the pin, not the state of the latch inside the ADS7870. These may be different if the pin(s) is configured as an input or if there is a fault condition on an output pin(s).

Convert/Busy

If CNV/BSY is set to a "1" during a write operation, a conversion will start on the second falling edge of CCLK after the active edge of SCLK that latched the data into the Digital I/O register. The CNV/BSY bit may be read with a read instruction. The CNV/BSY will be set to "1" in a read operation if the ADS7870 is performing a conversion at the time the register is sampled in the read operation.

DIGITAL I/O CONTROL REGISTER

The Digital I/O Control register (ADDR = 6) contains the information that determines whether each of the four digital I/O lines is configured as an input or output. Setting the appropriate OE bit to "1" enables the corresponding I/O pin as an output. Setting the appropriate OE bit to "0" enables the corresponding I/O pin as an input (see Table IX).

REFERENCE/OSCILLATOR CONFIGURATION REGISTER

The Reference/Oscillator Configuration register (ADDR = 7) determines whether the internal oscillator is used for the conversion clock (OSCE and OSCR), whether the internal voltage reference and buffer are on or off (REFE and BUFE), and whether the reference is 2.5V, 2.048V, or 1.15V as shown in Table X.

Oscillator Control

The internal voltage reference uses a switched capacitor technique which requires a clocking signal input. When OSCR = 1, the clocking signal for the reference comes from the internal oscillator. When OSCR = 0, the clocking signal for the reference is derived from the signal on the CCLK pin and affected by the frequency divider controlled by the CFD0 and CFD1 bits in the A/D Control register.

The OSCE bit is the internal oscillator enable bit. When it is set to "1" power is applied to the internal oscillator causing it to produce a 2.5MHz output and causing the signal to appear at the CCLK pin. The internal oscillator is also enabled when the OSCR bit is set to "1" and the REFE bit is also set to "1".

The internal oscillator is also enabled when the OSC ENABLE pin is set to "1". The power-up default condition is "0" for OSCE and OSCR. If either the OSC ENABLE pin is held high or these control register bits are "1" then the oscillator will be turned on.

Voltage Reference and Buffer Enable

When the REFE bit = "0" (power-up default condition), the reference is powered down and draws no current. When it is set to "1", it is powered up and draws approximately 190µA of current.

When the BUFE bit = "0" (power-up default condition) the buffer amplifier is powered down and draws no current. When it is set to "1", it is powered up and draws approximately 150µA of current.

DIGITAL I/O CONTROL REGISTER

ADDR	D7 (MSB)	D6	D5	D4	D3	D2	D1	D0
6	0	0	0	0	OE3	OE2	OE1	IOE0

ADDR = 6

BIT	SYMBOL	NAME	VALUE	FUNCTION
D7-D4	—	—	0	These bits are reserved and must always be set to 0.
D3	OE3	State for I/O3	**0** 1	**Digital I/O 1 = digital input** Digital I/O 1 = digital output
D2	OE2	State for I/O2	**0** 1	**Digital I/O 2 = digital input** Digital I/O 2 = digital output
D1	OE1	State for I/O1	**0** 1	**Digital I/O 3 = digital input** Digital I/O 3 = digital output
D0	OE0	State for I/O0	**0** 1	**Digital I/O 4 = digital input** Digital I/O 4 = digital output

Bold items are power-up default conditions.

TABLE IX. Digital I/O Control Register (ADDR = 6).

REFERENCE/OSCILLATOR REGISTER

ADDR	D7 (MSB)	D6	D5	D4	D3	D2	D1	D0
7	0	0	OSCR	OSCE	REFE	BUFE	R2V	RBG

ADDR = 7

BIT	SYMBOL	NAME	VALUE	FUNCTION
D7-D6	—	—	0	These bits are reserved and must always be set to 0.
D5	OSCR	Oscillator Control	**0** 1	**Source of clock for internal V_{REF} is CCLK pin.** Clocking signal comes from the internal oscillator.
D4	OSCE	Oscillator Enable	**0** 1	**CCLK is configured as an input.** CCLK outputs a 2.5MHz signal (70µA).
D3	REFE	Reference Enable	**0** 1	**Reference is powered down and draws no current.** Reference is powered up and draws 190µA of current.
D2	BUFE	Buffer Enable	**0** 1	**Buffer is powered down and draws no current.** Buffer is powered up and draws 150µA of current.
D1	R2V	2V Reference	**0** 1	**V_{REF} = 2.5V (RBG bit = 0)** V_{REF} = 2.048V (RBG bit = 0)
D0	RBG	Bandgap Reference	**0** 1	**Bit R2V determines the value of the reference voltage.** V_{REF} = 1.15V

Bold items are power-up default conditions.

TABLE X. Reference/Oscillator Configuration Register (ADDR = 7).

Selecting the Reference Voltage

When the RBG bit is set to "1" the voltage on the V_{REF} pin is 1.15V and the R2V bit has no effect. When this bit is set to "0" (power-up default condition), the R2V bit determines the value of the reference voltage.

When R2V = 0 and RBG = 0 (power-up default condition), the voltage at the V_{REF} pin is 2.5V. When R2V = 1 and RBG = 0, the reference voltage is 2.048V.

A 12-bit bipolar input A/D converter has 4096 states and each state corresponds to 1.22mV with the 2.500V reference. With a 2.048V reference, each A/D bit corresponds to 1.0mV.

SERIAL INTERFACE CONTROL REGISTER

The Serial Interface Control register (ADDR = 24), see Table XI, allows certain aspects of the serial interface to be controlled by the user. It controls whether data is presented MSB or LSB first, whether the serial interface is configured for 2-wire or 3-wire operation and determines proper timing control for 8051-type microprocessor interfaces.

The information in this register is formatted with the information symmetric about its center. This is done so that it may be read or written either LSB (bit D7) or MSB (bit D0) first. Each control bit has two locations in the register. If either of the two is set, the function is activated. This arrangement can potentially simplify micro-controller communication code.

The instruction byte to write this configuration data to Register 24 is itself symmetric. From Table I, a register mode write instruction of 8 bits to address 24 is "0001 1000" in binary form. Therefore, this command will be valid under all conditions.

LSB or MSB

The LSB bit determines whether the serial interface receives and transmits either LSB or MSB first. Setting the LSB bit ("1") configures the interface to expect all bytes LSB first as opposed to the default MSB first (LSB = "0").

2-Wire or 3-Wire Operation

The 2W bit configures the ADS7870 for two-wire or three-wire mode. In two-wire mode (2W = 1), the DIN pin is enabled as an output during the data output portion of a read instruction. The DIN pin accepts data when the ADS7870 is receiving and it outputs data when the ADS7870 is transmitting. When data is being sent out of the DIN pin, it also appears on the DOUT pin as well. In three-wire mode (2W = 0), data to the ADS7870 is received on the DIN pin and is transmitted on the DOUT pin. The power-up default condition is three-wire mode.

Serial Interface Timing (8051 Bit)

The 8051 bit will change the timing of when the DIN pin will go to high impedance at the end of a operation. When the bit is a "1" the pin goes to high impedance on the last active SCLK edge of the last byte of data transfer instead of waiting for the next inactive edge or $\overline{CS}$ to go inactive. This allows the ADS7870 to disconnect from the data lines soon enough to avoid contention with an 80C51-type interface. The 80C51 drives data four CPU cycles before an inactive SCLK edge and for two CPU cycles after an active SCLK edge. When the bit is a "0" the DIN pin goes high impedance on the next inactive SCLK edge or when $\overline{CS}$ goes inactive ("1").

SERIAL INTERFACE CONTROL REGISTER

ADDR	D7 (MSB)	D6	D5	D4	D3	D2	D1	D0
24	LSB	2W	8051	0	0	8051	2W	LSB

ADDR = 24

BIT	SYMBOL	NAME	VALUE	FUNCTION
D7	LSB	LSB or MSB first	**0** 1	**Serial Interface receives and transmits MSB first.** Serial Interface receives and transmits LSB first.
D6	2W	2-Wire or 3-Wire	**0** 1	**3-Wire Mode** 2-Wire Mode
D5	8051	Serial Interface	**0** 1	**DIN high impedance on the next inactive edge or when CS goes inactive**. DIN pin is high impedance on last active SCLK edge of the last byte of data transfer.
D4-D3	—	—	0	These bits are reserved and must always be set 0.
D2	8051	Serial Interface	**0** 1	**DIN high impedance on the next inactive edge or when CS goes inactive** DIN pin is high impedance on last active SCLK edge of the last byte of data transfer
D1	2W	2-Wire or 3-Wire	**0** 1	**3-Wire Mode** 2-Wire Mode
D0	LSB	LSB or MSB first	**0** 1	**Serial Interface receives and transmits MSB first.** Serial Interface receives and transmits LSB first.

Bold items are power-up default conditions.

TABLE XI. Serial Interface Control Register (ADDR = 24).

Figures 8 and 9 show the timing of when the ADS7870 will set the DIN pin to high impedance mode at the end of a read operation when the 2W bit is set. The behavior of DOUT does not depend of the state of 2W. The 8051 bit is not set for these two examples.

Figure 10 shows the timing for entering the high impedance state when the 8051 bit is set. Notice that on the last bit of the read operation the DIN (and DOUT) pin goes to the high impedance state on the active edge of SCLK instead of waiting for the inactive edge of SCLK or $\overline{CS}$ going high as shown in Figures 8 and 9. This is for compatibility with 80C51 Mode 0 type serial interfaces. An 80C51 forces DIN valid before the SCLK falling edge and holds it valid until after the SCLK rising edge. This can lead to contention but setting the 8051 bit fixes this potential problem without requiring $\overline{CS}$ to be toggled high after every read operation.

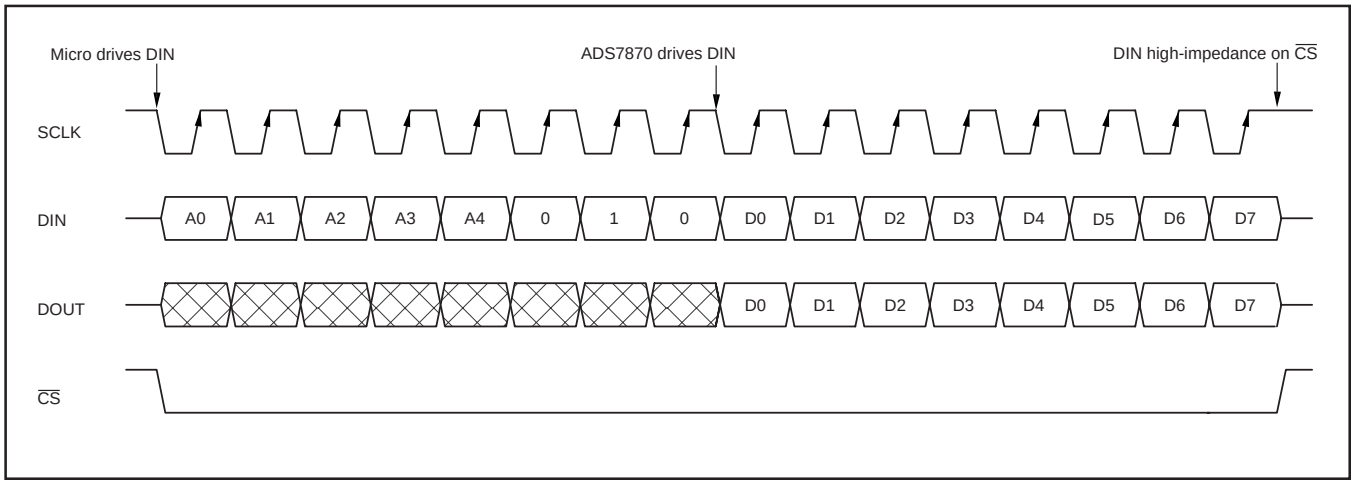


FIGURE 8. Timing for High Impedance State on DIN/DOUT ($\overline{CS}$ = "1").

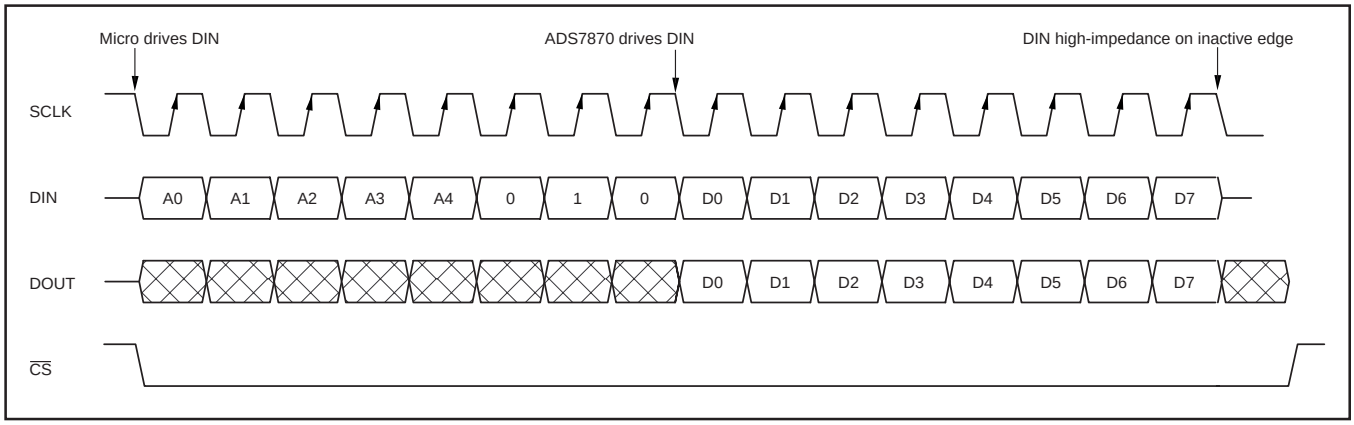


FIGURE 9. Timing for High Impedance State on DIN/DOUT (Inactive SCLK edge).

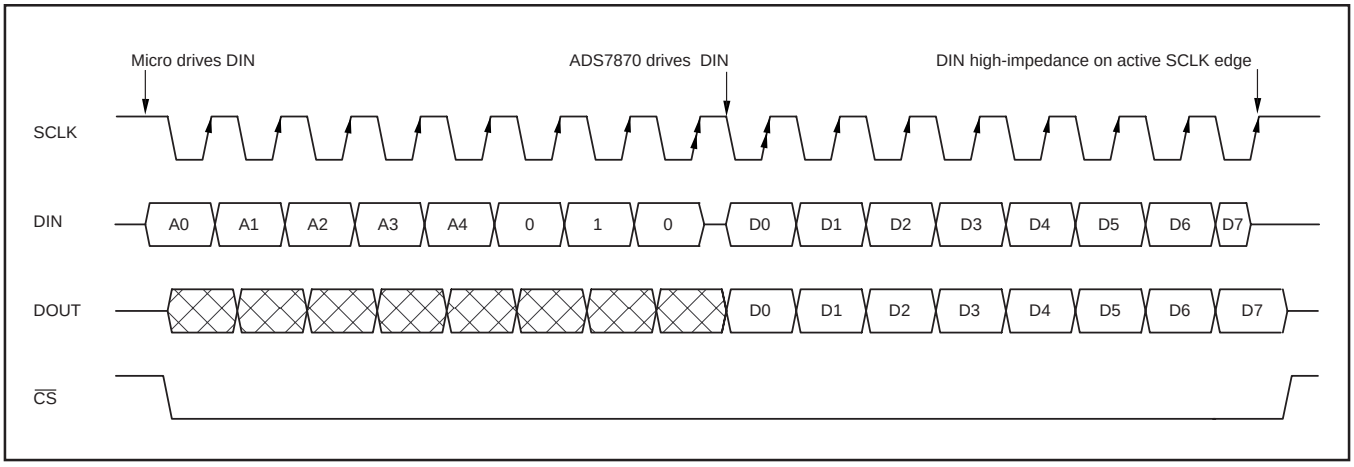


FIGURE 10. Timing for High Impedance State on DIN/DOUT (8051 bit = "1").

ID Register

The ADS7870 has an ID Register (at ADDR = 31) to allow the user to identify which revision of the ADS7870 is installed. This is shown in Table XII.

Remaining Registers

The remaining register addresses are not used in the normal operation of the ADS7870. These registers will return random values when read and non-zero writes to these registers will cause erratic behavior. Unused bits in the partially used registers must always be written low.

STARTING A CONVERSION THROUGH THE SERIAL INTERFACE

There are two methods of starting a conversion cycle through the serial interface. The first (non-addressed or "direct" mode) is by using the start conversion byte as described earlier. The second (addressed mode) is by setting the CNV/BSY bit in one of the registers by performing a write instruction.

The conversion will start on the second falling edge of CCLK after the eighth active edge of SCLK (for the instruction in non-addressed mode or the data in addressed mode). The BUSY pin will go active ("1") one DCLK period (1, 2, 4, or 8 CCLK periods depending on CFD1 and CFD0) after the start of a conversion. This delay is to allow BUSY to go inactive when conversions are queued to follow in immediate succession. BUSY will go inactive at the end of the conversion.

If a conversion is already in progress when the CNV/BSY bit is set on the eighth active SCLK edge, the CNV/BSY bit will be placed in queue and the current conversion will be allowed to finish. If a conversion is already queued, the new one will replace the currently queued conversion. The queue is only one conversion long. Immediately upon completion of the current conversion, the next conversion will start. This allows for maximum throughput through the A/D converter. Since BUSY is defined to be inactive for the first A/D clock period of the conversion, the inactive (falling) edge of BUSY can be used to mark the end of a conversion (and start of the next conversion).

Figure 11 shows the timing of a conversion start using the convert start instruction byte. The double rising arrow on SCLK indicates when the instruction is latched. The double falling arrow on CCLK indicates where the conversion cycle will actually start (second falling edge of CCLK after the eight active edge of SCLK). This example is for LSB first, CCLK divider = 1, and SCLK active on rising edge. Notice that BUSY goes active one CCLK period later since CCLK divider = 1.

ID REGISTER

ADDR	D7 (MSB)	D6	D5	D4	D3	D2	D1	D0
31	0	0	0	0	0	0	0	1

ADDR = 31

BIT	SYMBOL	NAME	VALUE	FUNCTION
D7-D0	—	—	—	The contents of this register identify the revision of the ADS7870.

TABLE XII. ID Register (ADDR = 31).

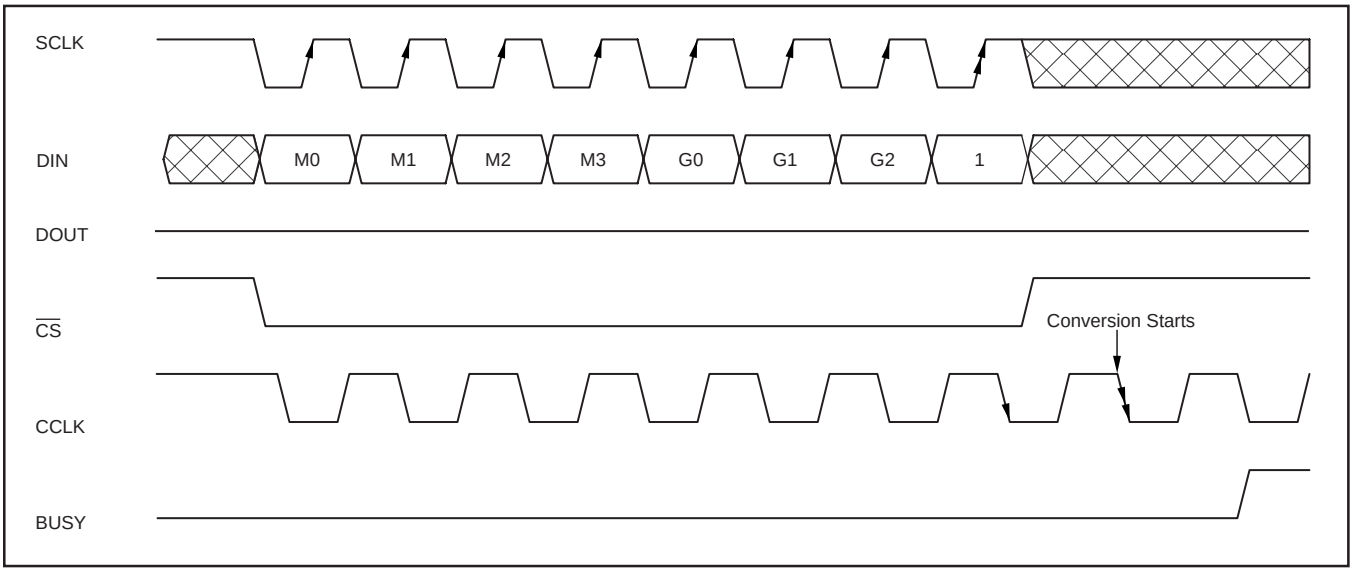


FIGURE 11. Timing Diagram Example for a Conversion Start using Serial Interface Convert Instruction.

Figure 12 shows an example of a conversion start using an 8-bit write operation to the Gain/Mux Register with the CNV/BSY bit set to "1". The double rising arrow on SCLK indicates where the data is latched into the Gain/Mux register and the double arrow on CCLK indicates when the conversion will start. The example is for LSB first, CCLK divider = 1, and SCLK active on rising edge.

Figure 13 shows the timing of a conversion start using the convert start instruction byte when a conversion is already in progress (indicated by BUSY high). The double rising arrow on SCLK indicates when the instruction is latched. The second falling arrow on CCLK indicates when the conversion cycle would have started had a conversion not been in progress. The double falling arrow on CCLK indicates where the conversion cycle will actually start (immediately after completion of the previous conversion). This example is for LSB first, CCLK divider = 2, and SCLK active on rising edge. Notice that BUSY will be low for two CCLK periods because the CCLK divider = 2.

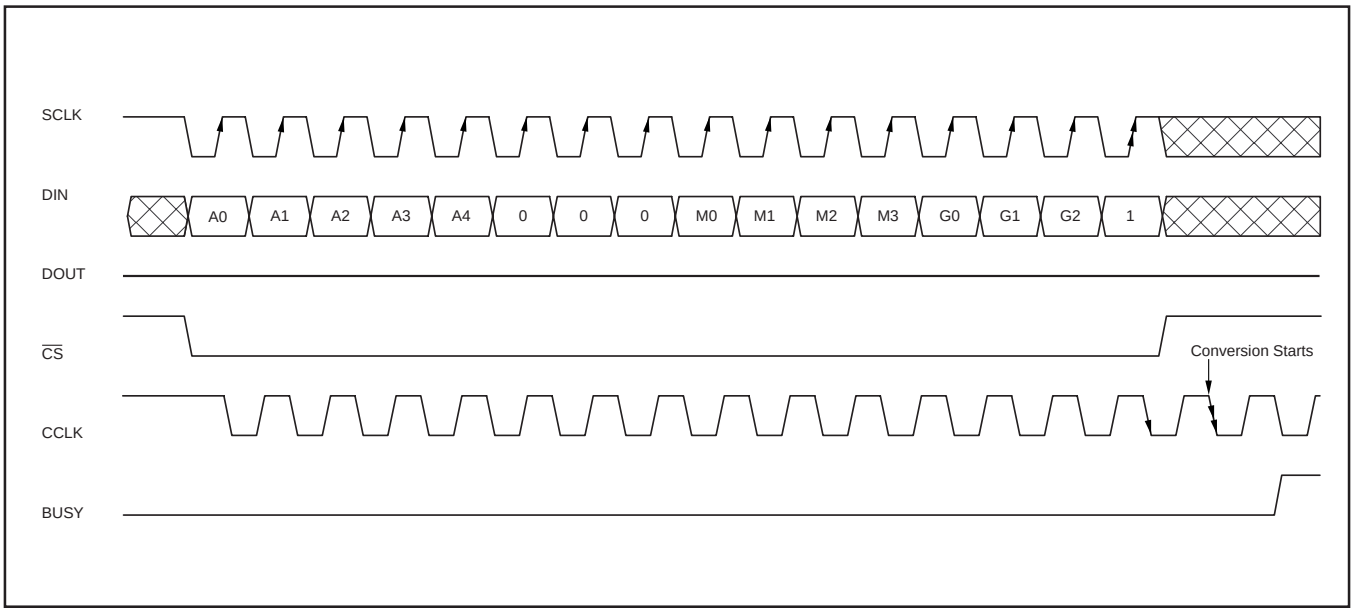


FIGURE 12. Timing Diagram Example for a Conversion Start using 8-Bit Write to the Gain/Mux Register.

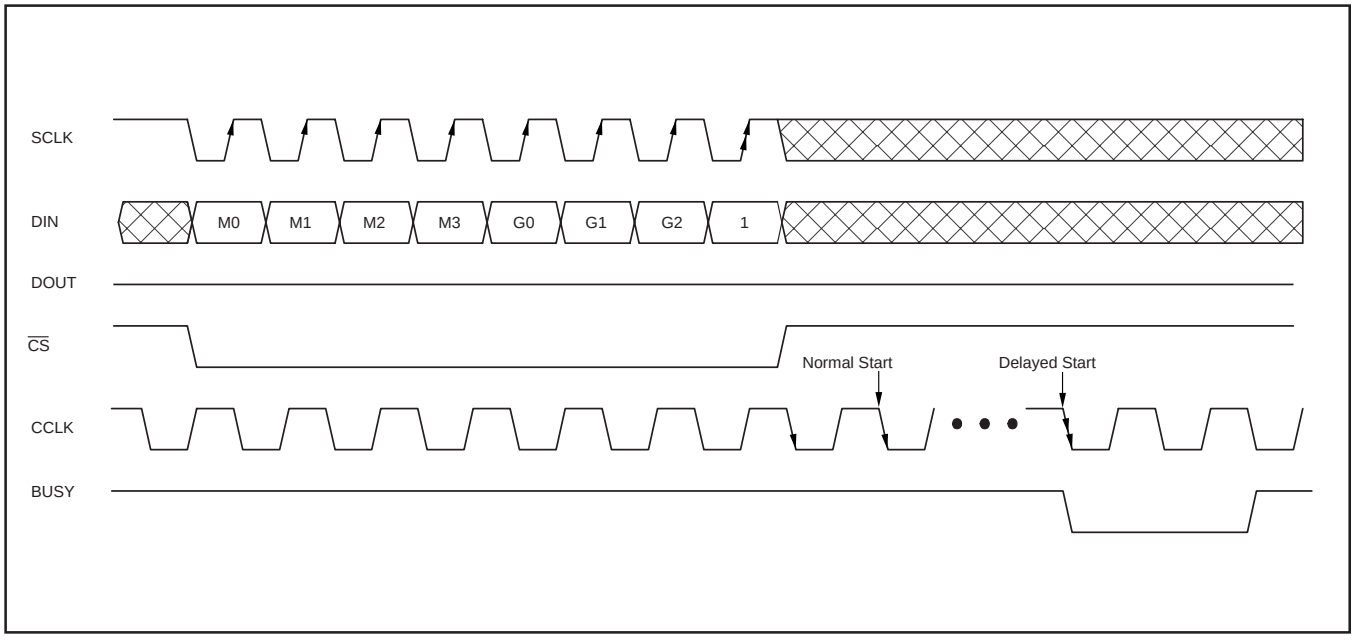


FIGURE 13. Timing Diagram Example of Delayed Conversion Start with Serial Interface.

STARTING A CONVERSION USING THE CONVERT PIN

A conversion can also be started by an active (rising) edge on the CONVERT pin. Similar to the CNV/BSY register bit, the conversion will start on the second falling edge of CCLK after the Convert rising edge.

The CONVERT pin must stay high for at least two CCLK periods. CONVERT must also be low for at least two CCLK periods before going high. BUSY will go active one DCLK period after the start of the conversion.

Contrary to the CNV/BSY bit in the register, the Convert pin will abort any conversion in process and restart a new conversion. BUSY will go low at the end of the conversion. $\overline{CS}$ may be either high or low when the Convert pin starts a conversion.

Figure 14 shows the timing of a conversion start using the CONVERT pin. The double falling arrow on CCLK indicates when the conversion cycle will actually start (the second active CCLK edge after CONVERT goes active). This example is for CCLK divider = 4. Notice that BUSY goes active four CCLK periods later.

READ BACK MODES

There are four automatic modes available to read the A/D conversion result from the A/D Output Registers. The RBM1 and RBM0 bits in the A/D Control Register (ADDR = 3) control which mode is used by ADS7870.

- Mode 0 (default mode) requires a separate read instruction to retrieve the conversion result
- Mode 1 provides the output most significant byte first
- Mode 2 provides the output least significant byte first.
- Mode 3 provides only the most significant byte

Mode 3 will not short cycle the A/D. Automatic Read Back Mode is only triggered when starting a conversion using the serial interface. Conversions started using the CONVERT pin do not trigger the read back mode

The first bit of data for an automatic read back is sampled on the first active SCLK edge of the read portion of instruction. The remaining bits are sampled on the next inactive SCLK edge (the first one after the first active edge). To avoid getting one bit from one conversion and the remainder of the byte from another conversion, a conversion should not finish between the first active SCLK edge and the next inactive edge.

Mode 0

Mode 0 (default operating mode) requires a read instruction to be performed to retrieve a conversion result. MS byte first format is achieved by performing a sixteen bit read from ADDR = 1. LS byte first format is achieved by performing a sixteen bit read from ADDR = 0. The most significant byte only can be achieved by performing an eight bit read from ADDR = 1.

To increase throughput it is possible to read the result of a conversion while a conversion is in progress. The last conversion to be completed prior to the first active SCLK edge of the conversion data word (not the instruction byte) is retrieved. This overlapping allows a sequence of start conversion N, read conversion N – 1, start conversion N + 1, read conversion N, etc. For conversion 0, the result of conversion –1 would need to be discarded.

Mode 1

In this mode, the serial interface configures itself to clock out a conversion result as soon as a conversion is started. This is useful since a read instruction is not required so eight SCLK cycles are saved. This mode operates like an implied sixteen bit read instruction byte for ADDR = 1 was sent to the ADS7870 after starting the conversion

It is not necessary to wait for the end of the conversion to start clocking out conversion results. The last completed conversion at the sampling edge of SCLK will be read back (whether a conversion is in progress or not.)

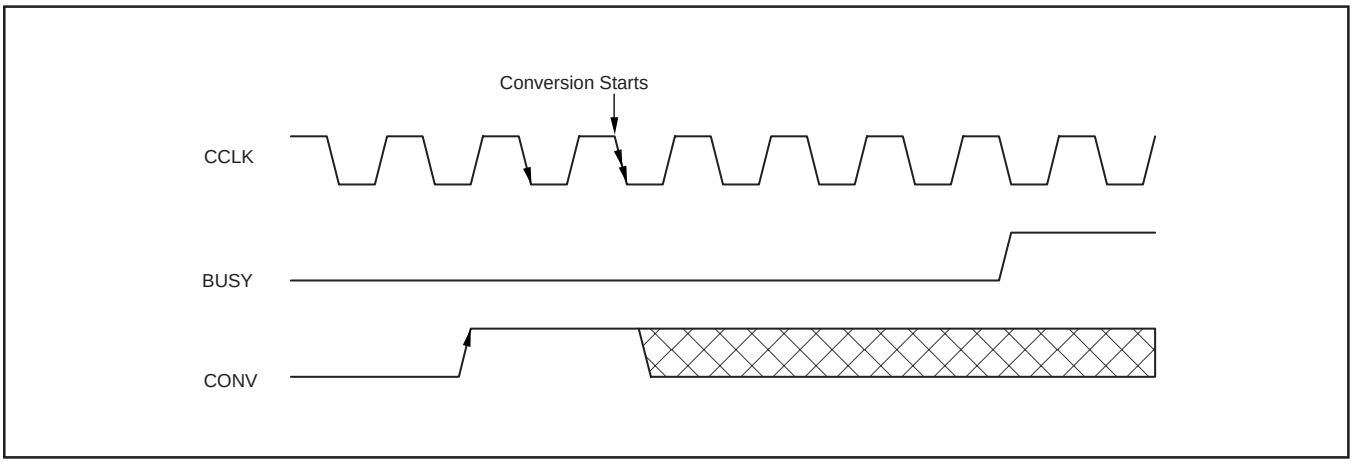


FIGURE 14. Timing Diagram Example of Conversion Start Using Convert Pin.

Mode 2

This mode is similar to Mode 1 except that the conversion result is provided LS byte first (equivalent to a sixteen bit read from ADDR = 0).

Figures 15 and 16 show timing examples of an automatic read back operation using Mode 2. In Figure 15, the result of the previous conversion is retrieved. This example is for LSB first, CCLK divider = 2, and SCLK active on rising edge. The data may be read back immediately after the start conversion instruction. It is not necessary to wait for the conversion to actually start (or finish).

In Figure 16 the result of the just requested conversion is retrieved. The micro-controller must wait for BUSY to go inactive before clocking out the ADC Output Register. $\overline{CS}$ must stay low while waiting for BUSY. This example is for LS byte first, CCLK divider = 1, and SCLK active on falling edge. Notice that the DOUT pin is not driven with correct data until the appropriate active edge of SCLK.

Mode 3

This mode only returns the most significant byte of the conversion. It is equivalent to an eight bit read from ADDR = 1.

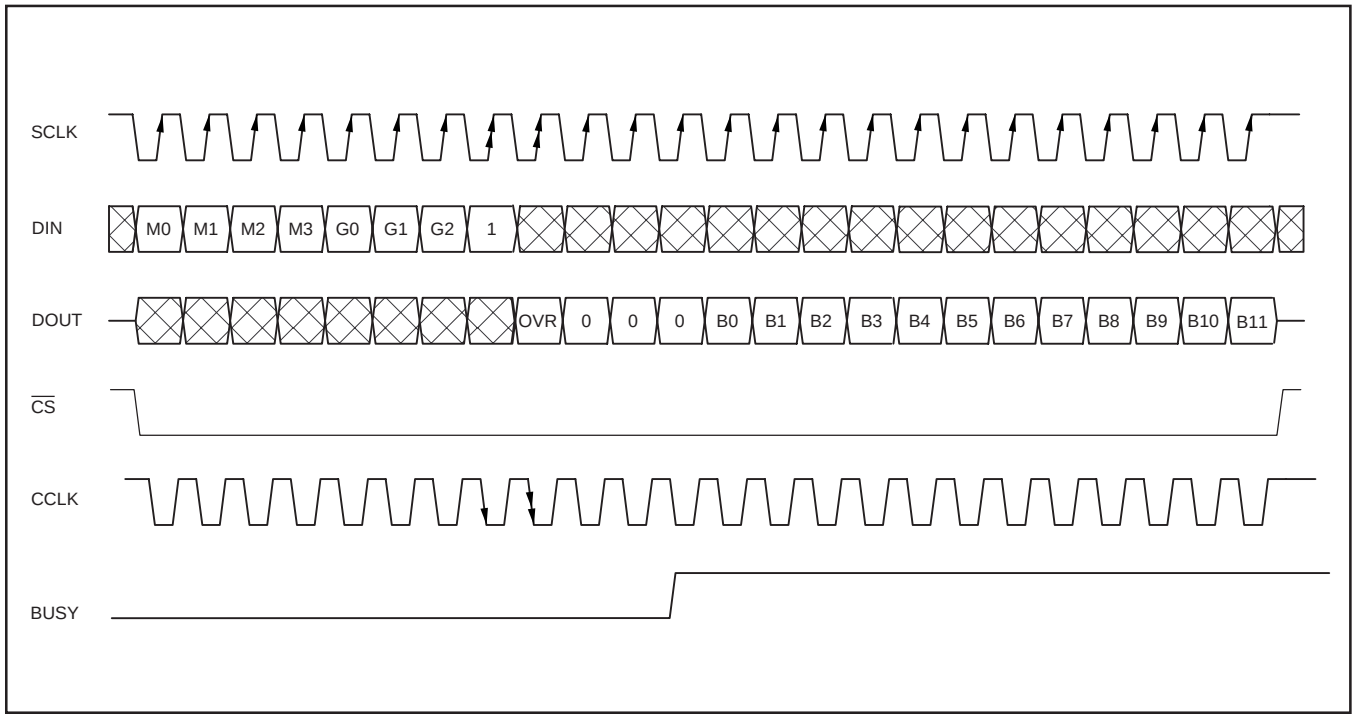


FIGURE 15. Timing Diagram for Automatic Read Back of Previous Conversion Result Using Mode 2.

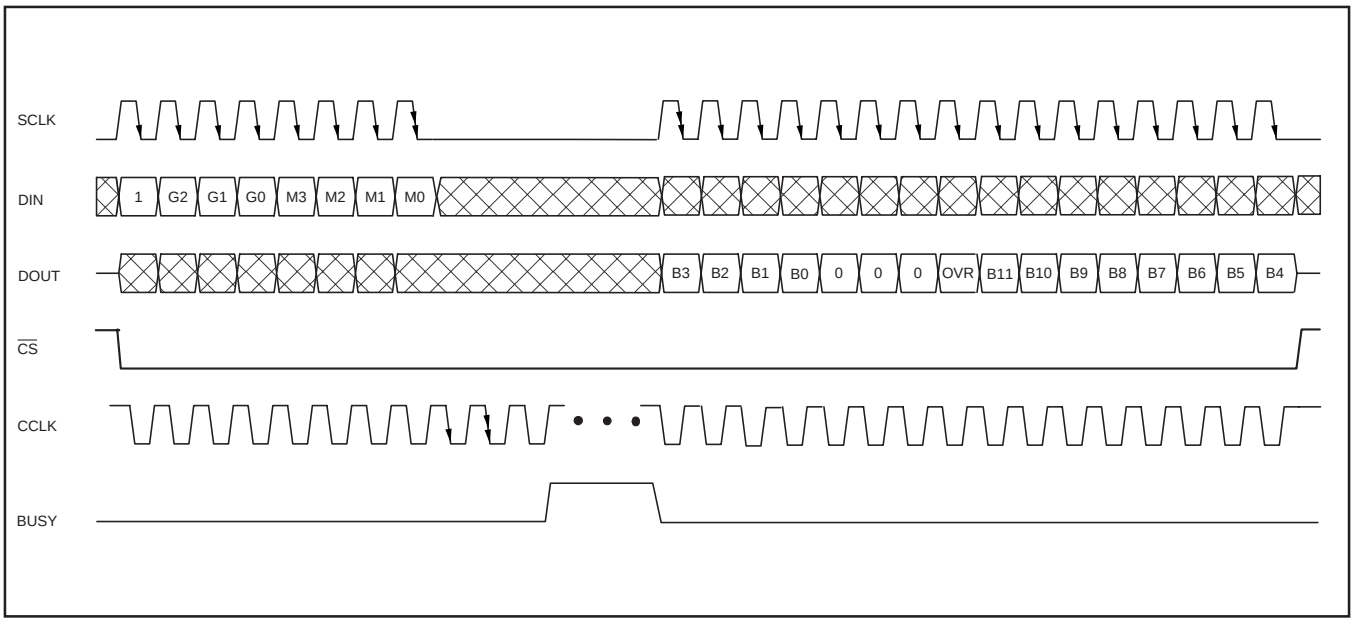


FIGURE 16. Timing Diagram for Automatic Read Back of Current Conversion Result Using Mode 2.

APPLICATIONS

REQUIRED SUPPORT ELEMENTS

As with any precision analog integrated circuit, good power supply bypassing is required. A low ESR ceramic capacitor in parallel with a large value electrolytic across the supply line will furnish the required performance. Typical values are 0.1µF and 10µF respectfully.

Noise performance of the internal voltage reference circuit is improved if a ceramic capacitor of approximately 0.01µF is connected from V_{REF} to ground. Increasing the value of this capacitor may bring slight improvement in the noise on V_{REF} but will increase the time required to stabilize after turn on.

If the internal buffer amplifier is used it must have an output filter capacitor connected to ground to ensure stability. A nominal value of 0.47µF provides the best performance. Any value between 0.1µF and 10µF is acceptable. In installations where one ADS7870 buffer is used to drive several devices an additional filter capacitor of 0.1µF should be installed at each of the slave devices.

Pin 15 is specified as a no-connect pin. The circuit is used in manufacture and should either be left open or connected to ground. There will be no significant current flow through it.

The circuit in Figure 17 shows a typical installation with all control functions under control of the host embedded controller. The SCLK is active on the falling edge. If the internal voltage reference and oscillator are used, they must be turned on by setting the corresponding control bits in the device registers. These registers must be set on power up and after any reset operation.

MICRO-CONTROLLER CONNECTIONS

The ADS7870 is quite flexible in interfacing to various micro-controllers. Connections using the hardware mode of two types of controllers (Motorola M68HC11, Intel 80C51) are described below.

Motorola M68HC11 (SPI)

The Motorola M68HC11 has a three-wire (four if you count the slave select) serial interface that is commonly referred to as SPI. (Serial Peripheral Interface) where the data is transmitted MSB first. This interface is usually described as the micro-controller and the peripheral each having two 8-bit shift registers (one for receiving and one for transmitting.)

The transmit shift register of the micro-controller and the receive shift register of the peripheral are connected together and vice versa. SCK controls the shift registers. SPI is capable of full duplex operation (simultaneous read and write.) The ADS7870 will not support full duplex operation. The ADS7870 can only be written to or read from. It cannot do both simultaneously.

Since the M68HC11 can configure SCK to have either rising or falling edge active, the RISE/$\overline{\text{FALL}}$ pin on the ADS7870 can be in which ever state is appropriate for the desired mode of operation of the M68HC11 for compatibility with other peripherals.

In the Interface Configuration Register (Table XI), the 2W bit should be cleared (default). The LSB bit should be clear (default.) The 8051 bit should also be clear (default.) Since the ADS7870 will default to SPI mode, the M68HC11 should not need to initialize the ADS7870 Interface Configuration Register after power-on or reset.

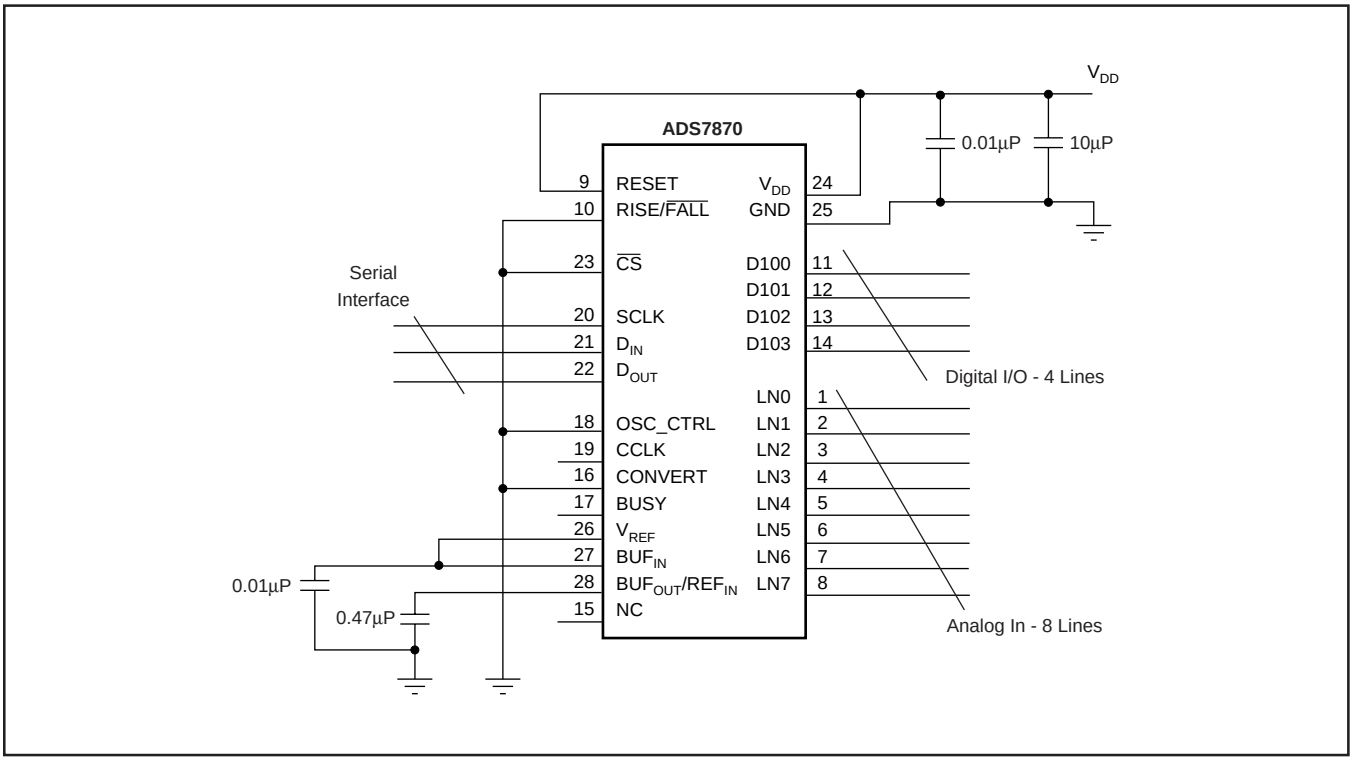


FIGURE 17. Typical Operation with Recommended Capacitor Values.

Figure 18 shows a typical physical connection between an M68HC11 and a ADS7870. A pull-up resister on DOUT may be needed to keep DOUT from floating during write operations. $\overline{CS}$ may be permanently tied low if desired, but the ADS7870 must be the only peripheral.

Intel 80C51

The Intel 80C51 operated in serial port Mode 0 has a two-wire (three-wire if an additional I/O pin is used for $\overline{CS}$) serial interface. The TXD pin provides the clock for the serial interface and RXD serves as the data input and output. The data is transferred LSB first. Best compatibility is achieved by connecting the RISE/$\overline{FALL}$ pin of the ADS7870 high (rising edge of SCLK active). In the Interface Configuration Register, the LSB bit and the 8051 bit should be set. The 2W bit should also be set. The first instruction after power-on or reset should be a write operation to the Interface Configuration Register.

Figure 19 shows a typical physical connection between an 80C51 and an ADS7870. $\overline{CS}$ may be permanently tied low if desired, but the ADS7870 must be the only peripheral.

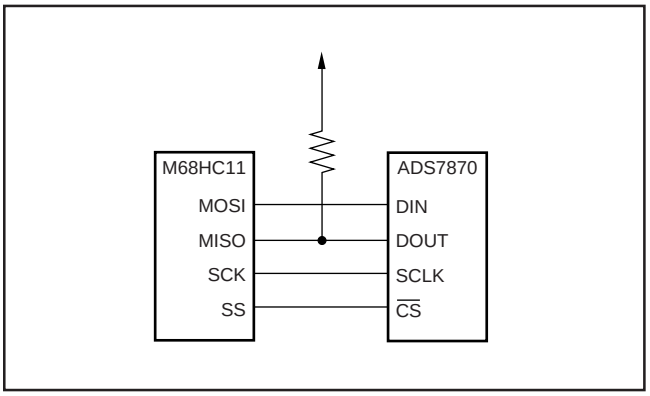


FIGURE 18. Connection of M68HC11 to the ADS7870.

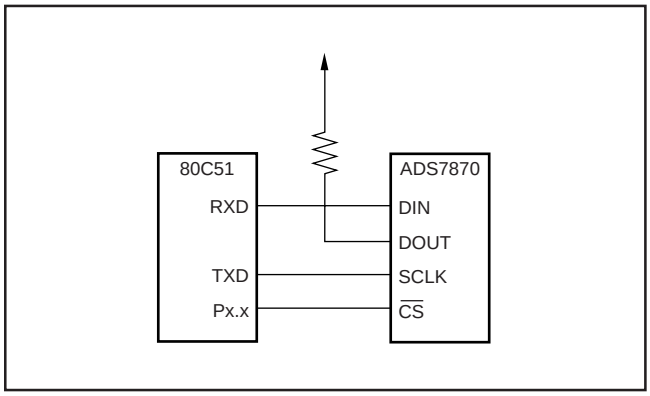


FIGURE 19. Connection of 80C51 to the ADS7870.

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