



# AK4525

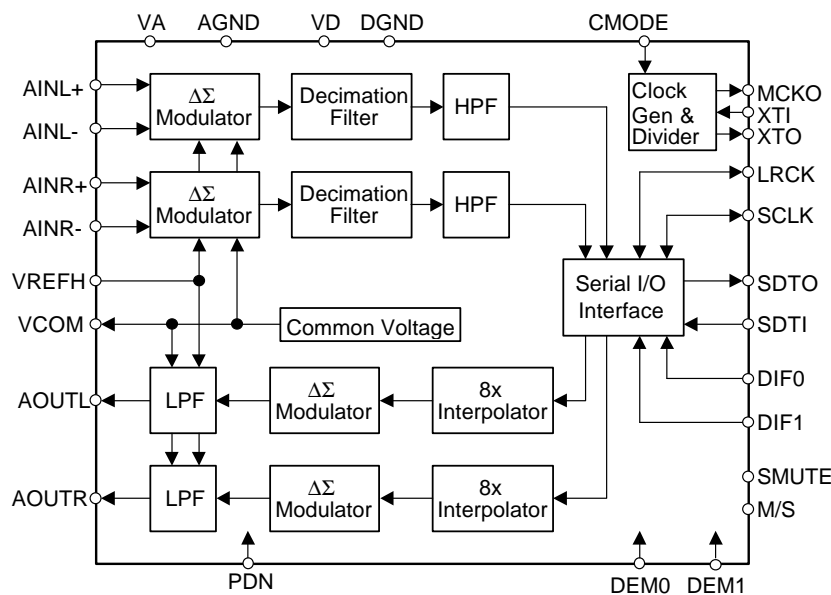
## 20Bit Stereo $\Delta\Sigma$ ADC & DAC with X' tal Osc

### GENERAL DESCRIPTION

The AK4525 has a dynamic range of 100dB and is well-suited middle-range MD, surround system, musical instruments and car audio. Analog inputs are full-differential with single-end capability. Analog outputs are single-ended. The AK4525 has X' tal oscillation circuit and master mode.

### FEATURES

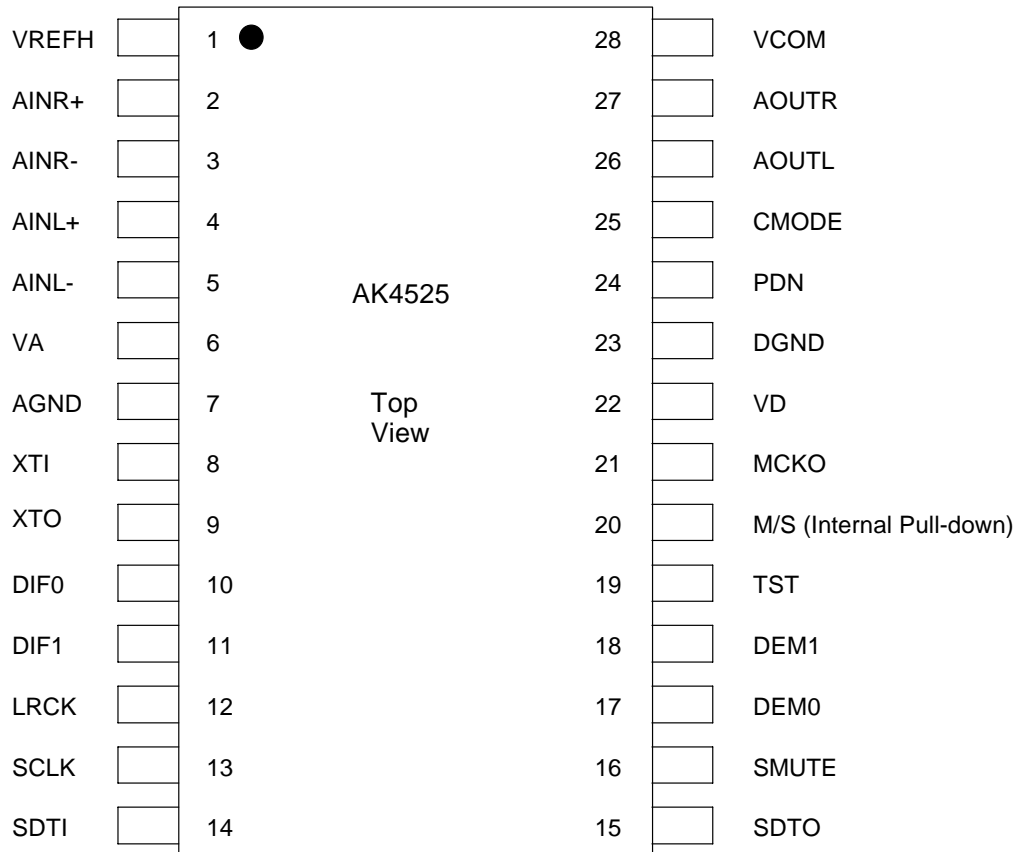
- $\Delta\Sigma$  Stereo ADC
  - 64x Oversampling
  - Sample Rate Ranging from 32kHz to 48kHz
  - S/(N+D): 92dB
  - Dynamic range, S/N: 100dB
  - Digital HPF for offset cancellation
- $\Delta\Sigma$  Stereo DAC
  - 128x Oversampling
  - Sampling Rate Ranging from 32kHz to 48kHz
  - 2nd order SCF + 2nd order CTF
  - Digital de-emphasis for 32kHz, 44.1kHz, 48kHz sampling
  - S/(N+D): 90dB
  - Dynamic Range, S/N: 100dB
  - Soft Mute
- High Jitter Tolerance
- Master Clock: 256fs, 384fs, 512fs
- X' tal Oscillation circuit
- Master/Slave Mode
- Analog Power Supply: 4.5 to 5.5V, Digital Power Supply: 3.1 to 5.5V



■ Ordering Guide

AK4525VF                      -40 ~ +85°C                      28pin VSOP (0.65mm pitch)  
 AKD4525                      Evaluation Board for AK4525

■ Pin Layout



■ Difference with AK4522 and AK4523

	AK4522	AK4523	AK4525
Crystal Oscillator	Not available	Not available	Available
Master Mode	Not available	Not available	Available
Digital Power Supply	2.7 ~ 5.5V	3.0 ~ 5.5V	3.1 ~ 5.5V
Ambient Operating	-10 ~ 70°C	-40 ~ 85°C	-40 ~ 85°C
Package	24pin VSOP	28pin VSOP	28pin VSOP

PIN/FUNCTION			
No.	Pin Name	I/O	Function
1	VREFH	I	Positive Voltage Reference Input Pin, VA Used as a positive voltage reference by ADC & DAC. VREFH should be connected externally to filtered VA.
2	AINR+	I	Rch Analog Positive Input Pin
3	AINR-	I	Rch Analog Negative Input Pin
4	AINL+	I	Lch Analog Positive Input Pin
5	AINL-	I	Lch Analog Negative Input Pin
6	VA	-	Analog Power Supply Pin
7	AGND	-	Analog Ground Pin
8	XTI	I	X'tal Input Pin
9	XTO	O	X'tal Output Pin
10	DIF0	I	Audio Data Interface Format 0 Pin
11	DIF1	I	Audio Data Interface Format 1 Pin
12	LRCK	I/O	Input/Output Channel Clock Pin
13	SCLK	I/O	Audio Serial Data Clock Pin
14	SDTI	I	Audio Serial Data Input Pin
15	SDTO	O	Audio Serial Data Output Pin
16	SMUTE	I	Soft Mute Pin When this pin goes "H", soft mute cycle is initiated. When returning "L", the output mute releases.
17	DEM0	I	De-emphasis Frequency Select 0 Pin
18	DEM1	I	De-emphasis Frequency Select 1 Pin
19	TST	I	Test Pin This pin must be connected to DGND.
20	M/S	I	Master/Slave Mode "H": Master mode, "L": Slave mode (Internal pull-down pin)
21	MCKO	O	Master Clock Output Pin
22	VD	-	Digital Power Supply Pin
23	DGND	-	Digital Ground Pin
24	PDN	I	Power-Down Mode Pin
25	CMODE	I	Master Clock Select Pin "H": 384fs, "L": 256fs, "NC": 512fs (Internal biased pin)
26	AOUTL	O	Lch Analog Output Pin
27	AOUTR	O	Rch Analog Output Pin
28	VCOM	O	Common Voltage Output Pin, VA/2

Note: All input pins except pull-down or biased pins should not be left floating.

<b>ABSOLUTE MAXIMUM RATINGS</b>
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(AGND, DGND=0V; Note 1)

Parameter		Symbol	min	max	Units
Power Supplies	Analog	VA	-0.3	6.0	V
	Digital	VD	-0.3	6.0	V
	AGND-DGND  (Note 2)	$\Delta$ GND	-	0.3	V
Input Current, Any Pin Except Supplies		IIN	-	$\pm$ 10	mA
Analog Input Voltage		VINA	-0.3	VA+0.3	V
Digital Input Voltage		VIND	-0.3	VD+0.3	V
Ambient Temperature (power applied)		Ta	-40	85	°C
Storage Temperature		Tstg	-65	150	°C

- Notes: 1. All voltages with respect to ground.  
2. AGND and DGND must be same voltage.

WARNING: Operation at or beyond these limits may result in permanent damage to the device.  
Normal operation is not guaranteed at these extremes.

<b>RECOMMENDED OPERATING CONDITIONS</b>
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(AGND, DGND=0V; Note 1)

Parameter		Symbol	min	typ	max	Units
Power Supplies (Note 3)	Analog	VA	4.5	5.0	5.5	V
	Digital	VD	3.1	5.0	VA	V

- Notes: 1. All voltages with respect to ground.  
3. The power up sequence between VA and VD is not critical.

\*AKM assumes no responsibility for the usage beyond the conditions in this datasheet.

<b>ANALOG CHARACTERISTICS</b>
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(Ta=25°C; VA, VD=5.0V; AGND=DGND=0V; VREFH=VA; fs=44.1kHz; SCLK=64fs;

Signal Frequency =1kHz; 20bit Data; Measurement frequency = 10Hz ~ 20kHz; unless otherwise specified)

Parameter		min	typ	max	Units
<b>ADC Analog Input Characteristics: Differential Inputs; Analog Source Impedance=470Ω</b>					
Resolution				20	Bits
S/(N+D)	(-0.5dB Input) (Note 4)	84	92		dB
DR	(-60dB Input, A-Weighted) (Note 5)	94	100		dB
S/N	(A-Weighted) (Note 5, 6)	94	100		dB
Interchannel Isolation		90	110		dB
Interchannel Gain Mismatch			0.1	0.3	dB
Gain Drift			20		ppm/°C
Input Voltage	(AIN=0.6 x VREFH) (Note 7)	2.85	3.0	3.15	Vpp
Input Resistance		15	25		kΩ
Power Supply Rejection	(Note 8)		50		dB
<b>DAC Analog Output Characteristics:</b>					
Resolution				20	Bits
S/(N+D)		80	90		dB
DR	(-60dB Output, A-Weighted) (Note 5)	94	100		dB
S/N	(A-Weighted) (Note 6, 9)	94	100		dB
Interchannel Isolation		90	110		dB
Interchannel Gain Mismatch			0.2	0.5	dB
Gain Drift			20	-	ppm/°C
Output Voltage	(AOUT=0.58 x VREFH)	2.65	2.9	3.15	Vpp
Load Resistance		5			kΩ
Load Capacitance				25	pF
Power Supply Rejection	(Note 8)		50		dB
<b>Power Supplies VA=VD=5V</b>					
Analog, VA	PDN= "H"		40	55	mA
Digital, VD	PDN= "H"		12	20	mA
Power Down	PDN= "L" (Note 10)		6	12	mA

- Notes:
4. In case of single ended input, S/(N+D)=80dB(typ, @VA=5V).
  5. In case of 16bit, DR and S/N of ADC are 98dB. DR of DAC is 98dB.
  6. S/N measured by CCIR-ARM is 96dB at each converter and 94dB at ADC to DAC loopback.
  7. Full scale input for each AIN+/- pin is 1.5Vpp in differential mode.
  8. PSR is applied to VA, VD with 1kHz, 50mVpp. VREFH pin is held a constant voltage.
  9. As the input data is "0", S/N is 100dB regardless of resolution.
  10. X'tal circuit is oscillating and all digital input pins are held VD or DGND.

FILTER CHARACTERISTICS							
(Ta=25°C; VA=4.5 ~ 5.5V; VD=3.1 ~ 5.5V; DEM0= "1", DEM1= "0")							
Parameter	Symbol	min	typ	max	Units		
<b>ADC Digital Filter (Decimation LPF):</b>							
Passband (Note 11)	-0.005dB	PB	0		19.76	kHz	
	-0.02dB		0		20.02	kHz	
	-0.06dB		0		20.20	kHz	
	-6.0dB		0		22.05	kHz	
Stopband	SB	24.34				kHz	
Passband Ripple	PR			±0.005		dB	
Stopband Attenuation	SA	80				dB	
Group Delay (Note 12)	GD		29.3			1/fs	
Group Delay Distortion	ΔGD		0			μs	
<b>ADC Digital Filter (HPF):</b>							
Frequency Response (Note 11)	-3dB	FR		0.9		Hz	
	-0.5dB			2.7		Hz	
	-0.1dB			6.0		Hz	
<b>DAC Digital Filter:</b>							
Passband (Note 11)	-0.06dB	PB	0		20.0	kHz	
	-6.0dB		0		22.05	kHz	
Stopband	SB	24.1				kHz	
Passband Ripple	PR			±0.06		dB	
Stopband Attenuation	SA	43				dB	
Group Delay (Note 12)	GD		14.7			1/fs	
<b>DAC Digital Filter + Analog Filter:</b>							
Frequency Response:	0 ~ 20.0kHz	FR	-	±0.2	-	dB	

Notes: 11. The passband and stopband frequencies scale with fs.

For example, 20.02kHz at -0.02dB is 0.454 x fs. The reference frequency of these responses is 1kHz.

12. The calculating delay time which occurred by digital filtering. This time is from the input of analog signal to setting the 20bit data of both channels to the output register for ADC.

For DAC, this time is from setting the 20bit data of both channels on input register to the output of analog signal.

DC CHARACTERISTICS						
(Ta=25°C; VA=4.5 ~ 5.5V; VD=3.1 ~ 5.5V)						
Parameter	Symbol	min	typ	Max	Units	
High-Level Input Voltage (Except CMODE pin)	VIH	70%VD	-	-	V	
Low-Level Input Voltage (Except CMODE pin)	VIL	-	-	30%VD	V	
High-Level Input Voltage (CMODE pin)	VIH	95%VD	-	-	V	
Low-Level Input Voltage (CMODE pin)	VIL	-	-	10%VD	V	
High-Level Output Voltage (Iout=-80μA)	VOH	VD-0.4	-	-	V	
Low-Level Output Voltage (Iout=80μA)	VOL	-	-	0.4	V	
Input Leakage Current (Note 14)	Iin	-	-	±10	μA	

Notes: 14. CMODE pin has internal pull-up and pull-down devices, nominally 50kohm.

M/S pin has internal pull-down device, nominally 46kohm.

SWITCHING CHARACTERISTICS					
(Ta=25°C; VA=4.5 ~ 5.5V; VD=3.1 ~ 5.5V; CL=20pF)					
Parameter	Symbol	min	typ	max	Units
<b>Master Clock Timing</b>					
256fs		8.192		12.288	MHz
384fs		12.288		18.432	MHz
512fs		16.384		24.576	MHz
<b>MCKO Output</b>					
Frequency	fMCK	8.192		24.576	MHz
Duty Cycle	dMCK		50		%
Rise Time	tR			5	ns
Fall time	tF			5	ns
<b>LRCK Timing</b>					
Frequency	fs	32		48	kHz
Duty Cycle	dfs	45		55	%
<b>Serial Interface Timing</b>					
<b>Slave mode</b>					
SCLK Period	tSCK	320			ns
SCLK Pulse Width Low	tSCKL	65			ns
Pulse Width High	tSCKH	65			ns
LRCK Edge to SCLK “↑”	tLRS	45			ns
SCLK “↑” to LRCK Edge	tSLR	45			ns
LRCK to SDTO (MSB)	tLRM			40	ns
SCLK “↓” to SDTO	tSSD			70	ns
SDTI Hold Time	tSDH	40			ns
SDTI Setup Time	tSDS	25			ns
<b>Master mode</b>					
SCLK Frequency	fSCK		64fs		Hz
SCLK Duty	dSCK		50		%
SCLK “↓” to LRCK	tMSLR	-20		20	ns
SCLK “↓” to SDTO	tSSD			70	ns
SDTI Hold Time	tSDH	40			ns
SDTI Setup Time	tSDS	25			ns
<b>Reset Timing</b>					
PDN Pulse Width	tPD	150			ns
PDN “↑” to SDTO valid	tPDV		516		1/fs

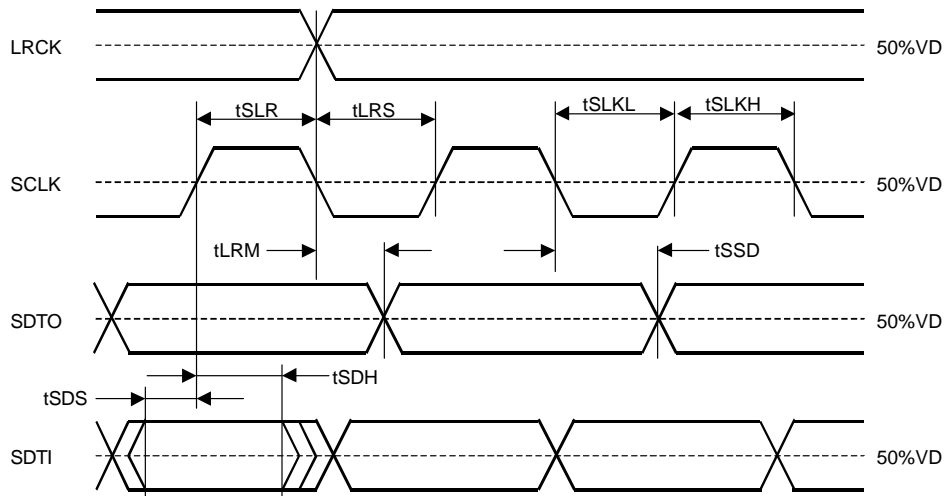
Notes: 15. VD=3.1V, 0.8 ~ 2.0V.

16. SCLK rising edge must not occur at the same time as LRCK edge.

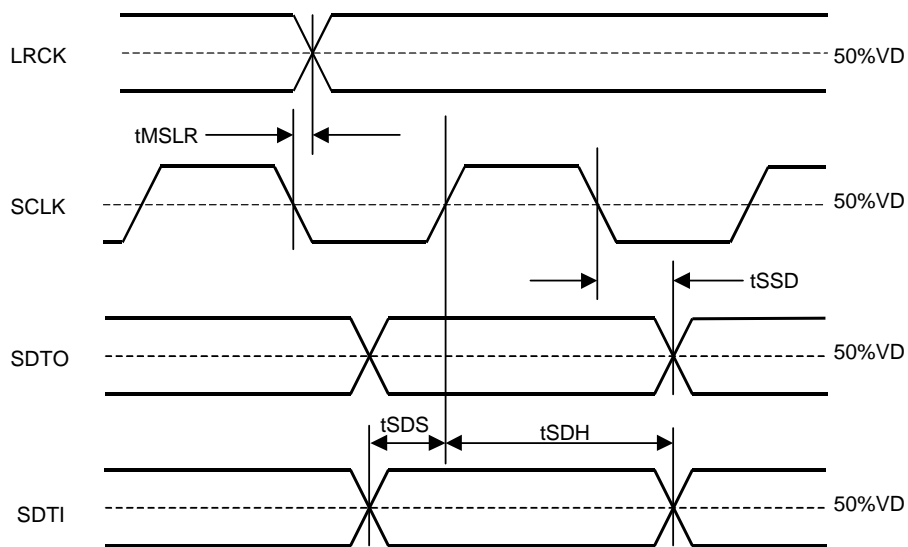
17. The AK4525 can be reset by bringing PDN “L”. When the state of CMODE changes during operation, the AK4525 should be reset by PDN. PDN should be held “L” for 5ms to allow the X’tal oscillation to begin at power-up.

18. These cycles are the number of LRCK rising from PDN rising.

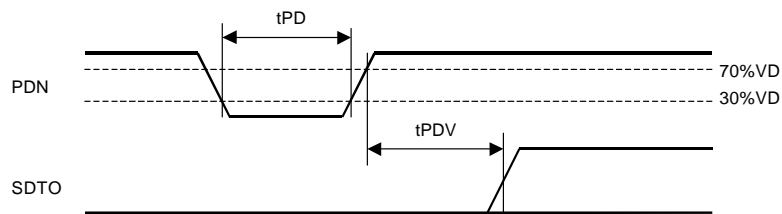
■ Timing Diagram



Serial Interface Timing (Slave mode)



Serial Interface Timing (Master mode)



Reset & Initialize Timing

## OPERATION OVERVIEW

### ■ System Clock

The master clock (MCLK) can be a crystal resonator placed across the XTI and XTO pin. The relationship between the MCLK and the desired sample rate is defined in Table 1. The MCLK frequency is set by CMODE pin and the sampling rate corresponds to 32kHz ~ 48kHz.

In slave mode, the LRCK clock input must be synchronized with MCLK, however the phase is not critical. Internal timing is synchronized to LRCK upon power-up. All external clocks must be present unless PDN= "L", otherwise excessive current may result from abnormal operation of internal dynamic logic.

fs	MCLK			SCLK
	256fs CMODE= "L"	384fs CMODE= "H"	512fs CMODE= "NC"	64fs
32.0kHz	8.1920MHz	12.2880MHz	16.3840MHz	2.0480MHz
44.1kHz	11.2896MHz	16.9344MHz	22.5792MHz	2.8224MHz
48.0kHz	12.2880MHz	18.4320MHz	24.5760MHz	3.0720MHz

Table 1. System Clock Example at normal speed

When the state of CMODE changes under operation, the AK4525 should be reset by PDN. At that case, the analog outputs should be muted externally because some click noise may occur.

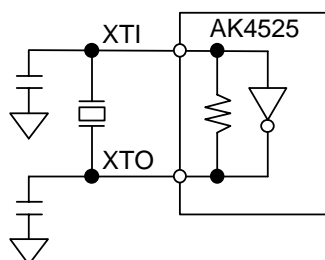


Figure 1. X'tal resonator connection

External loading capacitor (~ 22pF to AGND for XTI/XTO) are required for a crystal oscillator. PDN should be held "L" for 5ms to allow the X'tal oscillation to begin at power-up.

■ Audio Serial Interface Format

Data is shifted in/out the SDTI/SDTO pins using SCLK and LRCK inputs. The AK4525 supports the master mode. In this case, SCLK and LRCK are outputs and the frequency of SCLK is fixed to 64fs. Four serial data modes selected by the DIF0 and DIF1 pins are supported as shown in Table 3. In all modes the serial data has MSB first, 2's compliment format. The data is clocked out on the falling edge of SCLK and latched on the rising edge. For mode 3, if SCLK is 32fs, then the least significant bits will be truncated.

Mode	DIF1	DIF0	SDTO (ADC)	SDTI (DAC)	L/R	SCLK (Slave)
0	0	0	20bit, MSB justified	16bit, LSB justified	H/L	≥ 32fs
1	0	1	20bit, MSB justified	20bit, LSB justified	H/L	≥ 40fs
2	1	0	20bit, MSB justified	20bit, MSB justified	H/L	≥ 40fs
3	1	1	IIS (I2S)	IIS (I2S)	L/H	32fs or ≥ 40fs

Table 2. Serial Data Modes

Note: In master mode, SCLK frequency is fixed to 64fs.

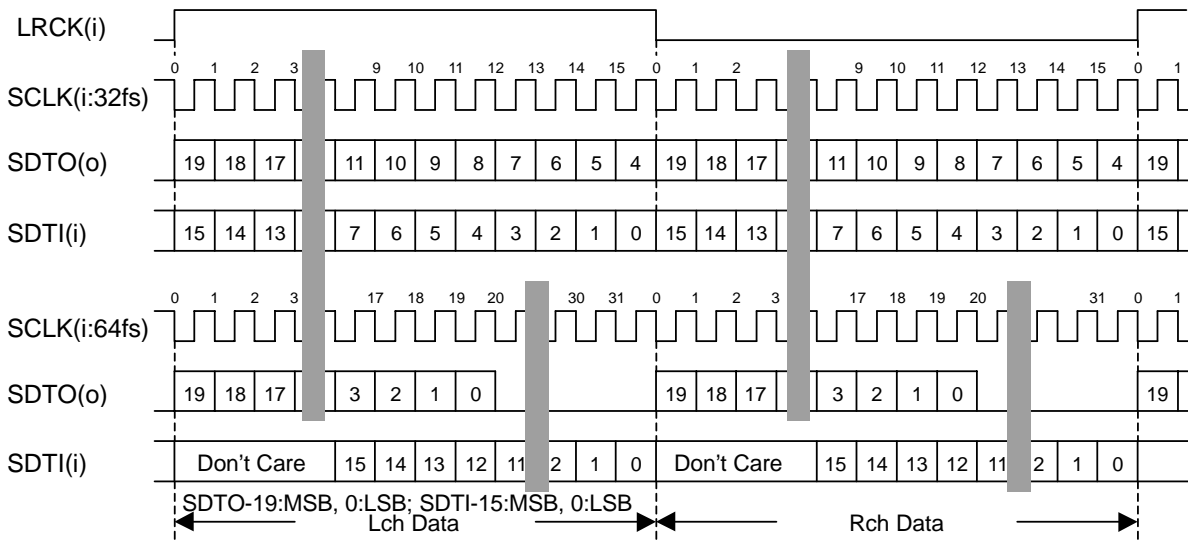


Figure 2. Mode 0 Timing

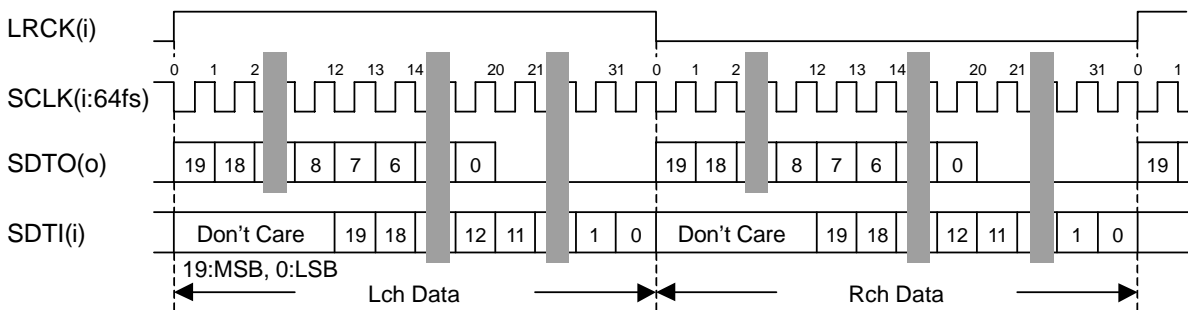


Figure 3. Mode 1 Timing

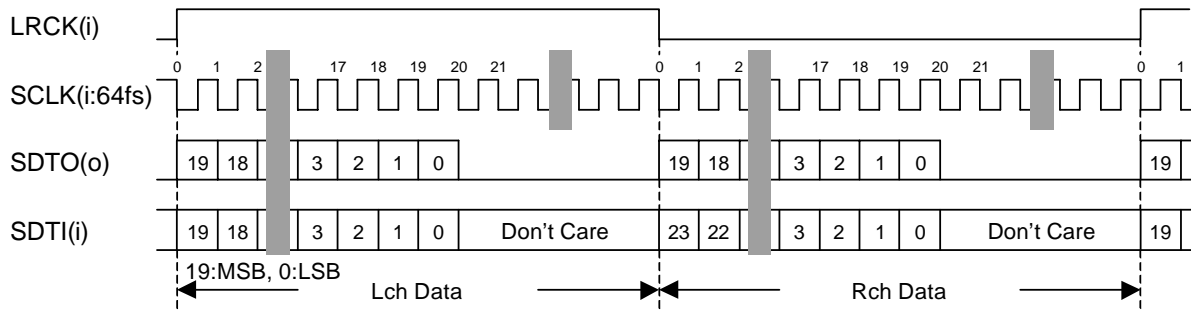


Figure 4. Mode 2 Timing

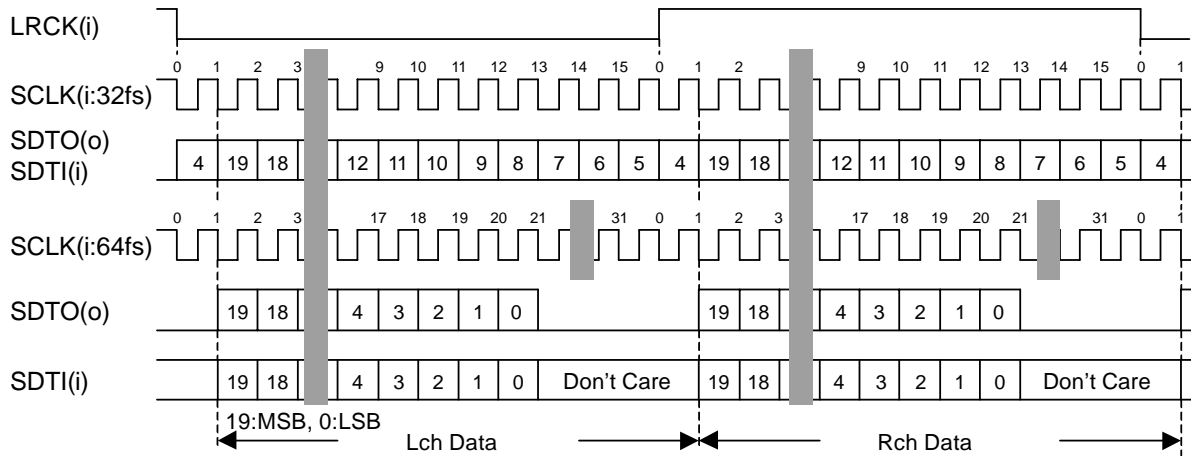


Figure 5. Mode 3 Timing

■ Digital High Pass Filter

The ADC of AK4525 has a digital high pass filter for DC offset cancel. The cut-off frequency of the HPF is 0.9Hz at  $f_s=44.1\text{kHz}$  and also scales with sampling rate (fs).

## ■ De-emphasis Filter

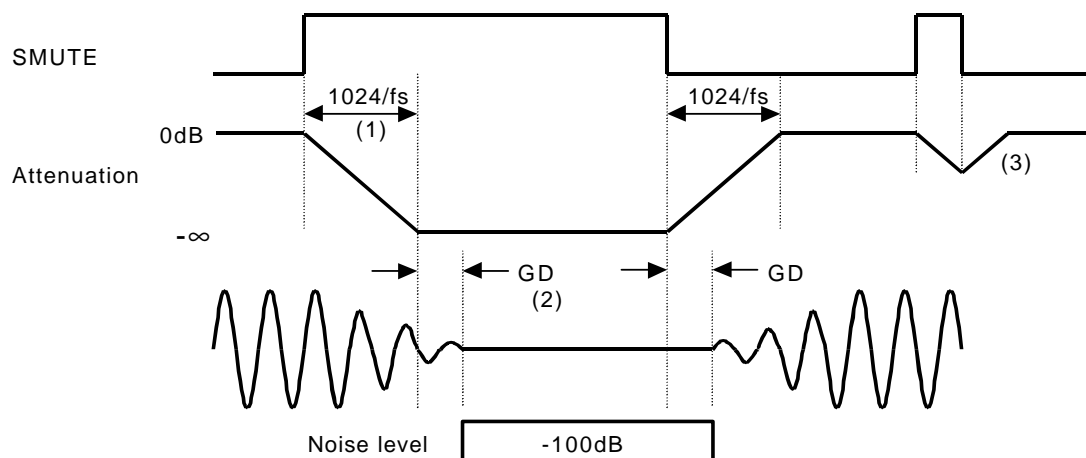
The DAC of AK4525 includes the digital de-emphasis filter ( $t_c=50/15\mu s$ ) by IIR filter. This filter corresponds to three frequencies (32kHz, 44.1kHz and 48kHz). The de-emphasis filter selected by DEM0 and DEM1 is enabled for input audio data. The de-emphasis is also disabled at DEM0= "1" and DEM1= "0".

DEM1	DEM0	Mode
0	0	44.1kHz
0	1	OFF
1	0	48kHz
1	1	32kHz

Table 3. De-emphasis filter control

## ■ Soft Mute Operation

Soft mute operation is performed at digital domain. When SMUTE goes to "H", the output signal is attenuated by  $-\infty$  during 1024 LRCK cycles. When SMUTE is returned to "L", the mute is cancelled and the output attenuation gradually changes to 0dB during 1024 LRCK cycles. If the soft mute is cancelled within 1024 LRCK cycles after starting the operation, the attenuation is discontinued and returned to 0dB. The soft mute is effective for changing the signal source without stopping the signal transmission.



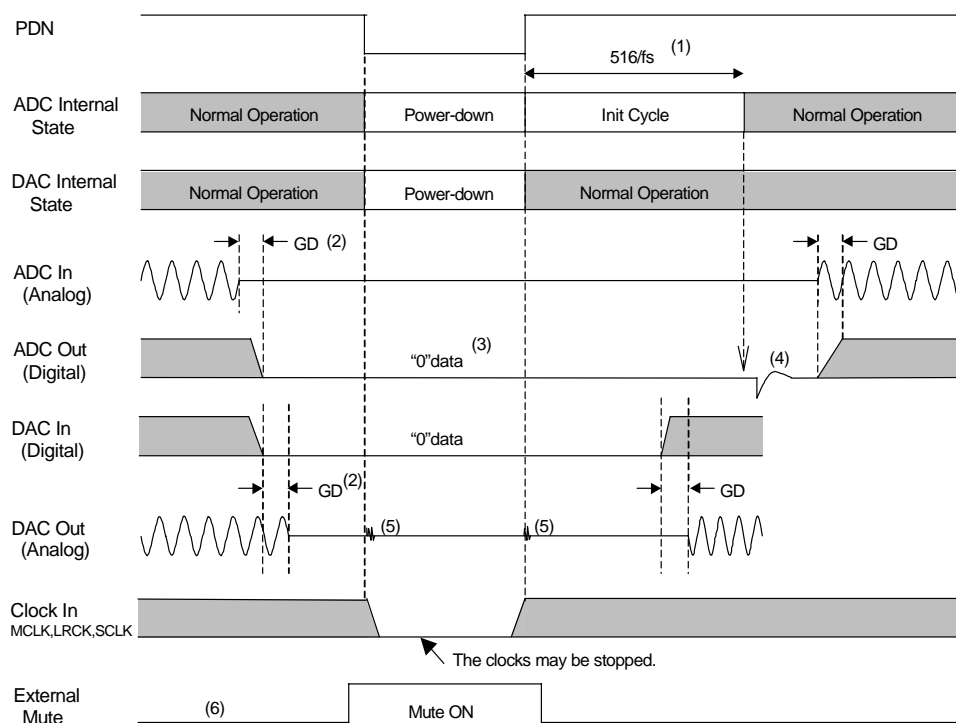
Notes:

- (1) The output signal is attenuated by  $-\infty$  during 1024 LRCK cycles ( $1024/f_s$ ).
- (2) Analog output corresponding to digital input has the group delay (GD).
- (3) If the soft mute is cancelled within 1024 LRCK cycles, the attenuation is discontinued and returned to 0dB.

Figure 6. Soft Mute Operation

## ■ Power-Down & Reset

The ADC and DAC of AK4525 are placed in the power-down mode by bringing a power down pin, PDN “L” and each digital filter is also reset at the same time. This reset should always be done after power-up. In case of the ADC, an analog initialization cycle starts after exiting the power-down mode. Therefore, the output data, SDTO becomes available after 516 cycles of LRCK clock. This initialization cycle does not affect the DAC operation. Figure 7 shows the power-up sequence.



- (1) The analog part of ADC is initialized after exiting the power-down state.
- (2) Digital output corresponding to analog input and analog output corresponding to digital input have the group delay (GD).
- (3) ADC output is “0” data at the power-down state.
- (4) Small click noise occurs at the end of initialization of the analog part. Please mute the digital output externally if the click noise influences system application.
- (5) Click noise occurs at the edge of PDN.
- (6) Please mute the analog output externally if the click noise (5) influences system application.

Figure 7. Power-up Sequence

During the power-down mode, the crystal oscillator is left running. The condition of the outputs are as follows.

SDTO = “L”  
 MCKO = Clock out  
 LRCK = “H” (master mode)  
 SCLK = “L” (master mode)  
 AOUT = VCOM (VA/2)



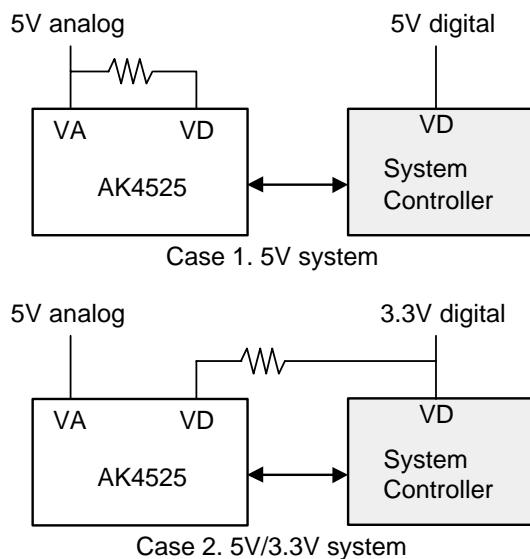


Figure 10. Power Supply Arrangement

## 1. Grounding and Power Supply Decoupling

The AK4525 requires careful attention to power supply and grounding arrangements. VA and VD are usually supplied from analog supply in system. Alternatively if VA and VD are supplied separately, the power up sequence is not critical. AGND and DGND of the AK4525 should be connected to analog ground plane. System analog ground and digital ground should be connected together near to where the supplies are brought onto the printed circuit board. Decoupling capacitors should be as near to the AK4525 as possible, with the small value ceramic capacitor being the nearest.

## 2. Voltage Reference

The differential voltage between VREFH and AGND sets the analog input/output range. VREFH pin is normally connected to VA with a 0.1 $\mu$ F ceramic capacitor. VCOM is a signal ground of this chip. An electrolytic capacitor 10 $\mu$ F parallel with a 0.1 $\mu$ F ceramic capacitor attached to VCOM pin eliminates the effects of high frequency noise. No load current may be drawn from VCOM pin. All signals, especially clocks, should be kept away from the VREFH and VCOM pins in order to avoid unwanted coupling into the AK4525.

## 3. Analog Inputs

The ADC inputs are differential and internally biased to the common voltage ( $VA/2$ ) with 25k $\Omega$  (typ) resistance. Figure 7 is a circuit example which analog signal is input by single end. The signal can be input from either positive or negative input and the input signal range scales with the supply voltage and nominally 0.6 x VREFH Vpp. In case of single ended input, the distortion around full scale degrades compared with differential input. Figure 11 is a circuit example which analog signal is input to both positive and negative input and the input signal range scales with the supply voltage and nominally 0.3 x VREFH Vpp. The AK4525 can accept input voltages from AGND to VA. The ADC output data format is 2's complement. The output code is 7FFFFH(@20bit) for input above a positive full scale and 80000H(@20bit) for input below a negative full scale. The ideal code is 00000H(@20bit) with no input signal. The DC offset is removed by the internal HPF.

The AK4525 samples the analog inputs at 64fs. The digital filter rejects noise above the stop band except for multiples of 64fs. A simple RC filter ( $f_c=150$ kHz) may be used to attenuate any noise around 64fs and most audio signals do not have significant energy at 64fs.

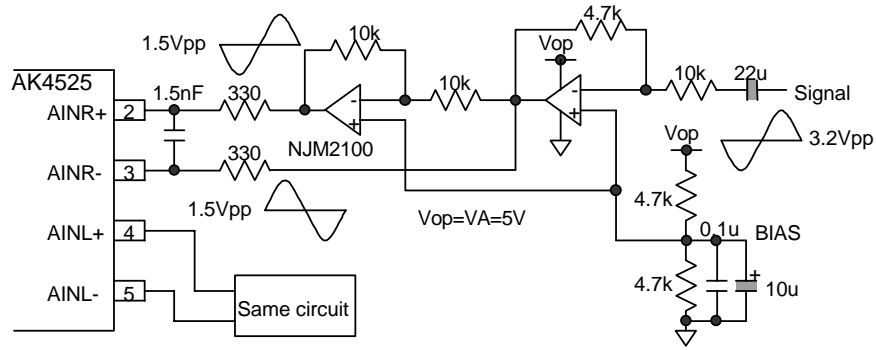


Figure 11. Differential Input Buffer Example

**4. Analog Outputs**

The analog outputs are also single-ended and centered around the VCOM voltage. The input signal range scales with the supply voltage and nominally  $0.58 \times VREFH$  Vpp. The DAC input data format is 2's complement. The output voltage is a positive full scale for 7FFFH(@20bit) and a negative full scale for 8000H(@20bit). The ideal output is VCOM voltage for 0000H(@20bit). The internal switched-capacitor filter and continuous-time filter remove most of the noise generated by the delta-sigma modulator of DAC beyond the audio passband.

DC offsets on analog outputs are eliminated by AC coupling since DAC outputs have DC offsets of a few mV. Figure 12 shows the example of external op-amp circuit with 6dB gain. The output signal is inverted by using the circuit in this case.

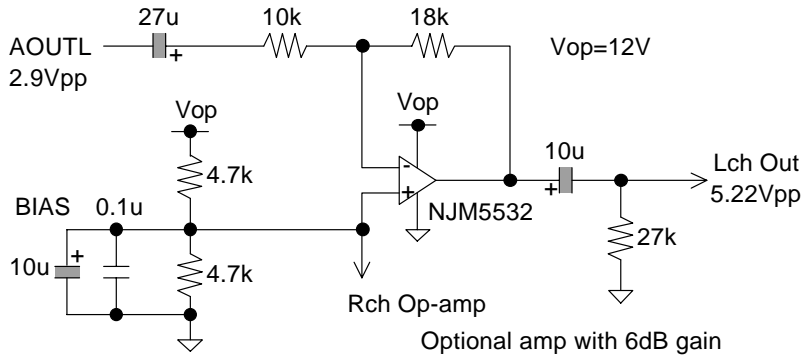
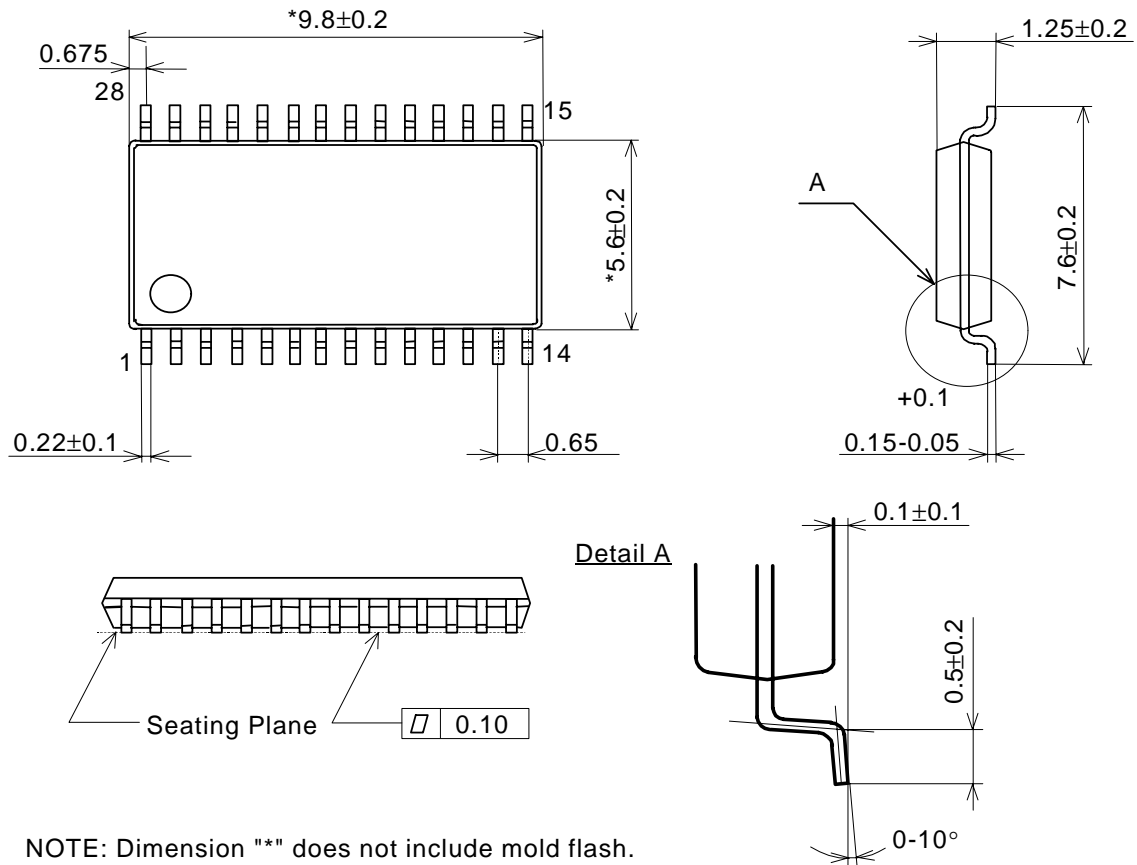


Figure 12. External analog circuit example (gain=6dB)

**PACKAGE**

**28pin VSOP (Unit: mm)**

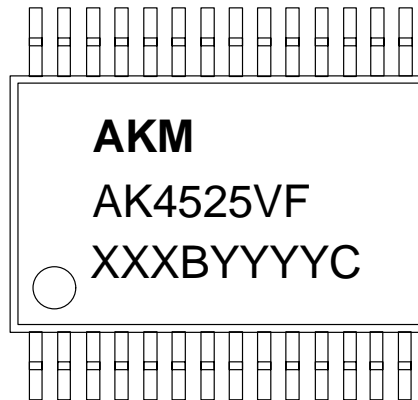


NOTE: Dimension "\*" does not include mold flash.

■ **Material & Lead finish**

Package molding compound:	Epoxy
Lead frame material:	Cu
Lead frame surface treatment:	Solder plate

<b>MARKING</b>
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XXXBYYYYC    Date code identifier

XXXB :    Lot number (X : Digit number, B : Alpha character)

YYYYC :    Assembly date (Y : Digit number, C Alpha character)

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