AK4544A

AC' 97™ Multimedia Audio CODEC with SRC

Features

- **AC' 97 Rev. 2.1 Compliant**
- **18bit Resolution A/D and D/A**
- **Exceeds PC99 Performance Requirements:**
  - **AK4544A (@fs=48k)**
  - **A/D……90dBA**
  - **D/A……89dBA**
  - **A-A……95dBA**
- **Analog Inputs:**
  - **4 Stereo Inputs: LINE, CD, VIDEO, AUX**
  - **Speakerphone and PC BEEP Inputs**
  - **2 Independent MIC Inputs**
- **Variable Sampling Rate Support**
  - **48k, 44.1k, 32k, 22.05k, 16k, 11.025k, 8k**
- **Analog Output:**
  - **Stereo LINE Output with volume control**
  - **True Line Level with volume control**
  - **Mono Output with volume control**
- **3D Stereo Enhancement**
- **POP Function & DAC Feed Back Control**
- **Multiple codec Capability**
  - **The AK4544A can work as a Primary or Secondary codec depended on codec ID configuration.**
- **EAPD(External Amplifier Powerdown) Support**
- **Power Supplies: Analog 5.0V, Digital 5.0V or 3.3V**
- **Low Power Consumption**
  - **230mW(Analog:5V/Digital:3.3V) at full operation**
- **48 Pin LQFP Package**

General Description

The AK4544A is a 18bit high performance codec which support variable sampling rate conversion compliant with Audio Codec ' 97 Rev 2.1 requirements.

The AK4544A provides two pairs of stereo outputs with independent volume controls, a mono output, and multiple stereo and mono inputs, along with flexible mixing, gain and mute functions to provide a complete integrated audio solution for PCs. In addition, the AK4544A has the POP feature suitable for 3D positioning and direct output from DAC for AD monitoring or docking station application.

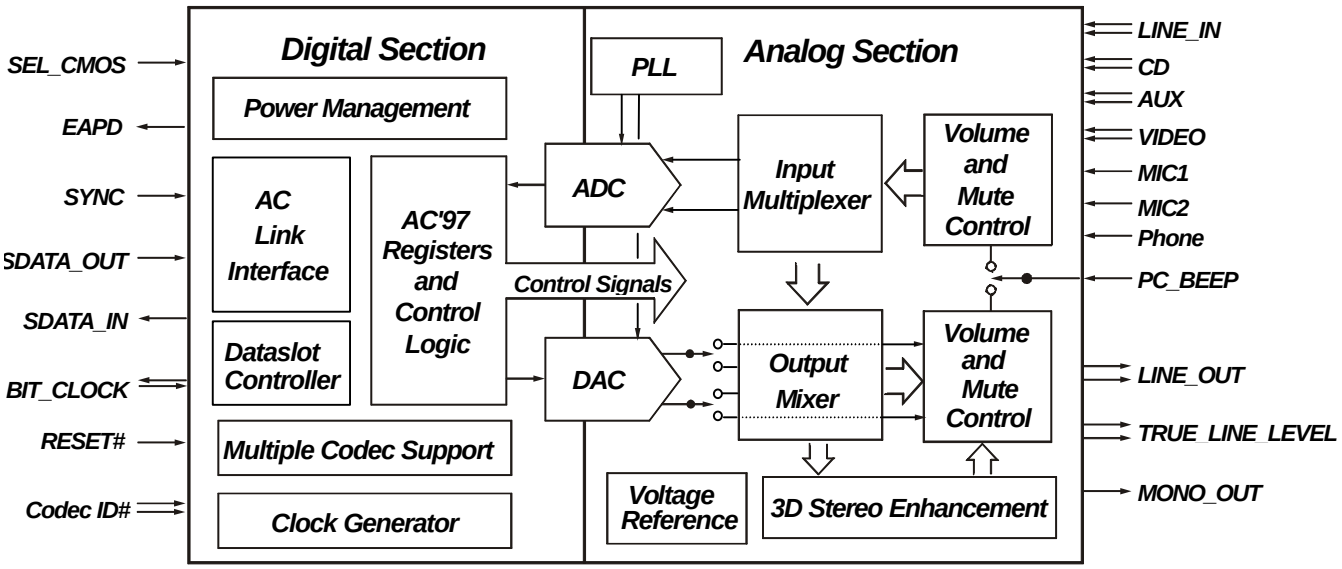
The AK4544A can function as a Primary AC' 97 or Secondary codec depending on the codec ID configuration(Multiple codec extension), making the AK4544A suitable for the docking station application and multiple codec applications.

Sampling frequency is programmable through AC-link as 48k, 44.1k, 32k, 22.05k, 16k, 11.025k, and 8kHz. This setting is done independent to ADC and DAC side while L/R channels are kept identical.

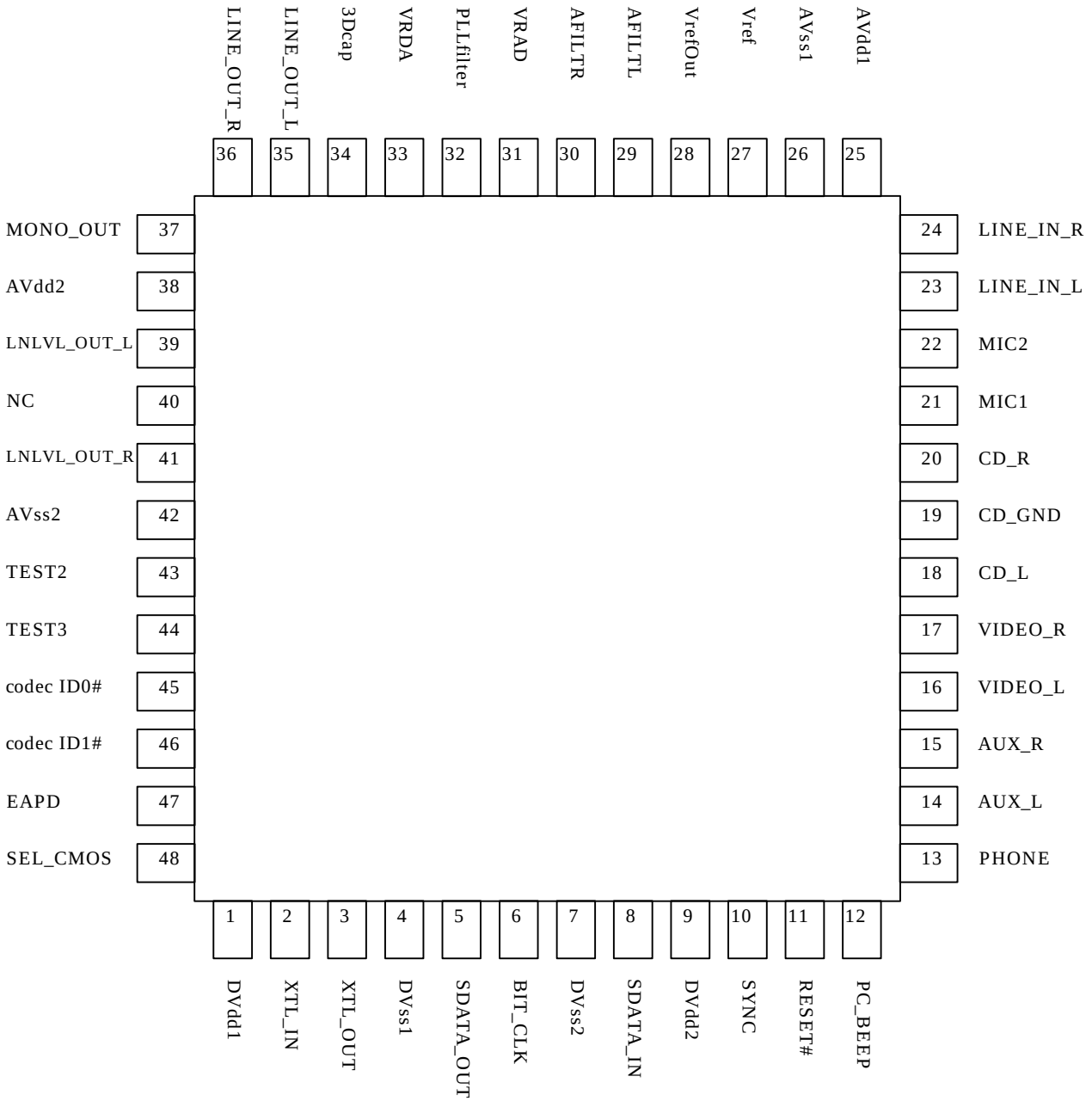
The AK4544A provides excellent audio performance, meeting or exceeding PC99 requirements for a PCI audio solution. It has low power consumption, and flexible power-down modes for use in laptops as well as desktop PCs and aftermarket add-in boards.

Like the earlier pin-compatible AK4540, AK4541, AK4542, and AK4543, the AK4544A is available in a compact 48-lead LQFP package.
Reference : Audio Codec ' 97 Revision 2.1

■ Block Diagram



* AKM assumes no responsibility for the usage beyond the conditions in this data sheet.


LINE_OUT_R 36
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VRAD 31
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LNLVL_OUT_R 41
AVss2 42
TEST2 43
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EAPD 47
SEL_CMOS 48
24 LINE_IN_R
23 LINE_IN_L
22 MIC2
21 MIC1
20 CD_R
19 CD_GND
18 CD_L
17 VIDEO_R
16 VIDEO_L
15 AUX_R
14 AUX_L
13 PHONE
1 DVdd1
2 XTL_IN
3 XTL_OUT
4 DVss1
5 SDATA_OUT
6 BIT_CLK
7 DVss2
8 SDATA_IN
9 DVdd2
10 SYNC
11 RESET#
12 PC_BEEP

Pin/Function

No.	Signal Name	I/O	Description
1	DVdd1	-	Digital power supply; 3.3V or 5.0V(DVdd1 = DVdd2) 0.1uF + 4.7uF capacitors should be connected to digital ground.
2	XTL_IN (MCLKI)	I	24.576MHz(512fs) Crystal is normally connected. If crystal is not connected, external clock can be used.
3	XTL_OUT(open)	O	24.576MHz(512fs) Crystal. If external clock is used, this pin should be open.
4	DVss1	-	Digital Ground; 0V. This pin should be directly connected to DVss2 on board.
5	SDATA_OUT	I	Serial 256-bit AC'97 data stream from digital controller
6	BIT_CLK	I/O	12.288MHz(256fs) serial data clock Output at Primary codec. Input at Secondary codec.
7	DVss2	-	Digital Ground; 0V. This pin should be directly connected to DVss1 on board.
8	SDATA_IN	O	Serial 256-bit AC'97 data stream to digital controller
9	DVdd2	-	Digital power supply; 3.3V or 5.0V(DVdd1 = DVdd2) 0.1uF + 4.7uF capacitors should be connected to digital ground.
10	SYNC	I	AC'97 Sync Clock, 48kHz(1fs) fixed rate sampling rate
11	RESET#	I	AC'97 Master Hardware Reset
12	PC_BEEP	I	PC Speaker beep pass through
13	PHONE	I	From telephony subsystem speakerphone
14	AUX_L	I	Aux Left Channel
15	AUX_R	I	Aux Right Channel
16	VIDEO_L	I	Video Audio Left Channel
17	VIDEO_R	I	Video Audio Right Channel
18	CD_L	I	CD Audio Left Channel
19	CD_GND	I	CD Audio analog ground CD_GND or analog ground should be connected through capacitor.
20	CD_R	I	CD Audio Right Channel
21	MIC1	I	Desktop Microphone Input
22	MIC2	I	Second Microphone Input
23	LINE_IN_L	I	Line In Left Channel
24	LINE_IN_R	I	Line In Right Channel
25	AVdd1	-	Power supply; 5.0V(AVdd1=AVdd2) 0.1uF + 4.7uF capacitors should be connected to AVss1(analog ground).
26	AVss1	-	Analog Ground; 0V
27	Vref	O	Reference Voltage Output; 0.1µF +4.7µF capacitors should be connected to Avss1(analog ground).
28	VrefOut	O	Reference Voltage Output (2.5V,1.25mA)
29	AFILTL	O	Anti-Aliasing Filter Cap; Connected to analog ground with 1nF capacitor.
30	AFILTR	O	Anti-Aliasing Filter Cap; Connected to analog ground with 1nF capacitor.
31	VRAD	O	Vref for ADC ; 0.1µF capacitor should be connected to analog ground.
32	PLLfilter	O	Loop filter for PLL is connected; 36k resistor and 33nF capacitor in series and 390pF capacitor.
33	VRDA	O	Vref for DAC; 0.1µF capacitor should be connected to analog ground.
34	3Dcap	O	3D Enhancement Cap; 27nF capacitor should be connected to analog ground.
35	LINE_OUT_L	O	Line Out Left Channel
36	LINE_OUT_R	O	Line Out Right Channel
37	MONO_OUT	O	To telephony subsystem speakerphone
38	AVdd2	-	Power supply; 5.0V(AVdd1=AVdd2) 0.1uF capacitor should be connected to AVss2(analog ground).
39	LNLVL_OUT_L	O	True Line Level Out Left Channel
40	NC	-	No Connection
41	LNLVL_OUT_R	O	True Line Level Out Right Channel
42	AVss2	-	Analog Ground
43	TEST2	I	Test pin (This pin should be open for normal operation):With internal pull-down.
44	TEST3	I	Test pin (This pin should be open for normal operation):With internal pull-down.
45	Codec ID0#	I	Codec ID configuration(ID select input for multiple codec extension) See Page21. Negative logic input. With internal pull-up.
46	Codec ID1#	I	Codec ID configuration(ID select input for multiple codec extension) See Page21. Negative logic input. With internal pull-up.

47	EAPD	O	EAPD(External amplified powerdown)
48	SEL_CMOS	I	CMOS/TTL selection for digital input levels. With internal pull-up. See Page 28. CMOS: Leave open for 3.3V supply. TTL : Tie to GND for 5V supply.

Absolute Maximum Rating

AVss1, AVss2, DVss1, DVss2 =0V (Note 1)

Parameter	Symbol	min	max	Units
Power Supplies (Note 2)				
Analog(AVdd1 & AVdd2)	VA	-0.3	6.0	V
Digital(DVdd1 & DVdd2)	VD	-0.3	6.0	V
Input Current (any pins except for supplies)	IIN	-	±10	mA
Analog Input Voltage	VINA	-0.3	VA+0.3	V
Digital Input Voltage	VIND	-0.3	VD+0.3	V
Ambient Temperature	Ta	-10	70	°C
Storage Temperature	Ta	-65	150	°C

Note 1: All voltages with respect to ground.
AGND(AVss1, AVss2) and DGND(DVss1, DVss2) should be same voltage.
Note 2: Supplying Digital Power, Analog Power should be supplied.

Warning: Operation at or beyond these limits may results in permanent damage to the device.
Normal operation is not guaranteed at these extremes.

Recommended Operating Condition

AGND, DGND=0V (Note 1)

Parameter		Symbol	min	typ	max	Units
Power Supplies	AK4544A					
	Analog	VA	4.75	5.0	5.25	V
	Digital	VD	3.135	5.0 or 3.3	5.25	V

Note 1 : All voltages with respect to ground.

AK4544A Analog Characteristics

Ta=25°C,AVdd=5.0V,DVdd=3.3V, fs=48kHz unless otherwise specified, Signal Frequency =1kHz
All volume setting for ADC/DAC performance measurement is 0dB.

Parameter	min	typ	max	Units
Audio-ADC				
Resolution			18	Bits
S/N (A weight, fs=48kHz)	83	90		dB
S/N (A weight, fs=44.1kHz)		87		dB
S/(N+D) (fs=48KHz, -1dB analog input)	70	77		dBFS
Inter Channel Isolation	70	77		dB
Inter Channel Gain Mismatch			0.5	dB
Full Scale Input Voltage	0.88	1.0	1.12	Vrms
Power Supply Rejection		50		dB
Audio DAC: measured at AOUTL/AOUTR via MIXER path				
Resolution			18	Bits
S/N (A weighted, fs=48kHz) : mixer+DAC measured at AOUT	84	89		dB
S/N (A weighted, fs=44.1kHz) : mixer+DAC measured at AOUT		86		dB
S/(N+D) (fs=48KHz, -1dB digital input)	72	80		dBFS
Inter Channel Isolation	70	80		dB
Inter Channel Gain Mismatch			1.0	dB
Full Scale Output Voltage	0.88	1.0	1.12	Vrms
Total Out-of-Band Noise (28.8kHz - 100kHz)		-70		dB
Power Supply Rejection		50		dB
MIC Amplifier / MUX				
Gain : 20dB is selected	18	20	22	dB
Master volume (Mono, Stereo, True Line Level Out) : 1.5dB x 32 step				
Step Size		-1.5		dB
Attenuation Control Range	-46.5		0	dB
Load Resistance	10			kΩ
PC Beep : 3dB x 16 step				
Step Size		-3.0		dB
Attenuation Control Range	-45		0	dB
Analog Mixer : 1.5dB x 32 step				
Step Size		-1.5		dB
Gain Control Range	-34.5		+12	dB
Record Gain : 1.5dB x 16 step				
Step Size		+1.5		dB
Gain Control Range	0		+22.5	dB
Mixer				
Input Voltage (except for MIC)		1.0		Vrms
Input Voltage MIC : Gain = 0dB MIC : Gain = 20dB		1 0.1		Vrms Vrms
S/N(A weighed) : 0dB setting, 1 path is selected at Mixer CD to AOUT: Other analog input to AOUT	88	 95 95		 dB dB
Input Impedance (Input gain=0dB,Rec_MUTE=off) PC_BEEP only Others(PHONE, LINE, CD, AUX, VIDEO) Input Impedance (MIC1 and MIC2)	 (10) (10) (10)	 76 40 20		 kΩ kΩ kΩ
Output load Resistance (LINE_OUT_L/R, MONO_OUT, LNLVL_OUT_L/R)	10			kΩ
Vrefout				
Drivability			1.25	mA

Parameter	min	typ	max	Units
Power Supplies				
Analog Power Supply Current(AVdd1 & AVdd2)				
All ON mode(all PR_bits are 0)		41	62	mA
Cold Reset status(Reset#=L, Vref is ON)		4.1	8	mA
All OFF mode(all PR_bits are 1)		0	0.2	mA
Digital Power Supply Current(DVdd1 & DVdd2)				
All ON mode(all PR_bits are 0) at DVDD=5V		13.5	21	mA
All ON mode(all PR_bits are 0) at DVDD=3.3V		7.5	11	mA
All OFF mode(all PR_bits are 1)		0	0.4	mA

Filter Characteristics

Ta=25°C,AVdd=5.0V±5%,DVdd=3.3V±5% , fs=48KHz(fixed)

Parameter	min	typ	Max	Units
ADC Digital Filter (Decimation LPF)				
Passband (±0.2dB) Note)	0		19.2	kHz
Stopband	28.8			kHz
Stopband Attenuation	70			dB
Group Delay			0.5	ms
ADC Digital Filter (HPF)				
Frequency Response; -3dB		7.5		Hz
-0.5dB		21		
-0.1dB		49		
DAC Digital Filter				
Passband (±0.2dB)	0		19.2	kHz
Stopband	28.8			kHz
Group Delay			0.5	ms
Stopband Rejection	70			dB
DAC Post filter				
Passband Frequency Response (0 - 19.2kHz)		±0.1		dB

Note) This frequency scales with the sampling frequency (fs).

AK4544A DC Characteristics

Ta=-10~70°C, VD=5V±5%(SEL_CMOS=L) or 3.3V±5%(SEL_CMOS=H: Open), VA=5V±5%, 50pF external load

Parameter	Symbol	min	typ	Max	Units
"H" level input voltage	VIH		-	-	
XTAL_IN		0.7xVD			V
RESET#, SYNC, SDATA_OUT, BIT_CLK					
At SEL_CMOS=L(GND) : TTL		2.2			V
At SEL_CMOS=H(Open) : CMOS		0.7xVD			V
ID0#, ID1#, SEL_CMOS(Pull up)		0.8xVD			V
"L" level input voltage	VIL	-	-		
XTAL_IN				0.3xVD	V
RESET#, SYNC, SDATA_OUT, BIT_CLK					
At SEL_CMOS=L(GND) : TTL				0.8	V
At SEL_CMOS=H(Open) : CMOS				0.3xVD	V
ID0#, ID1#, SEL_CMOS(Pull up)				0.2xVD	V
"H" level output voltage Iout= -1mA	VOH	VD-0.55	-	-	V
"L" level output voltage Iout= 1mA	VOL	-	-	0.55	V
Input leakage current(exclude pull up pins)	Iin	-	-	±10	μA
Pull up resistance	Rup	50	100	200	kΩ

Switching Characteristics

Ta=25°C, AVdd=5.0V±5%, DVdd=3.3V±5% or 5V±5%, 50pF external load

Parameter	Symbol	Min	Typ	max	Units
Master Clock Frequency Note)	Fmclk	-	24.576	-	MHz
If Crystal is not used.		45	50	55	%
AC link Interface Timing					
BIT_CLK frequency	Fbclk		12.288		MHz
BIT_CLK clock Period(Tbclk=1/Fbclk)	Tbclk	-	81.38		ns
BIT_BLK low pulse width	Tclk_low	36	40.7	45	ns
BIT_BLK low pulse width	Tclk_high	36	40.7	45	ns
BIT_CLK rise time	Trise_clk	-	-	6	ns
BIT_CLK fall time	Tfall_clk	-	-	6	ns
SYNC frequency		-	48	-	kHz
SYNC low pulse width	Tsync_low	-	19.5 (240 cycle)	-	µs (Tbclk)
SYNC high pulse width	Tsync_high	-	1.3 (16 cycle)	-	µs (Tbclk)
SYNC rise time	Trise_sync	-	-	6	ns
SYNC fall time	Tfall_sync	-	-	6	ns
Setup time(SYNC, SDATA_OUT)	Tsetup	10	-	-	ns
Hold time(SYNC, SDATA_OUT)	Thold	25	-	-	ns
SDATA_IN delay time from BIT_CLK rising edge	Tdelay	-	-	15	ns
SDATA_IN rise time	Trise_din	-	-	6	ns
SDATA_IN fall time	Tfall_din	-	-	6	ns
SDATA_OUT rise time	Trise_dout	-	-	6	ns
SDATA_OUT fall time	Tfall_dout	-	-	6	ns
Cold Rest (SDATA_OUT=L, SYNC=L)					
RESET# active low pulse width	Trst_low	1.0	-	-	µs
RESET# inactive to BIT_CLK delay	Trst2clk	162.8 (2 cycle)			ns (Tbclk)
Warm Rest Timing					
SYNC active low pulse width	Tsync_high	1.0	1.3 (16 cycle)	-	µs (Tbclk)
SYNC inactive to BIT_CLK delay	Tsync2clk	162.8 (2 cycle)			ns (Tbclk)
AC-link Low Power Mode Timing					
End of Slot 2 to BIT_CLK, SDATA_IN Low	Ts2_pdwn	-	-	1.0	µs
Activate Test Mode Timing					
Setup to trailing edge of RESET#	Tsetup2rst	15.0	-	-	ns
Hold from RESET# rising edge	Thold2rst	100	-	-	ns
Rising edge of RESET# to Hi-Z	Toff	-	-	50	ns
Falling edge of RESET# to "L"	Tlow	-	-	50	ns

Note) The use of a crystal is recommended. If master clock is supplied from controller (or if a external oscillator is used), Master Clock should be input to XTAL_IN, meanwhile XTAL_OUT should be open.

n Set ID for Multiple CODEC and CMOS/TTL

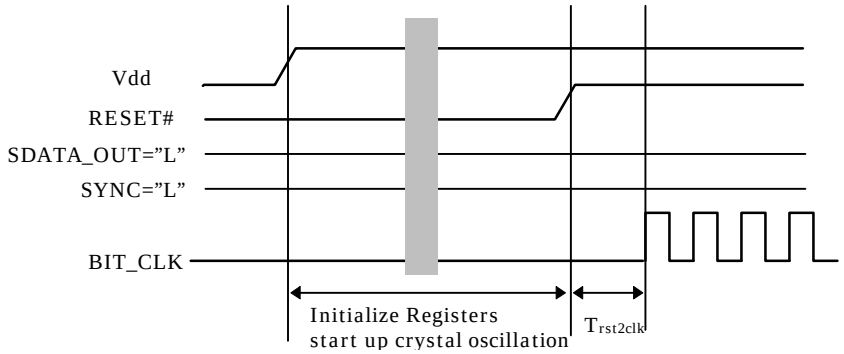
Before the device is power up, ID1# pin, ID0# pin and SEL_CMOS pin should be open or should be connected to DGND.

ID1 bit and ID0 bit are set by ID1# pin and ID0# pin that are 46 pin and 45 pin.
If both ID1# pin and ID0# pin are open, ID1 bit and ID0 bit in the extended audio register(28h) are stored as (0,0) respectively.

SEL_CMOS pin (48pin) decides which input level is CMOS or TTL.
If SEL_CMOS pin is open, CMOS input level is selected.
If SEL_CMOS pin is connected to DGND, TTL input level is selected.

n Power On

Note that AK4544A must be in cold reset at power on and RESET# must be low until master crystal clock becomes stable, or reset must be done once master clock is stable.



When using the AK4544A in multiple codec mode, all codec's connected to the AC-link are waken up at the same time.

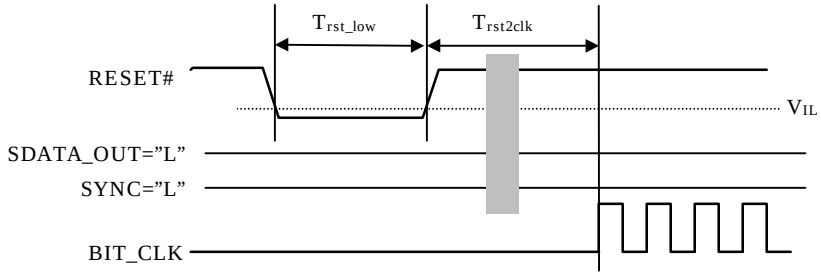
Secondary codec doesn't need the master clock of 24.576MHz. Then XTL_IN pin is low internally.
BIT_CLK signal of primary codec must be input into BIT_CLK pin of secondary CODEC. After AK4544A powers on, BIT_CLK mustn't stop except below case.

1) RESET#=L
2) PR0=PR1=PR4=1

nCold Reset Timing

Note that both SDATA_OUT and SYNC must be low at the rising edge of RESET# for cold reset.
The AK4544A initializes all registers including the Powerdown Control Registers, BIT-CLK is reactivated and each analog output is in Hi-Z state except for PC Beep while RESET# pin is low. **The PC Beep is directly routed to L & R line outputs when AK4544A is in Cold Reset.**
At the rising edge of RESET#, the AK4544A starts the initialization of ADC and DAC, which takes 1028TS cycles. After that, the AK4544A is ready for normal operation.

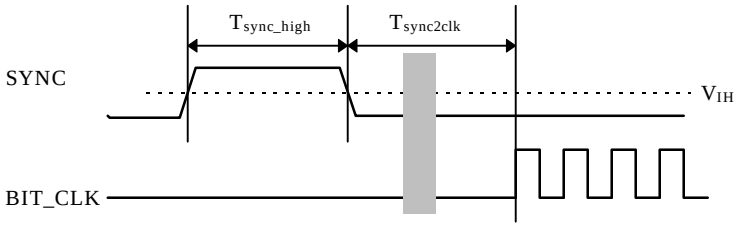
Status bit in the slot 0 is "0" (not ready) when the AK4544A is in RESET period ("L") or in initialization process. After initialization cycles, the status bit goes to "1" (ready).



When the AK4544A is used under the multiple codec configurations and when cold reset is issued, all AK4544A connected to the AC-link will execute a cold reset concurrently.

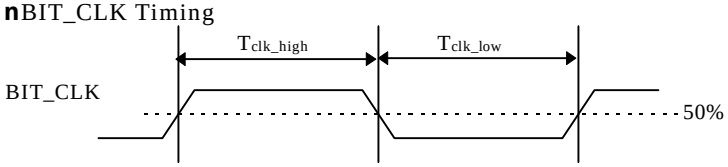
nWarm Reset

The AK4544A initiates warm reset process by receiving a single pulse on the sync. The AK4544A clears PR4 bit and PR5 bit in the Powerdown Control Register. However, warm reset does not influence PR0~PR3 or PR6,7 bits in Powerdown Control Register. Note that SYNC signal should synchronize with BIT_CLK after AK4544A starts to output BIT_CLK clock. And if an external clock is used, external clocks should be supplied before issuing a sync pulse for warm reset.
ADC and DAC require 1028TS for the initialization.

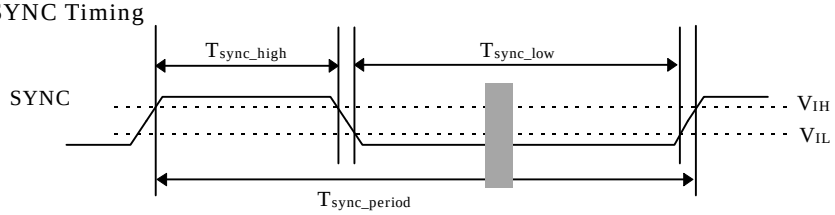


Please refer to the appendix on the warm reset when the AK4544A is used under the multiple codec configuration.

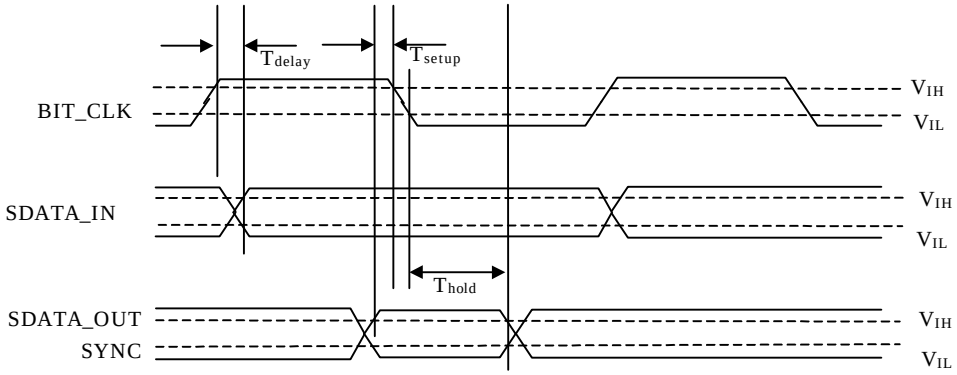
nBIT_CLK Timing



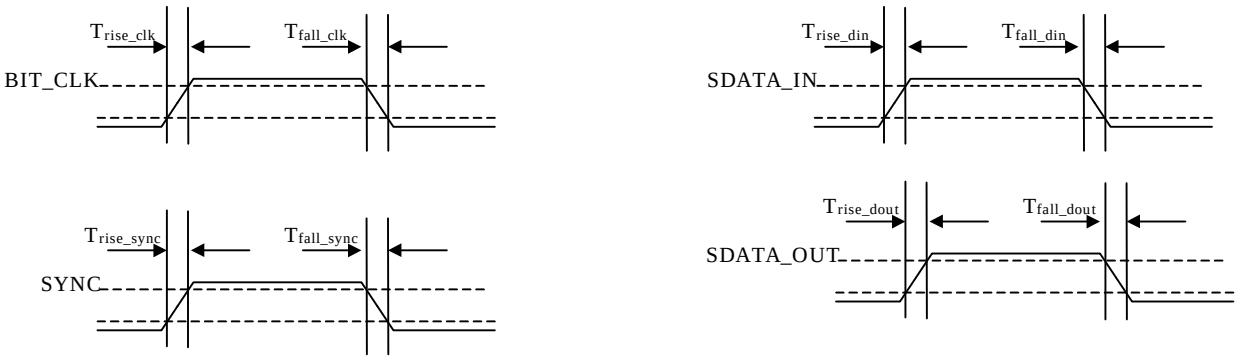
nSYNC Timing



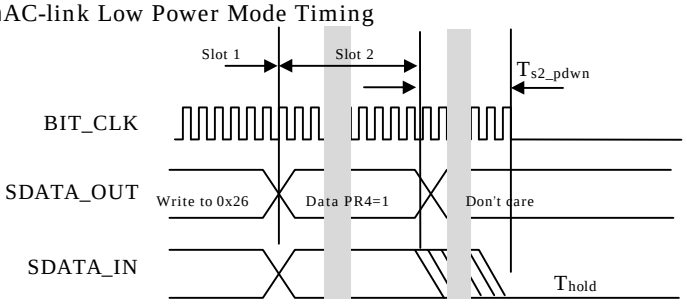
nSetup and Hold Timing



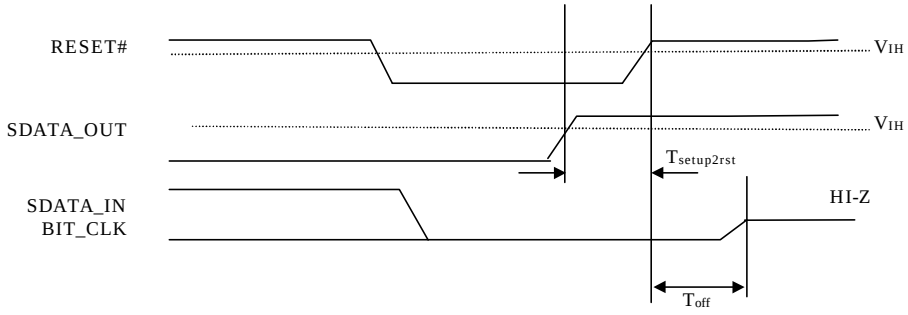
nSignal Rise and Fall Times
(50pF external load : from 10% 90% of DVdd)



nAC-link Low Power Mode Timing



nActivate Test Mode



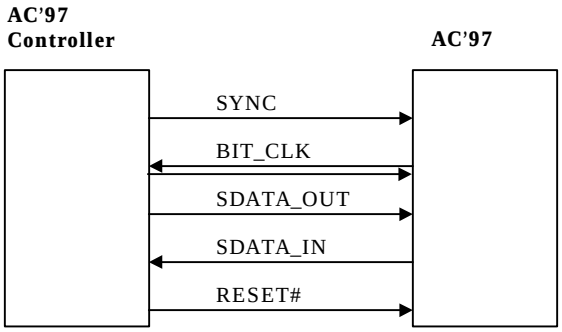
Notes:[1]
1. All AC-link signals are normally low through the trailing edge of RESET#. Bringing SDATA_OUT high for the rising edge of RESET# causes the AK4544A AC-link outputs to go high impedance which is suitable for ATE in circuit testing. Note that the AK4544A enters in the ATE test mode regardless SYNC is high or low.
2. Once test modes have been entered, the only way to return to the normal operating state is to issue "cold reset" which issues RESET# with both SYNC and SDATA_OUT low.

[1] All the following sentences written with small italic font in this document quote the AC' 97 component specification.

General Description

■ AC '97 Connection to the Digital AC '97 controller

[2]AC '97 communicates with its companion AC '97 controller via a digital serial link, AC-link". All digital audio streams, and command/status information are communicated over this point to point serial interconnect. A breakout of the signals connecting the two is shown in the following figure.



■ Digital Interface

The AK4544A incorporates a 5 pin digital serial interface that links it to the AC '97 controller. AC-link is a bi-directional, fixed rate(48kHz), serial PCM digital stream. It handles multiple input, and output audio streams, as well as control register accesses employing a time division multiplexed (TDM) scheme. The AC-link architecture divides each audio frame into 12 outgoing and 12 incoming data streams, each with 20-bit sample resolution. DAC and ADC resolution of the AK4544A is 18 bit resolution. The data streams currently defined by the AC '97 specification include:

l ***PCM Playback*** ***6 output slots(One codec can use 2 slots out of 6 slots)***
2 channel composite PCM output stream
l ***PCM Record data*** ***2 input slots***
2 channel composite PCM input stream
l ***Control*** ***2 output slot***
Control register write port
l ***Status*** ***2 input slots***
Control register read port

SYNC, fixed at 48 KHz, is derived by dividing down the serial bit clock (BIT_CLK). BIT_CLK, fixed at 12.288 MHz, provides the necessary clocking granularity to support 12, 20-bit outgoing and incoming time slots. AC-link serial data is transitioned on each rising edge of BIT_CLK. The receiver of AC-link data, the AK4544A for outgoing data and AC '97 controller for incoming data, samples each serial bit on the falling edges of BIT_CLK.
The AK4544A outputs BIT_CLK when it is assigned as Primary codec by codec ID configuration ID1# pin and ID0# pin. The other hand, the AK4544A receives BIT_CLK when assigned as the Secondary codec.
The AC-link protocol provides for a special 16-bit slot (Slot 0) wherein each bit conveys a valid tag for its corresponding time slot within the current audio frame. A "1" in a given bit position of slot 0 indicates that the corresponding time slot within the current audio frame has been assigned to a data stream, and contains valid data. If a slot is "Tagged" invalid, it is the responsibility of the source of the data, (The AK4544A for the input stream, AC '97 controller for the output stream), to stuff all bit positions with 0's during that slot's active time.
SYNC remains high for a total duration of 16 BIT_CLKs at the beginning of each audio frame. The portion of the audio frame where SYNC is high is defined as the "Tag Phase". The remainder of the audio frame where SYNC is low is defined as the "Data Phase".
Note that SDATA_OUT and SDATA_IN data is delayed one BIT_CLK because AC'97 controller causes SYNC signal high at a rising edge of BIT_CLK which initiates a frame.

"Output" stream means the direction from AC'97 controller to the AK4544A, and "Input" stream means the direction from the AK4544A to AC'97 controller

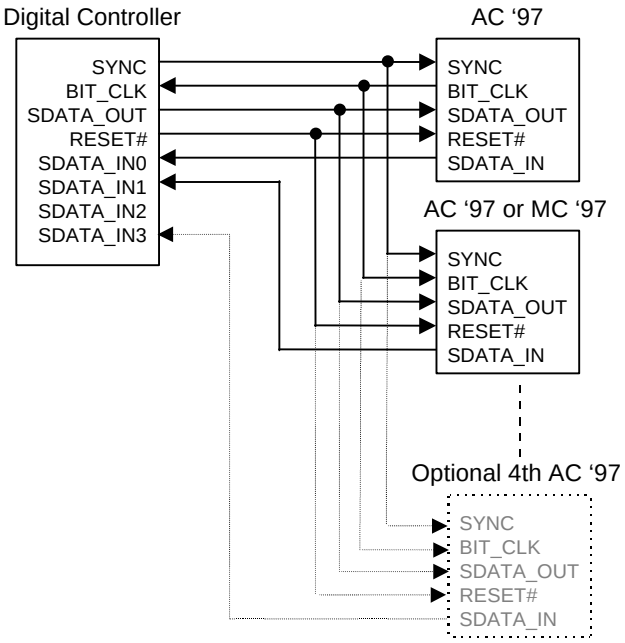
[2]All the following sentences written with small italic font in this document quote the AC' 97 component specification.

n **Multiple codec function**

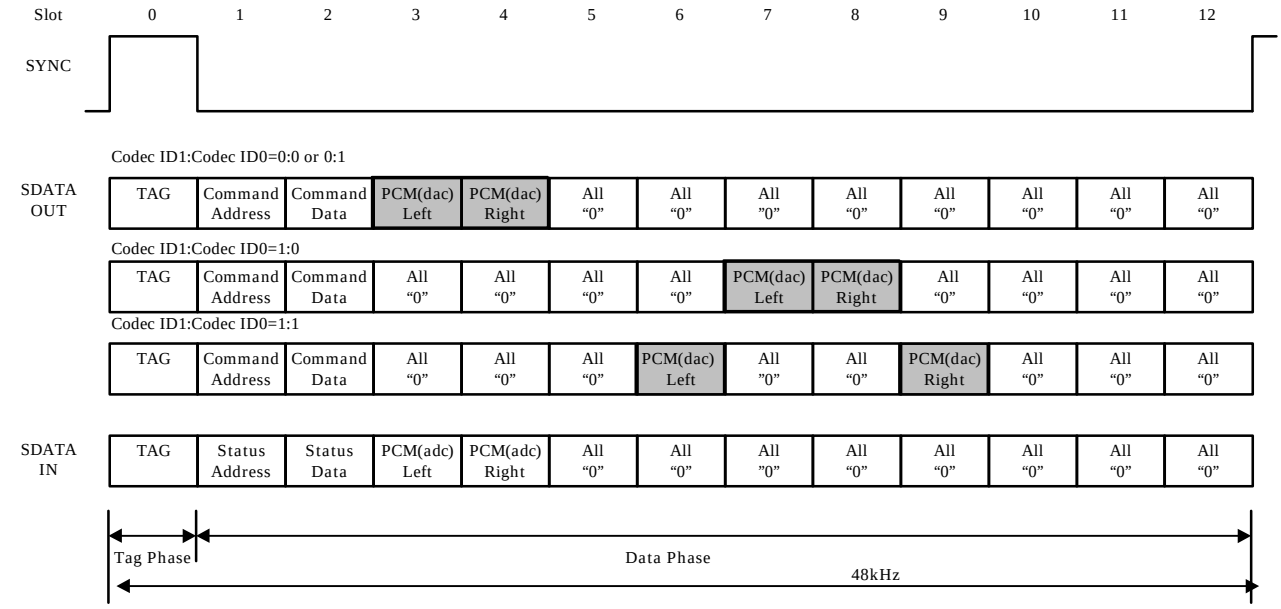
There can be up to 4 Codecs on the extended AC-link. The Primary Codec generates the master AC-link BIT_CLK for both the AC '97 Digital Controller and any Secondary Codecs. The AK4544A may be used as a master or slave in any systems using more than one codec.

ID for these 4 Codecs is set by combination of ID1# pin and ID0# pin. When AK4544A operates as primary codec, ID1# pin and ID0# pin must be open state before power on. In this case ID1 bit and ID0 bit in Extended Audio register are stored as (0,0) respectively. If either ID1# pin or ID0# pin is connected to DGND or both pins are connected to DGND, AK4544A operates as secondary codec.

The slot request bits of ID(0,1) CODEC are same as that of ID(0,0) CODEC. Therefore, note that all sample rates except 48KHz can't be used for DAC in the multiple CODEC system which secondary CODEC ID is (0,1).



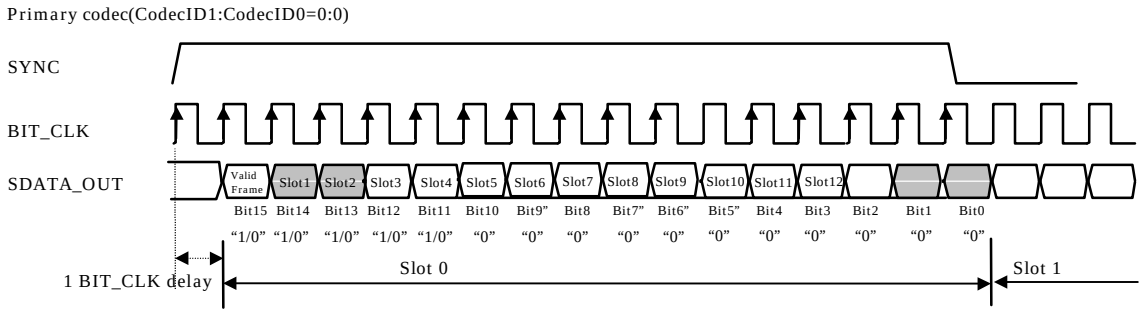
Multiple Codec Example

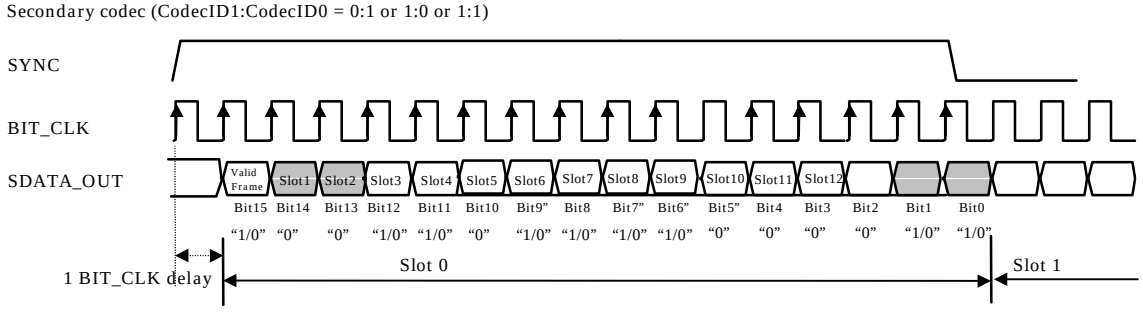


AC-link protocol identifies 13slots of data per frame. The frequency of sync is fixed to 48kHz. Only Slot 0, which is the Tag phase, is 16bits, all other slots are 20bits in length. These slots are explained in later sections.

AC-link Audio Output Frame (SDATA_OUT)

a)Slot 0





The AK4544A checks bit15 (valid frame bit). Note that when the valid frame bit is "1", at least one bit14-6 (slot 1-9) or bit1-0 must be valid, bit5-2 will be "0"and should be ignored.
If bit15 is "0", the AK4544A ignores all following information in the frame.
The AK4544A then checks the validity of each bit in the TAG phase (slot 0).
If each bit is "0", the AK4544A ignores the slot indicated by "0". On the other hand, if each bit is "1", the slot is valid.
All bits in slot10-12(bit5-3) are "0" and bit2 is also "0".
The AK4544A monitors bit1 and 0, which are codec ID configuration bits used in multiple codec designs. These bits are used to identify which codec the frame data is issued to.

When codec ID configuration bits1 and 0 which are set by codec ID configuration 45/46 strapping pins(codec ID0# pin and ID1# pin) are set to zero(00), the frame is aimed for the Primary codec. And when codec ID configuration bit1 and 0 are set to non-zero values(01, 10, or 11), the frame is meant for Secondary codec.

A new audio output frame begins with a low to high transition of SYNC. SYNC is synchronous to the rising edge of BIT_CLK. On the immediately following falling edge of BIT_CLK, the AK4544A samples the assertion of SYNC. This falling edge marks the time when both sides of AC-link are aware of the start of a new audio frame. On the next rising of BIT_CLK, the AC '97 controller transitions SDATA_OUT into the first bit position of slot 0 (Valid Frame bit). Each new bit position is presented to AC-link on a rising edge of BIT_CLK, and subsequently sampled by the AK4544A on the following falling edge of BIT_CLK. This sequence ensures that data transitions, and subsequent sample points for both incoming and outgoing data streams are time aligned.

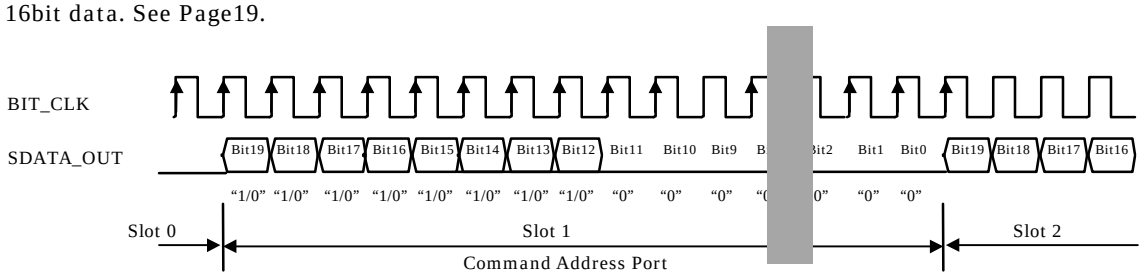
Data should be sent to the AC'97 codec with MSB first through the SDATA_OUT.

The following table shows the relationship of bit14&13 and the Read/Write operation depending on codec ID configuration.

Bit 15 Valid Frame	Bit 14: Slot1 Valid Bit (Command Address)	Bit 13: Slot 2 Valid Bit (Command Data)	Read/Write Operation of Primary AK4544A	Read/Write Operation of Secondary AK4544A
1	1	1	Read/Write(Normal Operation)	Ignore
1	0	1	Ignore	Ignore
1	1	0	Read: Normal Operation Write: Ignore	Ignore
1	0	0	Ignore	Read/Write(Normal Operation)

AK4544A Addressing: Slot0 Tag Bits

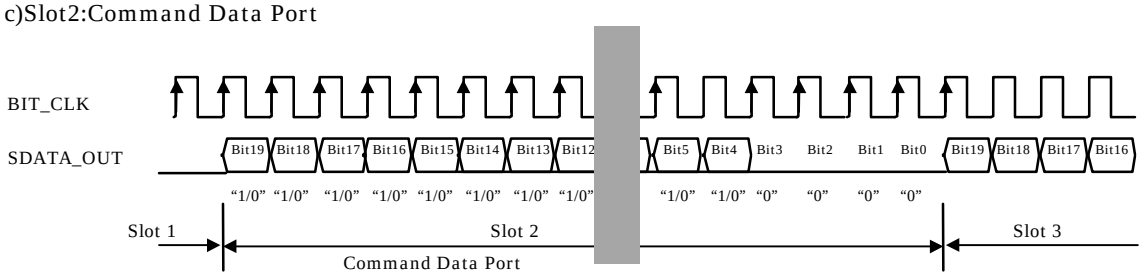
b)Slot1:Command Address Port
Slot1 gives the address of the command data, which is given in the slot 2. The AK4544A has 23 valid registers of 16bit data. See Page19.



Bit 19: Read/Write command 1=read, 0=write
Bit 18:12 Control Register Index (see "Mixer Registers for the detail)
Bit 11:0 Reserved ("0")

Bit 18 of this slot1 is equivalent to the most significant bit of the index register address.
The AK4544A ignores from bit11 to bit0. These bits will be reserved for future enhancement and must be staffed with 0's by the AC'97 controller.

c)Slot2:Command Data Port



Bit19:4 Control Register Write Data (if bit 19 of slot 1 is "1", all Bit19:4 should be "0")
Bit3:0 Reserved("0")

If bit19 in slot1 is "0", the AC'97 controller must output Command Data Port data in slot 2 ***of the same frame***. If the bit19 in slot1 is "1", the AK4544A will ignore any Command Data Port data in slot2.

Bit19 of this slot2 is equivalent to D15 bit of mixer register value.

d)Slot3 PCM Playback Left Channel (18bits)
In the case of codec ID1:codec ID0=0:0 or 0:1, the AK4544A uses the playback(DAC) data format in slot3 for left channel.
Playback data format is MSB first. Data format is 18bits 2's complement. AC'97 controller should stuff bit1-0 with "0". If valid bit (slot3) in the slot 0 is invalid ("0"), the AK4544A interprets the data as all "0".
Bit19:2 Playback data
Bit 1:0 "0"

e)Slot4 PCM Playback Right Channel (18bits)
In the case of codec ID1:codec ID0=0:0 or 0:1, the AK4544A uses the playback(DAC) data format in the slot4 for right channel. Playback data format is MSB first. Data format is 18bits 2's complement. AC'97 controller should stuff bit1-0 with "0". If valid bit (slot 4) in the slot 0 is invalid ("0"), the AK4544A interprets the data as all "0".
Bit19:2 Playback data
Bit 1:0 "0"

f)Slot5 Not implemented in the AK4544A
The AK4544A ignores this data slot.

g)Slot6 PCM Playback Left Channel (18bits)
In case of codec ID1:codec ID0=1:1, the AK4544A uses playback(DAC) data format in the slot 6 for left channel.
Playback data format is MSB first. Data format is18bits 2's complement. AC'97 controller should stuff bit1-0 with "0". If valid bit (slot6) in the slot 0 is invalid ("0"), the AK4544A interprets the data as all "0".
Bit19:2 Playback data
Bit 1:0 "0"

h)Slot7 PCM Playback Left Channel (18bits)
In case of codec ID1:codec ID0=1:0, the AK4544A uses playback(DAC) data format in the slot7 for left channel.
Playback data format is MSB first. Data format is18bits 2's complement. AC'97 controller should stuff bit1-0 with "0". If valid bit (slot7) in the slot 0 is invalid ("0"), the AK4544A interprets the data as all "0".
Bit19:2 Playback data
Bit 1:0 "0"

i)Slot8 PCM Playback Right Channel (18bits)
In case of codec ID1:codec ID0=1:0, the AK4544A uses playback(DAC) data format in the slot8 for right channel.
Playback data format is MSB first. Data format is 18bits 2's complement. AC'97 controller should stuff bit1-0 with "0". If valid bit (slot8) in the slot 0 is invalid ("0"), the AK4544A interprets the data as all "0".
Bit19:2 Playback data
Bit 1:0 "0"

j)Slot9 PCM Playback Right Channel (18bits)
In case of codec ID1:codec ID0=1:1, the AK4544A uses playback(DAC) data format in the slot 9 for right channel.
Playback data format is MSB first. Data format is 18bits 2's complement. AC'97 controller should stuff bit1-0 with "0". If valid bit (slot9) in the slot 0 is invalid ("0"), the AK4544A interprets the data as all "0".
Bit19:2 Playback data
Bit 1:0 "0"

k)Slot10-12 Not implemented in the AK4544A
The AK4544A ignores these data slots.

AC-link Input Frame(SDATA_IN)

Each AC-link frame consists of one 16bit tag phase and twelve 20bit slots used for data and control.

a)Slot0

Slot0 is a special time frame, and consists of 16bits. Slot0 is also named the Tag phase. The AK4544A supports Bits 15-11 and bits1-0. Each bit indicates "1"=valid(normal operation) or ready, "0"=invalid(abnormal operation) or not ready.

If the first bit in the slot 0 (Bit15) is valid, the AK4544A is ready for normal operation. [3]If the "Codec Ready" bit is invalid, the following bits and remaining slots are all "0". AC'97 controller should ignore the following bits in the slot 0 and all other slots. When the ADC sampling rate is set for less than 48kHz, then Bits 12and 11 in slot 0 (corresponds to slot3 and slot4 respectively) will be 1's when valid data is transferred in SDATA_IN, and will be 0's when no data is transmitted. (On-demand) base data transaction)

The next is the extracted description from AC'97 Rev.2.1 ;

"For variable sample rate input, the tag bit for each input slot indicates whether valid data is present or not. Thus, even in variable sample rate mode, the Codec is always the master: for SDATA_IN (Codec to Controller), the Codec sets the TAG bit; for SDATA_OUT (Controller to Codec), the Codec sets the SLOTREQ bit and then checks for the TAG bit in the next frame." AK4544A expects Controller will reply TAG bit in the next frame correctly.

Bit 14 means that Slot 1(Status Address) output is valid or invalid. And Bit 13 means that Slot 2(Status Data) is valid or invalid.

The following table shows the relationship between Bit 14,13 and each Status of the AK4544A.

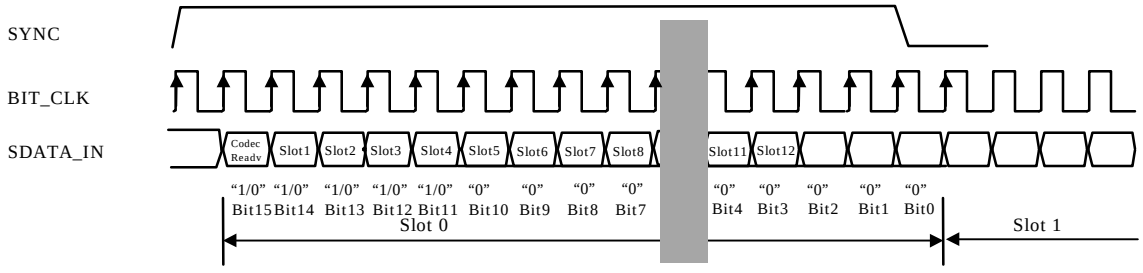
Bit 15 (Codec Ready)	Bit 14 (Status Address)	Bit 13 (Status Data)	Status
1	1	1	There is a Read Command in the previous frame. Then both Slot 1 and Slot 2 output normal data. If the access to non-implemented register or odd register is requested, the AK4544A returns "valid" 7-bit register address in slot 1 and returns "valid"0000h data in slot 2 on the next AC-link frame.
1	1	0	Prohibited or non-existing
1	0	0	There is no Read Command in the previous frame. Bits 19-12, Bit 9 and Bits 4-0 in Slot 1 are set to "0". And Slot2 outputs All"0".
1	0	1	Prohibited or non-existing

Note 1). The above Read sequence is done as response for previous frames read command. That is, if the previous frame is the Write Command, AK4544A outputs bit14 ="0", bit13 ="0" and slot 1&2 = All"0", if there is no SLOTREQ.

2). The Bits 14 and 13 in Slot 0 is independent of the SLOTREQ Bits 11,10, 8, 7, 6 and 5 in Slot 1 which the AK4544A supports.

Bit12 means the output of Slot 3(PCM(ADC) Left) is valid or invalid. And Bit 11 means the output of Slot 4(PCM(ADC)Right) is valid or invalid. Bits10-0 are occupied with "0".

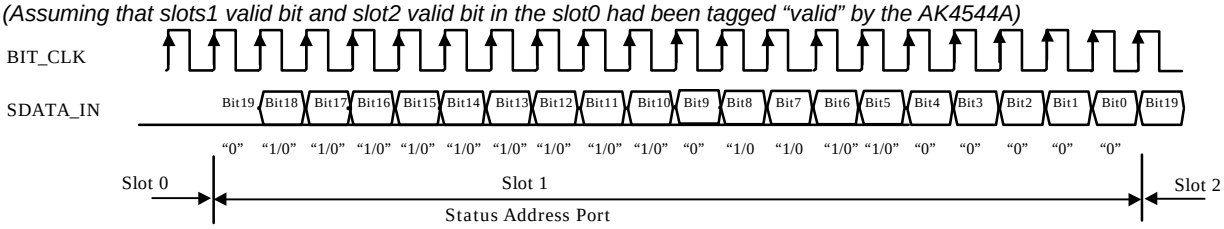
A new audio input frame begins with a low to high transition of SYNC. SYNC is synchronous to the rising edge of BIT_CLK. On the immediately following falling edge of BIT_CLK, the AK4544A samples the assertion of SYNC. This falling edge marks the time when both sides of AC-link are aware of the start of a new audio frame. On the next rising of BIT_CLK, the AK4544A transitions SDATA_IN into the first bit position of slot 0 ("Codec Ready" bit). Each new bit position is presented to AC-link on a rising edge of BIT_CLK, and subsequently sampled by the AC '97 controller on the following falling edge of BIT_CLK. This sequence ensures that data transitions, and subsequent sample points for both incoming and outgoing data streams are time aligned.



[3] When the AC' 97 is not ready for normal operation, output bits are not specified and should be ignored.

b)Slot1 Status Address Port

Audio input frame slot1's stream echoes the control register index, for historical reference, for the data to be returned in slot2. (Assuming that slots1 valid bit and slot2 valid bit in the slot0 had been tagged "valid" by the AK4544A)



This address shows register index for which data is being returned in the slot2.
This address port is the copy of slot1 of the output frame, and index address input to SDATA_OUT is looped back to the AC'97 controller through SDATA_IN even for non-supported register.

For "On Demand" base data transaction, when the DAC sampling rate is set less than 48kHz, then AK4544A will request new audio data as required by setting the SLOTREQ bits 11 and 10 (or bits 8 and 5, or bits 7 and 6) in Slot1 to 0's. When no data is required to support the selected sampling rate, these bits will be 1's. When SLOTREQ bits are asserted as "send data request" during the current frame on SDATA_IN, AC'97 digital controller should send data onto the corresponding slot in the next frame on SDATA_OUT.
If VRA is set "0", SLOTREQ bits show always "0" and sample rate is forced to 48ksps.

SLOTREQ Bit	Description
19	Reserved (Set to "0")
18 – 12	Control Register Index (Set to "0"s if tagged invalid)
11	Slot 3 Request : PCM Left channel for Codec ID=0:0 or 0:1 "0": send data request, "1": do not send
10	Slot 4 Request : PCM Right channel for Codec ID=0:0 or 0:1 "0": send data request, "1": do not send
9	Reserved (Set to "0")
8	Slot 6 Request : PCM Left channel for Codec ID=1:1 "0": send data request, "1": do not send
7	Slot 7 Request : PCM Left channel for Codec ID=1:0 "0": send data request, "1": do not send
6	Slot 8 Request : PCM Right channel for Codec ID=1:0 "0": send data request, "1": do not send
5	Slot 9 Request : PCM Right channel for Codec ID=1:1 "0": send data request, "1": do not send
4 – 0	Reserved (Set to "0")

c)Slot2: Status Data Port
Status data addressed by command address port of Output Stream is output through SDATA_IN pin.
Bit19:4 Control Register Read Data (the contents of indexed address in the slot 1)
Bit3:0 "0"

Note that the address of Status Data Port data are consistent with Status Address Port data of the slot 1 ***in the same frame***. If the read operation is issued in the frame N by AC'97 controller, Status Data Port data is output through SDATA_IN in the frame N+1. **Note that data is output in only this frame, only one time and that the following frames are invalid if the next read operation is not issued.**

d)Slot3 PCM Record Left Channel
Record(ADC) data format is MSB first. Data format is 2's complement. As the resolution of the AK4544A is 18bit, lower 2 bits are ignored. If ADC block is powered down, slot-3 valid bit in the slot 0 is invalid ("0"), and data is output as all "0".

Bit19:2 Audio ADC left channel output
Bit1:0 "0"

e)Slot4 PCM Record Right Channel
Record(ADC) data format is MSB first. Data format is 2's complement. As the resolution of the AK4544A is 18bit, lower 2 bits are ignored. If ADC block is powered down, slot-4 valid bit in the slot 0 is invalid ("0"), and data is output as all "0".
Bit19:2 Audio ADC right channel output
Bit1:0 "0"

f)Slot5 Modem Line Codec
As the AK4544A does not incorporate modem codec, all bits are stuffed with "0".
Bit19:0 "0"

g)Slot6 Microphone Record Data
As the AK4544A does not incorporate 3rd ADC codec, all bits are stuffed with "0".
Bit19:0 "0"

h)Slots7-12 Reserved for future enhancement
Bits19:0 "0"

■Mixer Registers

Each Register is 16 bit wide.

Note: The AK4544A outputs "valid" 0000h if the controller reads an unused or invalid register address.

Reg Num	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
00h	Reset	0	"0"	"1"	"0"	"1"	"1"	"0"	"1"	"0"	"1"	"0"	"1"	"0"	"0"	"0"	"0"	2D50h
02h	Master Volume	Mute	X	ML5	ML4	ML3	ML2	ML1	ML 0	X	X	MR5	MR4	MR3	MR2	MR1	MR0	8000h
04	LNLVL Volume	Mute	X	ML5	ML4	ML3	ML2	ML1	ML 0	X	X	MR5	MR4	MR3	MR2	MR1	MR0	8000h
06h	Master Volume Mono	Mute	X	X	X	X	X	X	X	X	X	MR5	MR4	MR3	MR2	MR1	MR0	8000h
0Ah	PC_BEEP Volume	Mute	X	X	X	X	X	X	X	X	X	X	PV3	PV2	PV1	PV0	X	0000h
0Ch	Phone Volume	Mute	X	X	X	X	X	X	X	X	X	X	GN4	GN3	GN2	GN1	GN0	8008h
0Eh	Mic Volume	Mute	X	X	X	X	X	X	X	X	20dB	X	GN4	GN3	GN2	GN1	GN0	8008h
10h	Line In Volume	Mute	X	X	GL4	GL3	GL2	GL1	GL0	X	X	X	GR4	GR3	GR2	GR1	GR0	8808h
12h	CD Volume	Mute	X	X	GL4	GL3	GL2	GL1	GL0	X	X	X	GR4	GR3	GR2	GR1	GR0	8808h
14h	Video Volume	Mute	X	X	GL4	GL3	GL2	GL1	GL0	X	X	X	GR4	GR3	GR2	GR1	GR0	8808h
16h	Aux Volume	Mute	X	X	GL4	GL3	GL2	GL1	GL0	X	X	X	GR4	GR3	GR2	GR1	GR0	8808h
18h	PCM Out Volume	Mute	X	X	GL4	GL3	GL2	GL1	GL0	X	X	X	GR4	GR3	GR2	GR1	GR0	8808h
1Ah	Record Select	X	X	X	X	X	SL2	SL1	SL0	X	X	X	X	X	SR2	SR1	SR0	0000h
1Ch	Record Gain	Mute	X	X	X	GL3	GL2	GL1	GL0	X	X	X	X	GR3	GR2	GR1	GR0	8000h
20h	General Purpose	POP	DFC	3D	X	X	X	MIX	MS	LPBK	X	X	X	X	X	X	X	0000h
22h	3D Control	X	X	X	X	X	X	X	X	X	X	X	X	DP3	DP2	DP1	DP0	0000h
26h	Powerdown Ctrl/Stat	PR7	PR6	PR5	PR4	PR3	PR2	PR1	PR0	X	X	X	X	REF	ANL	DAC	ADC	Na
28h	Extended Audio ID	ID1	ID0	X	X	X	X	AMAP	X	X	X	X	X	X	X	X	VRA	X201h
2Ah	Ext'd audio Stat/Ctrl	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	VRA	0000h
2Ch	PCM Front DAC Rate	SR15	SR14	SR13	SR12	SR11	SR10	SR9	SR8	SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0	BB80h
32h	PCM LR ADC Rate	SR15	SR14	SR13	SR12	SR11	SR10	SR9	SR8	SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0	BB80h
7Ch	Vendor ID1	"0"	"1"	"0"	"0"	"0"	"0"	"0"	"1"	"0"	"1"	"0"	"0"	"1"	"0"	"1"	"1"	414Bh
7Eh	Vendor ID2(AK4544A)	"0"	"1"	"0"	"0"	"1"	"1"	"0"	"1"	"0"	"0"	"0"	"0"	"0"	"1"	"1"	"0"	4D06h

*) Vender ID of AKM is "AKM" :This ID has been approved by Intel.

*) The AK4544A outputs "X" bits as "0".

*) A write on "Invalid" registers will not affect operation of the AK4544A.

*) ANL, DAC, ADC Bit in register 26h are all "0" following cold reset. When each section is ready for normal operation, the coresponding bit becomes "1". The Powerdown register(26h) is not affected by a write to Reset register(0h). See "Mixer Registers" in AC'97 specification for details. Vref is controlled only by PR3.

■Reset Register (Index 00h)

<Write>

When any value is written to the AK4544A, all registers including 2Ah, 2Ch, and 32h in the AK4544A except for 26h Powerdown/Control Register are reset to default values. The value of this register is not altered.

<Read>

Reading this register returns "2D50h"composed of the ID code of the part, a code for the type of 3D enhancement, 18 bit ADC/DAC resolution, and a code for True Line Level Out.

*Setting D14 – D10 "01011" means AKM 3D enhancement which is registered in Audio Codec '97 Component Specification Rev 1.03 and 2.1 .

*Setting D8 "1" means 18bit ADC resolution and D6"1" means 18bit DAC resolution.

*Setting D4 "1" means True Line Level Out is supported with Volume Control(Index 04h).

■ Play Master Volume Registers (Index 02h,06h) and LINVL(True Line Level Out) Volume Register(Index 04h)

The following table shows the relationship between bits and the attenuation value with step size of 1.5dB. The AK4544A has a range of 0dB to –46.5dB. The AK4544A does not support the optional MX5 bit.

The AK4544A detects when MX5 is set and set all 5 LSBs to 1s. Example: When the driver writes a "01xxxxx" the AK4544A interpret that as "0011111". When this register is read, the return value is "0011111".

Mute	MX5	MX4	MX3	MX2	MX1	MX0	Att.
0	0	0	0	0	0	0	0dB
0	0	0	0	0	0	1	-1.5dB
0	0	0	0	0	1	0	-3.0dB
0	0	0	0	0	1	1	-4.5dB
0	0	1	1	1	1	0	-45.0dB
0	0	1	1	1	1	1	-46.5dB
0	1	X	X	X	X	X	-46.5dB
1	X	X	X	X	X	X	Mute

n PC Beep Register (Index 0Ah)

The following table shows the relationship between bits and the attenuation value. The attenuation step is 3dB with a range of 0 to –45dB. PC_BEEP of the AK4544A is 0dB at default state.

The PC Beep is routed to L & R Line outputs directly when AK4544A is in a RESET State(Reset# is "L") or when the mixer is powerdown with Vref on(PR2="1" and PR3="0"). The PC BEEP isn't routed to True Line Level Out under these states. This is so that Power on Self Test(POST) codes can be heard by the user in case of a hardware problem with the PC. After Reset# goes "H", direct PC beep pass through becomes OFF.

Mute	PV3	PV2	PV1	PV0	Att.
0	0	0	0	0	0dB
0	0	0	0	1	-3.0dB
0	0	0	1	0	-6.0dB

0	1	1	1	1	-45.0dB
1	X	X	X	X	Mute

n Analog Mixer Input Gain Registers (Index 0Ch-18h)

The following table shows the relationship between bits and the gain/attenuation value. Attenuation step is 1.5dB with a range of +12dB to –34.5dB.

Mute	Gx4	Gx3	Gx2	Gx1	Gx0	Att.
0	0	0	0	0	0	+12dB
0	0	0	0	0	1	+10.5dB

0	0	1	0	0	0	0dB
0	0	1	0	0	1	-1.5dB

0	1	1	1	1	0	-33.0dB
0	1	1	1	1	1	-34.5dB
1	X	X	X	X	X	Mute

n Record Select Control Register (Index 1Ah)

SR2	SR1	SR0	Att.
0	0	0	Mic
0	0	1	CD In (R)
0	1	0	Video In (R)
0	1	1	Aux In (R)
1	0	0	Line In (R)
1	0	1	Stereo Mix (R)
1	1	0	Mono Mix
1	1	1	Phone

n Record Gain Register (Index 1Ch)

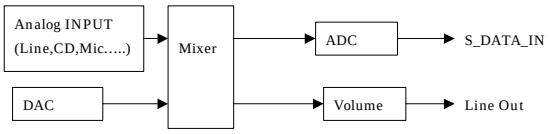
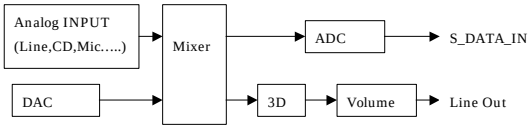
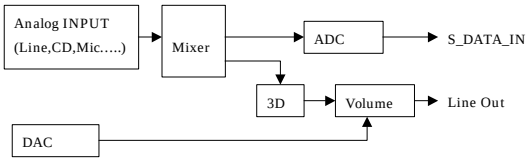
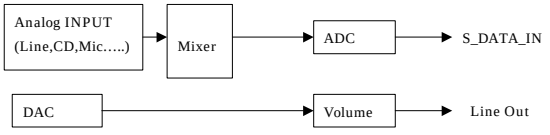
Mute	Gx3	Gx2	Gx1	Gx0	Gain
0	0	0	0	0	0dB
0	0	0	0	1	1.5dB
0	0	0	1	0	3.0dB
---	---	---	---	---	---
0	1	1	1	1	22.5dB
1	X	X	X	X	Mute

n General Purpose Register (Index 20h)

The following table shows the relationship between the bit and control for several miscellaneous functions of the AK4544A.

	Bit	Function	Comment
POP	D15	PCM(DAC) Bypass 3D 0= Via 3D Path, 1= 3D Bypass	Controls whether DAC output is mixed with analog inputs before the 3D circuit (POP=0) or after the 3D circuit (POP=1)
DFC	D14	DAC Feed Back Control 0=Mix, 1=DAC only	Controls whether Mix (DFC=0) or DAC only (DFC=1) is sent to the output
3D	D13	3D Stereo Enhancement 0=Off, 1=On	Controls whether the 3D circuit is bypassed (3D=0) or used (3D=1)
MIX	D9	Mono Output Select 0=Mix, 1=Mic	Controls whether Full Mix (Mix=0) or Mic inputs (Mix=1) is send to MONO_OUT
MS	D8	Mic Select 0=Mic1, 1 =Mic2	Selects Mic1 input (MS=0) or Mic2 (MS=1)
LPBK	D7	ADC/DAC Loopback Mode 1= Loopback	Selects normal operation (LPBK=0) or loops ADC data directly to DACs (LPBK=1)

Relations of control bits D15,14,13

POP	DFC	3D	Function	Path at selecting "Stereo Mixer" record(1Ah register = 0505h)
X	0	0	3D bypass to Volumes (Normal) Mixer **à** Vol	
0	0	1	3D output to Volumes Mixer **à** 3D **à** Vol	
1	0	1	(3D out + DAC) to Volumes (Mixer(w/0 DAC) + DAC) **à** Vol	
X	1	X	Only DAC fed to Volumes DAC **à** Vol Then the path from DAC to Mixer is cut.	

D13(3D) will activate the AKM's 3D enhancement.

LPBK(ADC/DAC Loopback Mode) bit enables loopback of the ADC output to slot3 &4 of DAC input for both the Primary codec and Secondary codec on the same AC-Link. While this function is used, the sample rates of ADC and DAC must be set to 48KHz.

n 3D Control Register (Index 22h)

The following table shows the relationship between the bit and 3D Depth.

DP3	DP2	DP1	DP0	Depth	Recommended Application
0	0	0	0	0%	Off
0	0	0	1	50%	Audio
0	0	1	0	50%	Audio
0	0	1	1	50%	Audio
0	1	0	0	50%	Audio
0	1	0	1	50%	Audio
0	1	1	0	50%	Audio
0	1	1	1	50%	Audio
1	0	0	0	70%	Audio
1	0	0	1	70%	Audio
1	0	1	0	70%	Audio
1	0	1	1	70%	Audio
1	1	0	0	70%	Audio
1	1	0	1	70%	Audio
1	1	1	0	70%	Audio
1	1	1	1	100%	Game

n Powerdown Control/Status Register (Index 26h)

BitsD0 to D3 are read only. Any write to these bits will not affect the AK4544A. These bits are used as status bits to subsections of the AC'97 codec. A 1 indicates the subsection is “ready” or that is capable of performing in a nominal manner.

	Bit	Function
REF	D3	Vref up to nominal state 0=NOT ready, 1=ready,
ANL	D2	Analog mixers, etc ready 0=NOT ready, 1=ready
DAC	D1	DAC section ready to accept data 0=NOT ready, 1=ready
ADC	D0	ADC section ready to transmit data 0=NOT ready, 1=ready

The power down modes are as follows.

	Bit	Function
PR0	D8	PCM in ADC's & Input Mux Powerdown
PR1	D9	PCM out DACs Powerdown
PR2	D10	Analog Mixer Powerdown (Vref still on)
PR3	D11	Analog Mixer Powerdown (Vref off)
PR4	D12	Digital Interface (AC-link) Powerdown
PR5	D13	Internal Clk disable
PR6	D14	True Line Level Out Powerdown
PR7	D15	EAPD(External Amplifier Powerdown)

When PR3 is set to “1”, ADC, DAC, Mixer, True Line Lever Out, and VREF are powered down even if any PRx bit are “0”. When PR3 bit is reset to “0”, the AK4544A resumes the previous state by referencing previous PRx bit. In this case, the AK4544A outputs corresponding slot-x valid bits in the slot 0 as “0” until the AK4544A is power-up.

EAPD(External Amplifier Power Down) bit controls an external audio amplifier. EAPD=”0” places a “0”(L) on the output pin, enabling an external audio amplifier, EAPD=”1”(H) shuts it down. Power-up default is EAPD=”0”(external audio amplifier enabled).

n Extended Audio ID(Index 28h)

The Extended Audio ID(28h) is a read only register. 2bits D15&D14 can be read for codec identification. D15,14 are automatically set with the codec ID1# pin(46pin) and ID0# pin(45pin). ID1# pin and ID0# pin can be strapped and adopt inverted polarity and these logic values are stored to D15 and D14 called as ID1 bit and ID0 bit. Default ID (ID1,ID0)=(0,0) when both ID1# pin and ID0# pin are open state. Depended on codec ID configuration, the AK4544A is assigned to Primary codec or Secondary codec. Note that codec ID configuration has to be fixed before Powering up of the device.

Physical Connection		Logic Value		Configuration
Pin46(ID1#)	Pin45(ID0#)	ID1	ID0	
NC	NC	0	0	Primary
NC	GND	0	1	Secondary ID01
GND	NC	1	0	Secondary ID10
GND	GND	1	1	Secondary ID11

The AMAP bit D9 of this read only register for the AK4544A will always be set to "1" indicating that the default(following cold or warm reset) codec slot DAC mapping(configured via hardwiring, strap pin(s), or other methods) conform to below table.
The audio DAC mapping can be changed based on the codec ID configuration.

Codec ID	AC-link Frame Data used for DACs		Comments
	PCM Left DAC uses data from Slot No.	PCM Right DAC uses data from Slot No.	
00	3	4	Original Definition(Master)
01	3	4	Original Definition(Docking)
10	7	8	Left/Right surround channels
11	6	9	Center/LFE channels

Since AK4544A supports variable sample rates, field of D0: VRA is set to 1, indicates Variable Rate PCM Audio is supported.

n Extended Audio Status and Control Register (Index 2Ah)
Bits D0 to D3, and D11 to D14 are read/write controls, while D6 to D9 are read only data to controller.

Bit	Function
VRA=1 (D0)	Enables Variable Rate Audio mode in conjunction with Audio Sample Rate Control Registers and tag-bit/SLOTREQ signaling

Because CDAC,LDAC,SDAC, and MICADC are not supported, default value at cold register reset for D11-D14 is set to "0".
Internal SRC related circuits are controlled by this VRA bit(2Ah), not by VRA in Extended Audio ID register(28h).

n Audio Sample Rate control Registers (Index 2Ch, 32h)

Sample Rate controls for DACs, and ADC. 16bit data in D15(MSB) to D0 show unsigned value between 0 to 65535, representing the exact sampling frequency in Hz. These Sample Rate setting is done at VRA=1 of Extended Audio Status and Control Register(2Ah).

Sample Rate (kHz)	Data in D15 – D0
8.0	1F40 hex
11.025	2B11 hex
16.0	3E80 hex
22.05	5622 hex
32.0	7D00 hex
44.1	AC44 hex
48.0	BB80 hex

The AK4544A supports these discrete frequencies. When any other codes is written in this register, the AK4544A works at the sampling rate rounded to the closest one above by decoding of only D15-D12 bits.

D15 – D12	Sample Rate (kHz)
0,1	8.0
2	11.025
3	16.0
4,5	22.05
6,7,8	32.0
9,Ah	44.1
Bh-Fh	48.0

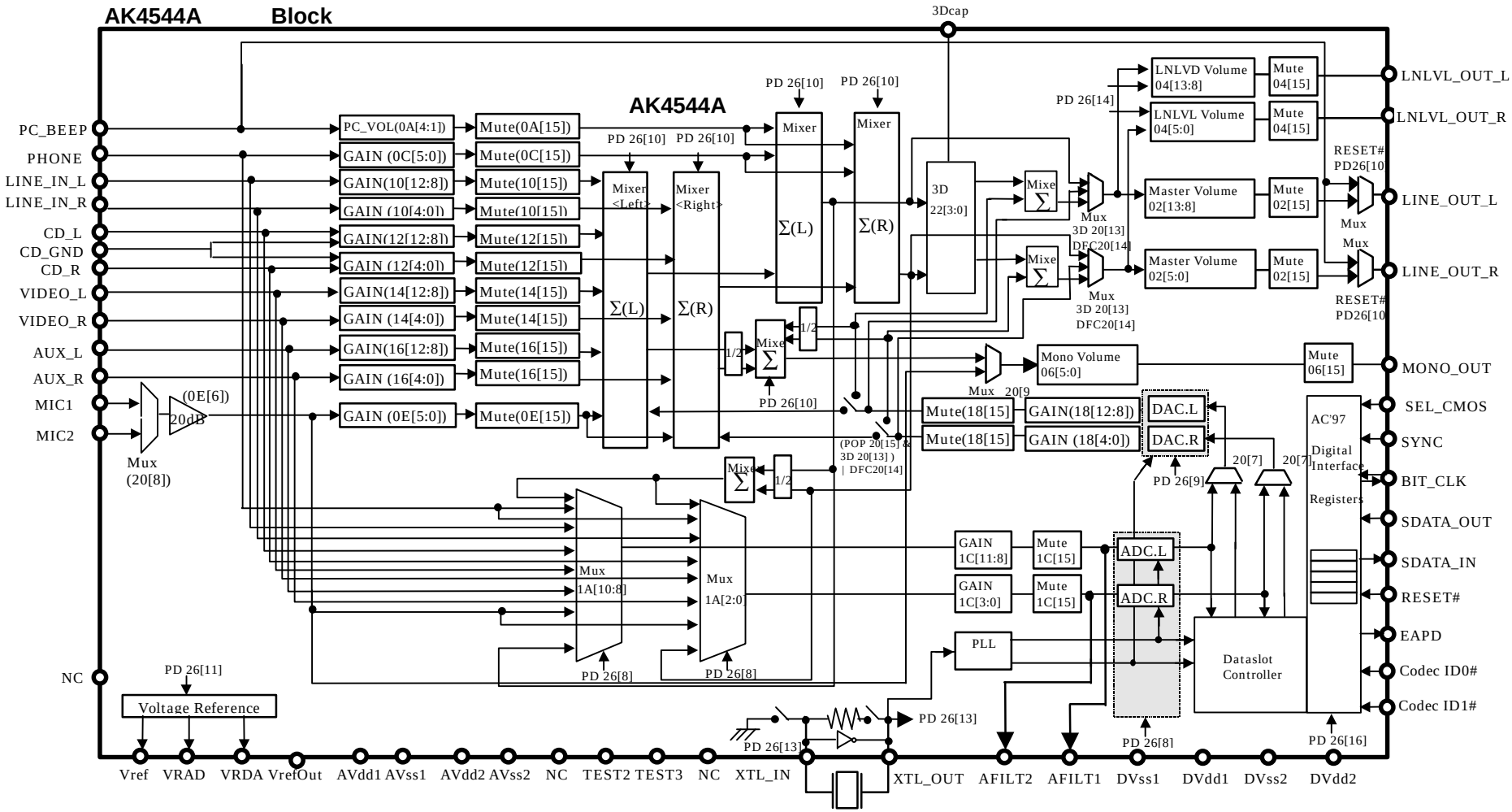
At VRA=0, 2Ch and 32h are “BB80h” and can’t be written. When VRA is set to 0, 2Ch and 32h register are set to “BB80h” automatically.

And the sample rate changing will be executed on the fly(immediately). It is recommended to set the zero data(no input/no ouput) at the fs changing in order to prevent some noise.

n Vendor ID Registers (Index 7Ch, 7Eh)

This register is a read only register that is used to determine the specific vendor identification. The ID method is Microsoft Plug and Play Vendor ID code with upper byte of 7Ch register, the first character of that id, lower byte of 7Ch register, the second character and upper byte of 7Eh register the third character. These three characters are ASCII encoded. Lower byte of 7E register is for the Vendor Revision number.

AKM’s vender ID is “AKM”, and revision number is 06 for AK4544A. As ASCII code “A” is 41h, “K” is 4Bh, and “M” is 4Dh, Vendor ID registers are 414Bh and 4D06h respectively for AK4544A.


AK4544A Block
AK4544A
3Dcap
PC_BEEP
PHONE
LINE_IN_L
LINE_IN_R
CD_L
CD_GND
CD_R
VIDEO_L
VIDEO_R
AUX_L
AUX_R
MIC1
MIC2
NC
(0E[6])
20dB
Mux
(20[8])
PC_VOL(0A[4:1])
GAIN (0C[5:0])
GAIN(10[12:8])
GAIN (10[4:0])
GAIN(12[12:8])
GAIN (12[4:0])
GAIN(14[12:8])
GAIN (14[4:0])
GAIN(16[12:8])
GAIN (16[4:0])
GAIN (0E[5:0])
Mute(0A[15])
Mute(0C[15])
Mute(10[15])
Mute(10[15])
Mute(12[15])
Mute(12[15])
Mute(14[15])
Mute(14[15])
Mute(16[15])
Mute(16[15])
Mute(0E[15])
PD 26[10]
Mixer
Mixer <Left>
Mixer <Right>
Σ(L)
Σ(R)
1/2
Mixer
3D 22[3:0]
PD 26[14]
LNLVD Volume 04[13:8]
LNLVL Volume 04[5:0]
Mute 04[15]
Master Volume 02[13:8]
Master Volume 02[5:0]
Mute 02[15]
Mux 3D 20[13] DFC20[14]
RESET# PD26[10]
LNLVL_OUT_L
LNLVL_OUT_R
LINE_OUT_L
LINE_OUT_R
Mono Volume 06[5:0]
Mute 06[15]
MONO_OUT
Mux 20[9
Mute(18[15]
GAIN(18[12:8])
Mute(18[15]
GAIN (18[4:0])
DAC.L
DAC.R
(POP 20[15] & 3D 20[13]) | DFC20[14]
PD 26[9]
20[7]
AC'97 Digital Interface Registers
SEL_CMOS
SYNC
BIT_CLK
SDATA_OUT
SDATA_IN
RESET#
EAPD
Codec ID0#
Codec ID1#
Mux 1A[10:8]
Mux 1A[2:0]
PD 26[8]
GAIN 1C[11:8]
GAIN 1C[3:0]
Mute 1C[15]
ADC.L
ADC.R
PLL
Dataslot Controller
PD 26[11]
Voltage Reference
PD 26[13]
PD 26[16]
Vref VRAD VRDA VrefOut AVdd1 AVss1 AVdd2 AVss2 NC TEST2 TEST3 NC XTL_IN XTL_OUT AFILT2 AFILT1 DVss1 DVdd1 DVss2 DVdd2

n Power Management/Low Power Modes

The AK4544A is capable of operating at multiple reduced power modes for when no activity is required. The state of power down is controlled by the Powerdown Register (26h). There are 8 separate commands for power down. See the table below for the different modes. As the AK4544A operates at static mode, the registers will not lose their values even if the master clock is stopped only upon power.

Powerdown Mode Truth Table

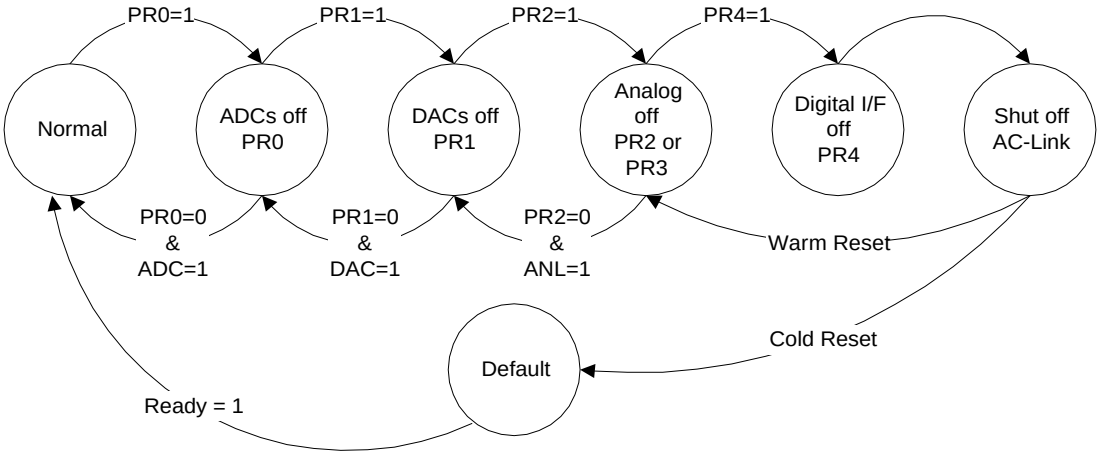
	ADC	DAC	Mixer	VREF	ACLINK	Internal CLK	LNLVL_OUT	EAPD
PR0="1"	PD	don't care	don't care	don't care	don't care	don't care	don't care	don't care
PR1="1"	don't care	PD	don't care	don't care	don't care	don't care	don't care	don't care
PR2="1"	don't care	don't care (No DAC out)	PD	don't care	don't care	don't care	PD	don't care
PR3="1"	PD	PD	PD	PD	don't care	don't care	PD	don't care
PR4="1"	PD	PD	don't care	don't care	PD	don't care	don't care	don't care
PR5="1"	PD	PD	don't care	don't care	PD	PD	don't care	don't care
PR6="1"	don't care	don't care	don't care	don't care	don't care	don't care	PD	don't care
PR7="1"	don't care	don't care	don't care	don't care	don't care	don't care	don't care	PD

*: PD means Powerdown .

**: No DAC out means that there is no PCM out because mixer is disabled.*

From normal operation sequential writes to the Powerdown Register are performed to power down subsections of the AK4544A one at a time. After everything has been shut off, a final write (of PR4) can be executed to shut down the AC '97 digital interface (AC-link). The part will remain in sleep mode with all its registers holding their static values. To wake up, the AC '97 controller will send a pulse on the sync line issuing a warm reset. This will restart the AK4544A digital (resetting PR4 to zero). The AK4544A can also be woken up with a cold reset. A cold reset will cause a loss of values of the registers as a cold reset will set them to their default states. When a subsection is powered back on the Powerdown Control/Status register (index 26h) should be read to verify that the section is ready (i.e. stable) before attempting any operation that requires its normal operation.

And the below figure illustrates one example of procedure to do a complete powerdown/power up of AK4544A.



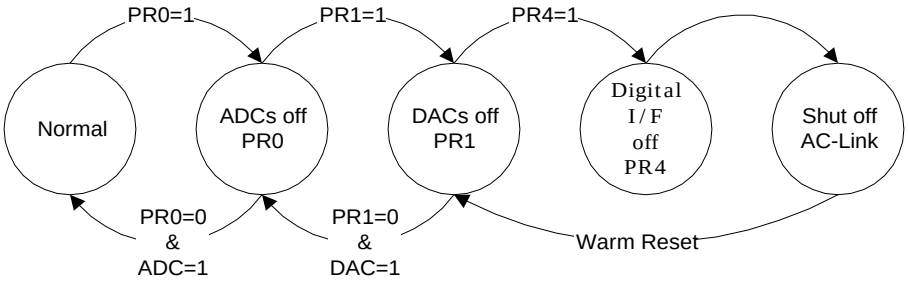
One example of AK4544A Powerdown/Powerup flow

When PR3 bit is set to "1", ADC, DAC, Mixer, True Line Level Out, and VREF will be powered down even if any PRx bit are "0". When PR3 bit is reset to "0", the AK4544A resumes with the previous state by referencing PRx bit. In this case, the AK4544A outputs "0" (invalid) for corresponding slot-x valid bits in the slot 0 until the corresponding block of the AK4544A is power-up.

Setting PR4 bit cause the Powerdown mode of AK4544A and AC-Link of AK4544A shut down. In this case, when Warm Reset is executed, PR4 bit is cleared and the AC-Link is reactivated. Meanwhile Cold reset is selected, AK4544A is restored to operation with default register settings.

In addition, setting PR5 bit causes the Powerdown mode of AK4544A and the internal clock of AK4544A to be stopped. When a warm reset is done in this case, PR5 bit is cleared to 0 and internal clock and AC-Link are reactivated. When Cold reset is executed, AK4544A is set up to the operation with default register setting, no powerdown modes active.

The next figure illustrates a state when all the mixers should work with the static volume settings that are contained in their associated registers. This is used when the user is playing a CD (or external LINE_IN source) through the AC '97 codec to the speakers but has most of the system in a low power mode. The procedure for this follows the previous except that the analog mixer is never shut down.



AK4544A Powerdown/Powerup flow with analog still alive

■ Powerdown/Powerup sequence of Multiple codec configuration

Under the multiple codec circumstances, there is no restriction on setting PR0(ADC), PR1(DAC), PR2(Mixer), PR6(LNLVL_OUT) and PR7(EAPD) to "1" or "0".

As suggested in AC'97 Specification Rev2.1, AC-Link Powerdown(PR"4") and Vref Powerdown(PR5="1") under the Multiple codec configuration are NOT recommended in order to continue supplying BIT_CLK to Secondary codecs.

Below table shows the relationship for AC-Link Powerdown/Powerup procedure.

AC-Link Powerdown Procedure	Subsequent Procedure for Powerup	Comments
RESET#=L	Cold Reset	Cold Reset wakes up all of codecs with default register setting concurrently.
Shutdown(Complete Powerdown)	Cold Reset	Cold Reset wakes up all of codecs with default register setting concurrently.

Note:
1) The AC-Link Powerdown of Primary AC'97 will stop supplying the BIT_CLK to the Secondary AC'97.
2) When the AC-Link Powerdown is issued to the Secondary of AC'97, the Secondary of AC'97 will go to the AC-Link Powerdown and Warm Reset will be followed by Syn signal at the next time frame.

■ **Testability**

Activating the Test Modes

AC '97 has two test modes. One is for ATE in circuit test and the other is for vendor specific tests. AC '97 enters the ATE in circuit test mode regardless of SYNC signal (high or low) if SDATA_OUT is sampled high at the trailing edge of RESET#. AC '97 enters AKM test mode in the case of condition below. These cases will never occur during standard operating conditions.
Regardless of the test mode, the AC '97 controller must issue a "Cold" reset to resume normal operation of the AC '97 Codec.

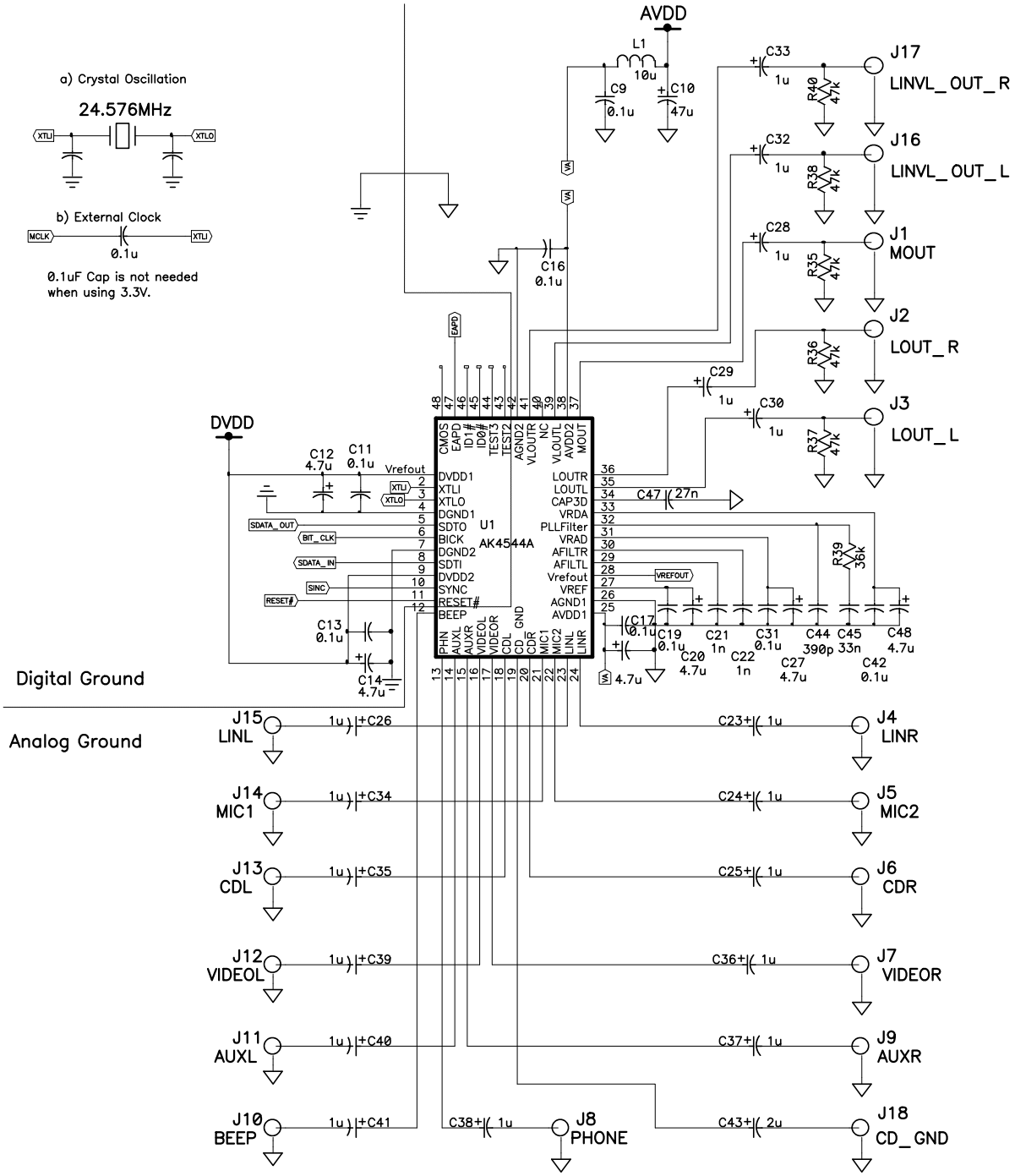
Test Mode Functions

ATE in circuit test mode
When AC '97 is placed in the ATE test mode, its digital AC-link outputs (i.e. BIT_CLK and SDATA_IN) are driven to a high impedance state. This allows ATE in circuit testing of the AC '97 controller.

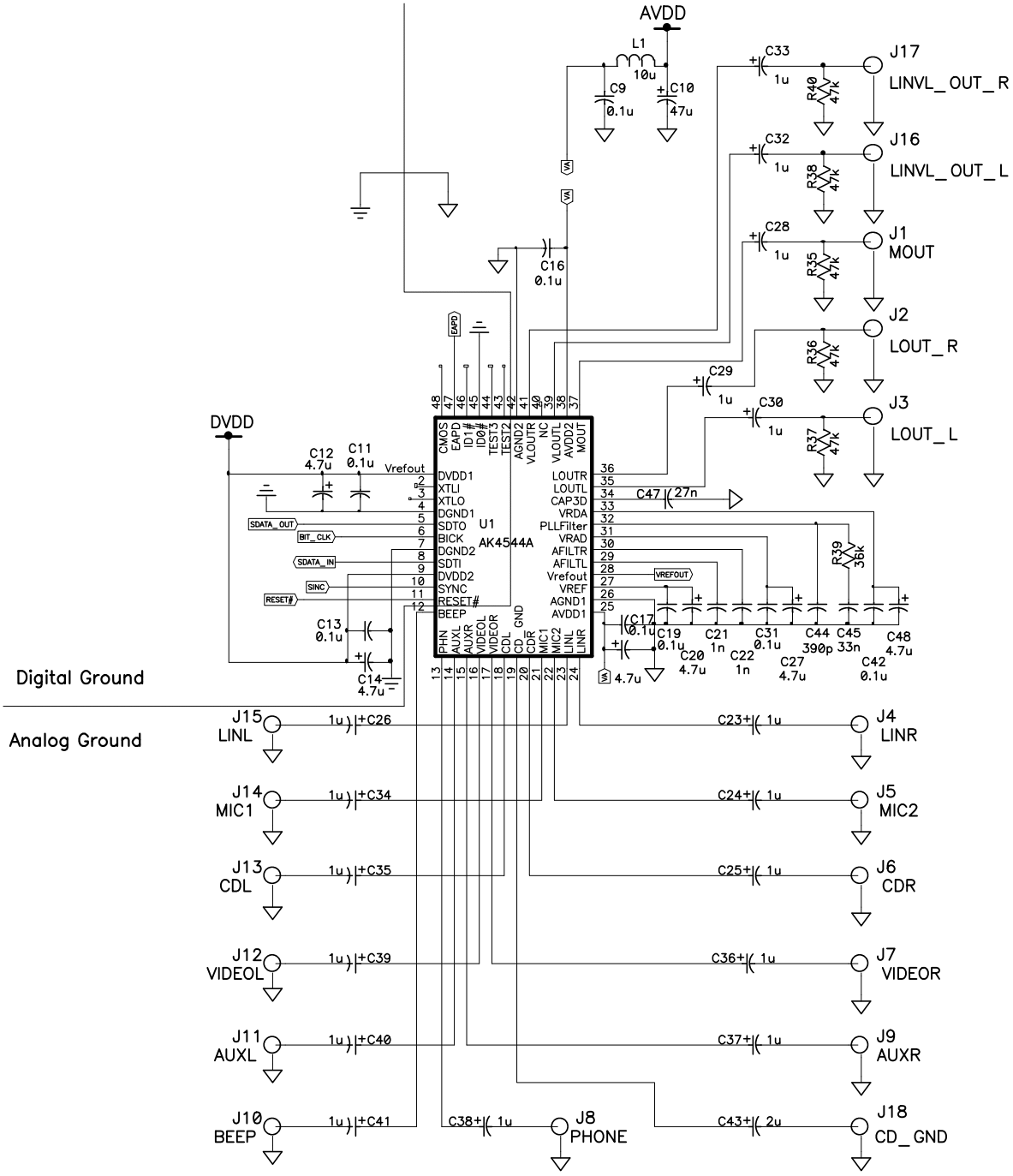
System Design

The following figure shows the system connection diagram.

Primary codec: codec ID1:codecID0=0:0
AVDD: 5V
DVDD: 3.3V or 5V
3.3V : 48pin open
5.0V : 48pin DGND



Secondary codec codec ID1:codecID0=0:1,1:0 or 1:1
This figure is the case of ID1 =0 and ID0=1.
AVDD: 5V
DVDD: 3.3V or 5V
3.3V : 48pin open
5.0V : 48pin DGND



1. Grounding and Power Supply Decoupling

AVdd1 and AVdd2 should be connected and derived from same AVdd. And DVdd1 and DVdd2 also should be connected and derived from same DVdd. Analog ground and digital ground should be connected together near to where the supplies are brought onto the printed circuit board. Decoupling capacitors should be as near to the AK4544A as possible, with the small value ceramic capacitor being the nearest.
No specific power supply sequencing is required on the AK4544A.

2. On-chip Voltage Reference

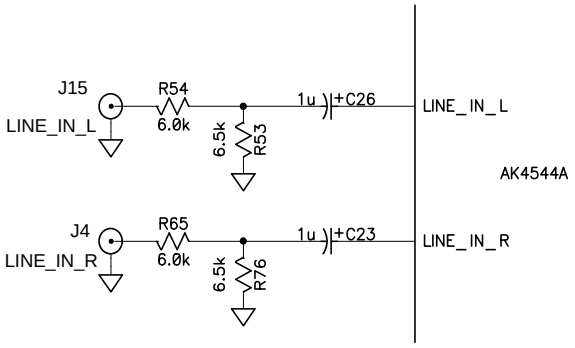
The on-chip voltage reference are output on the VRADDA, Vref pins for decoupling. A electrolytic capacitor less than 10uF in parallel with a 0.1 uF ceramic capacitor attached to these pins eliminates the effects of high frequency noise. No load current may be drawn from VRADDA, and Vref pins. All signals, especially clocks, should be kept away from the VRADDA, and Vref pins in order to avoid unwanted coupling into delta-sigma modulators.

3. Codec ID configuration Pin 45,46

Physical Connection		Logic Value		Configuration
Pin46(ID1#)	Pin45(ID0#)	ID1	ID0	
NC	NC	0	0	Primary
NC	GND	0	1	Secondary ID01
GND	NC	1	0	Secondary ID10
GND	GND	1	1	Secondary ID11

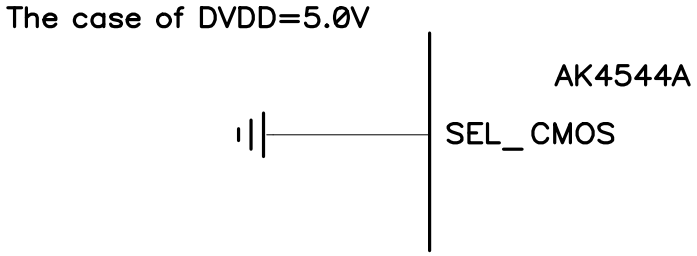
4.Analog input

Since many analog levels can be as high as 2Vrms, the circuit shown below can be used to attenuate the analog input 2Vrms to 1Vrms which is the maximum voltage allowed for all the stereo line-level inputs.



5.SEL_CMOS(48pin)

When DVDD is 3.3V for support of CMOS level, 48pin must be open.
The other hand, 48pin must be DGND as the below figure in the case of DVDD is 5.0V for TTL level
This SEL_CMOS has to be fixed before powered up the AK4544A.

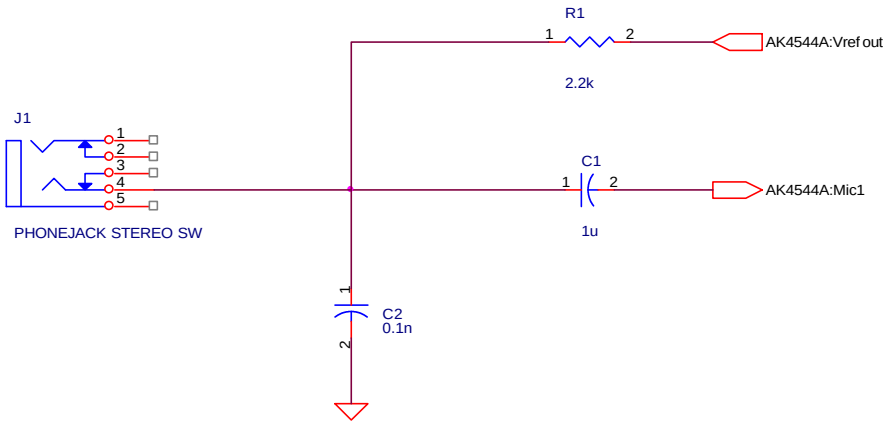


6.PC_BEEP

If PC_BEEP isn't used, this input pin should be NC(open) or connected to Analog-Ground through capacitor. In this case, the register for PC-Beep(04h,D15) should be set to mute on"1". (Note that the default of PC_BEEP is mute off.) In addition, when PC_BEEP is connected through capacity to Analog-Ground, PC_BEEP is recommended to be separated from other non-used input pins.

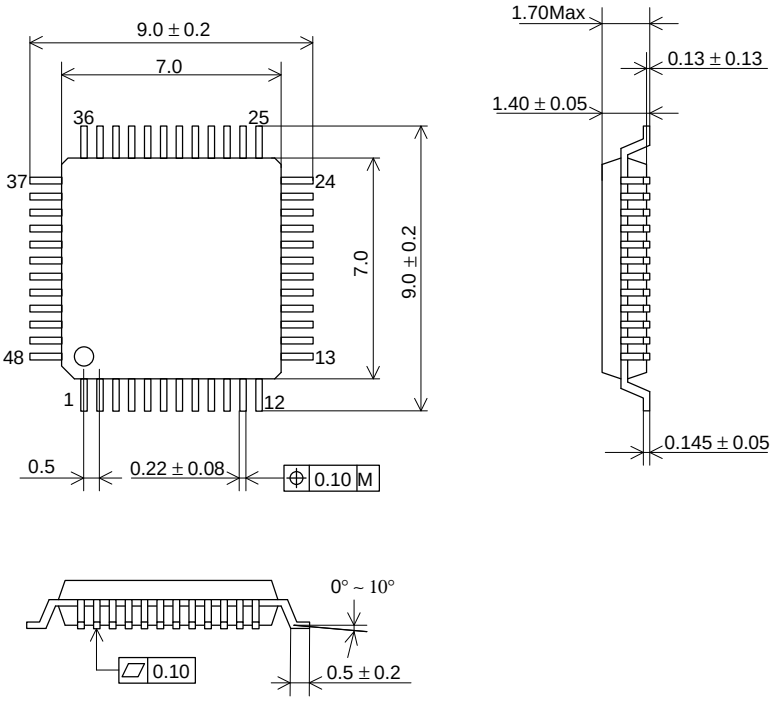
7.Microphone Input design

VrefOut of AK4544A 28pin can be used for Bias of Microphone Input.

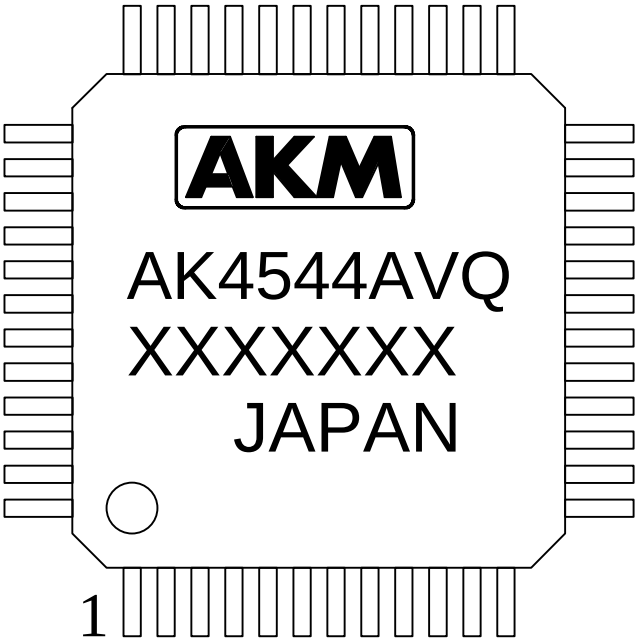


Package

48pin LQFP(Unit:mm)



Marking



1) Pin #1 indication
2) Date Code : XXXXXXX (7 digits)
3) Marketing Code : AK4544AVQ
4) Country of Origin
5) Asahi Kasei Logo

Appendix

1. Summary of the relationship of Slot 0 tag bit between SDATA_OUT and SDATA_IN

Following two tables describe the Slot0 tag bits relationship between SDATA_OUT and SDATA_IN.

Whenever the AC '97 Digital Controller addresses the Primary AK4544A or the AK4544A responds to a read command, Slot 0 tag bits should always be set to indicate actual Slot 1 and Slot 2 data validity.

Function	Slot 0, bit 15 (Valid Frame)	Slot 0, bit 14 (Valid Slot 1 Address)	Slot 0, bit 13 (Valid Slot 2 Data)	Slot 0, Bits 1-0 (Codec ID)
AC '97 Digital Controller Primary Read Frame N, SDATA_OUT	1	1	0	00
AC '97 Digital Controller Primary Write Frame N, SDATA_OUT	1	1	1	00
AK4544A Status Frame N+1, SDATA_IN	1	1	1	00

Primary AK4544A Addressing: Slot 0 tag bits

When the AC '97 Digital Controller addresses a Secondary AK4544A, the Slot 0 Tag bits for Address and Data must be "0". **A non-zero 2-bit Codec ID in the LSBs of Slot 0 indicates a valid Read or Write Address in Slot 1, and the Slot 1 R/W bit indicates presence or absence of valid Data in Slot 2.**

Function	Slot 0, bit 15 (Valid Frame)	Slot 0, bit 14 (Valid Slot 1 Address)	Slot 0, bit 13 (Valid Slot 2 Data)	Slot 0, Bits 1-0 (Codec ID)
AC '97 Digital Controller Secondary Read Frame N, SDATA_OUT	1	0	0	01, 10, or 11
AC '97 Digital Controller Secondary Write Frame N, SDATA_OUT	1	0	0	01, 10, or 11
AK4544A Status Frame N+1, SDATA_IN	1	1	1	00

Secondary AK4544A Addressing: Slot 0 tag bits

2. Summary of the relationship with Slot 0 tag bits and the SLOTREQ position in Slot1 of SDATA_IN with respect to the multiple codec assignment.

In the case of SDATA_OUT, when the AC '97 Digital Controller addresses a Secondary AK4544A, the Slot 0 Tag bits for Address and Data must be "0". Instead, either bit or both bits of Bit1-0 in Slot0 must be "1" for Read /Write operation for secondary codec.

Function	Slot 0, bit 15 (Valid Frame)	Slot 0, bit 14 (Valid Slot 1 Address)	Slot 0, bit 13 (Valid Slot 2 Data)	Slot 0, Bits 1-0 (Codec ID)	Slot 1 SLOTREQ
Primary (Codec ID=0:0 or 0:1)	1	1 or 0	1 or 0	00	Bit11 for PCM Left Bit10 for PCM Right
Secondary(CodecID=1:0)	1	1 or 0	1 or 0	00	Bit7 for PCM Left Bit6 for PCM Right
Secondary(CodecID=1:1)	1	1 or 0	1 or 0	00	Bit8 for PCM Left Bit5 for PCM Right

SLOTREQ position in Slot1 of SDATA_IN

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