

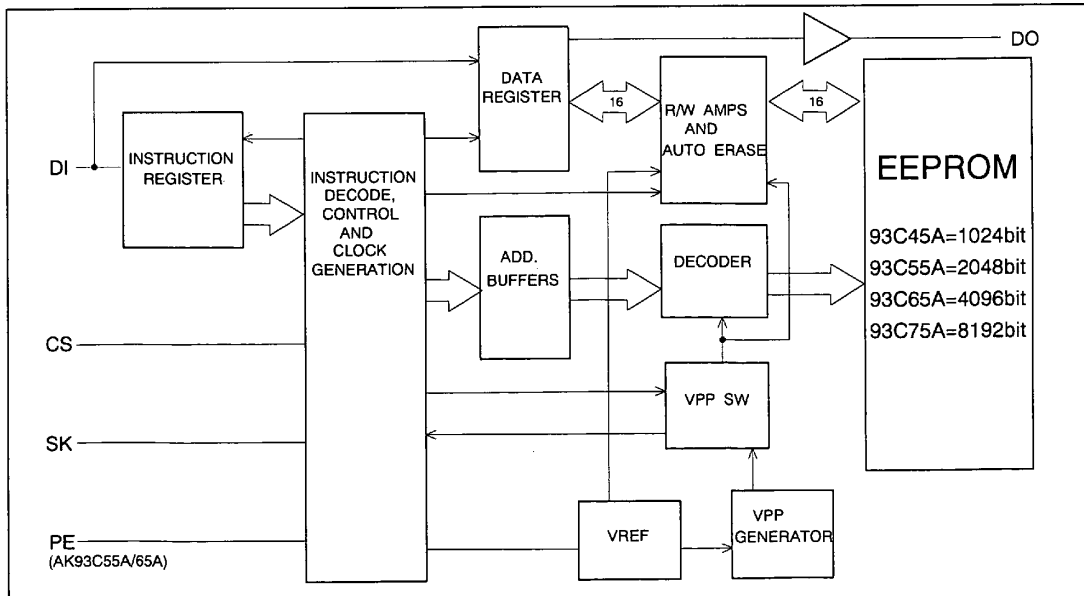


AK93C45A / 55A / 65A / 75A

1K / 2K / 4K / 8Kbit Serial CMOS EEPROM

Features

- ADVANCED CMOS EEPROM TECHNOLOGY
- READ/WRITE NON-VOLATILE MEMORY
- WIDE VCC OPERATION ... Vcc = 1.8V ~ 5.5V
- AK93C45A . . . 1024 bits, 64 × 16 organization
 AK93C55A . . . 2048 bits, 128 × 16 organization
 AK93C65A . . . 4096 bits, 256 × 16 organization
 AK93C75A . . . 8192 bits, 512 × 16 organization
- SERIAL INTERFACE
 - Interfaces with popular microcontrollers and standard microprocessors
- LOW POWER CONSUMPTION
 - 0.5mA max. Read Operation
 - 0.8μA Max. Standby
- HIGH RELIABILITY
 - Endurance : 100K cycles
 - Data Retention : 10 years
- Automatic address increment (READ)
- Automatic write cycle time-out with auto-ERASE
- Busy/Ready status signal
- Software controlled write protection
- IDEAL FOR LOW DENSITY DATA STORAGE
 - Low cost, space saving, 8-pin package



Block Diagram

| |
|----------------------------|
| General Description |
|----------------------------|

The AK93C45A/55A/65A/75A is a 1024/2048/4096/8192-bit serial CMOS EEPROM divided into 64/128/256/512 registers of 16 bits each.

The AK93C45A/55A/65A/75A has 4 instructions such as READ, WRITE, EWEN and EWDS. Those instructions control the AK93C45A/55A/65A/75A.

The AK93C45A/55A/65A/75A can operate full function under wide operating voltage range from 1.8V to 5.5V. The charge up circuit is integrated for high voltage generation that is used for write operation.

A serial interface of AK93C45A/55A/65A/75A, consisting of chip select (CS), serial clock (SK), data-in (DI) and data-out (DO), can easily be controlled by popular microcontrollers or standard microprocessors.

AK93C45A/55A/65A/75A takes in the write data from data input pin (DI) to a register synchronously with rising edge of input pulse of serial clock pin (SK). And at read operation, AK93C45A/55A/65A/75A takes out the read data from a register to data output pin (DO) synchronously with rising edge of SK.

The DO pin is usually in high impedance state. The DO pin outputs "L" or "H" in case of data output or $\overline{\text{Busy/Ready}}$ signal output.

• Software and Hardware controlled write protection

When Vcc is applied to the part, the part automatically powers up in the ERASE/WRITE Disable state. In the ERASE/WRITE disable state, execution of WRITE instruction is disabled. Before WRITE instruction is executed, EWEN instruction must be executed. The ERASE/WRITE enable state continues until EWDS instruction is executed or Vcc is removed from the part.

Execution of a read instruction is independent of both EWEN and EWDS instructions.

The PE is internally pulled up to VCC. If the PE is left unconnected, the part will accept WRITE, EWEN and EWDS instructions. • AK93C55A/65A

• $\overline{\text{Busy/Ready}}$ status signal

After a write instruction, the DO output serves as a $\overline{\text{Busy/Ready}}$ status indicator. After the falling edge of the CS initiates the self-timed programming cycle, the DO indicates the $\overline{\text{Busy/Ready}}$ status of the chip if the CS is brought high after a minimum of 250ns (Tcs). DO=logical "0" indicates that programming is still in progress. DO=logical "1" indicates that the register at the address specified in the instruction has been written with the new data pattern contained in the instruction and the part is ready for a next instruction.

The $\overline{\text{Busy/Ready}}$ status indicator is only valid when CS is active (high). When CS is low, the DO output goes into a high impedance state.

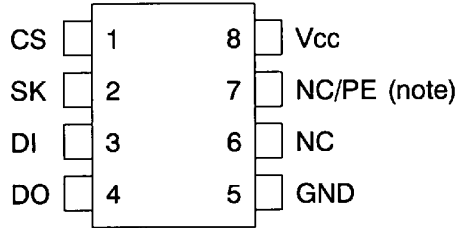
The $\overline{\text{Busy/Ready}}$ signal outputs until a start bit (Logic"1") of the next instruction is given to the part.

■ Type of Products

| Model | Memory size | Temp.Range | Vcc | Package |
|------------|-------------|------------|-----------|--------------------|
| AK93C45AF | 1Kbits | -40°C~85°C | 1.8V~5.5V | 8pin Plastic SOP |
| AK93C45ANF | | -40°C~85°C | 1.8V~5.5V | 8pin Plastic SOP |
| AK93C45AV | | -40°C~85°C | 1.8V~5.5V | 8pin Plastic TSSOP |
| AK93C55AF | 2Kbits | -40°C~85°C | 1.8V~5.5V | 8pin Plastic SOP |
| AK93C55ANF | | -40°C~85°C | 1.8V~5.5V | 8pin Plastic SOP |
| AK93C55AV | | -40°C~85°C | 1.8V~5.5V | 8pin Plastic TSSOP |
| AK93C65AF | 4Kbits | -40°C~85°C | 1.8V~5.5V | 8pin Plastic SOP |
| AK93C65ANF | | -40°C~85°C | 1.8V~5.5V | 8pin Plastic SOP |
| AK93C65AV | | -40°C~85°C | 1.8V~5.5V | 8pin Plastic TSSOP |
| AK93C75AF | 8Kbits | -40°C~85°C | 1.8V~5.5V | 8pin Plastic SOP |
| AK93C75ANF | | -40°C~85°C | 1.8V~5.5V | 8pin Plastic SOP |
| AK93C75AV | | -40°C~85°C | 1.8V~5.5V | 8pin Plastic TSSOP |

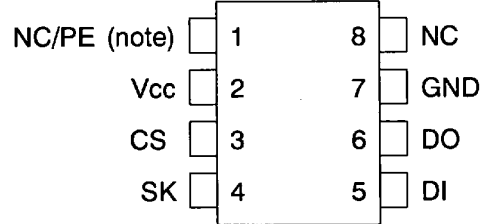
Pin arrangement

AK93C45ANF/55ANF/65ANF/75ANF



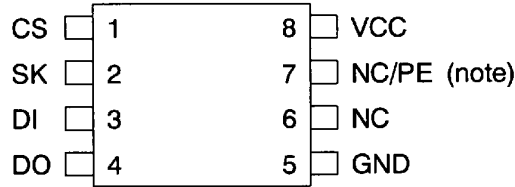
8pinSOP

AK93C45AF/55AF/65AF/75AF



8pinSOP

AK93C45AV/55AV/65AV/75AV



8pinTSSOP

(note) AK93C45A/75A . . . NC, AK93C55A/65A . . . PE

| Pin Name | Function |
|----------|--------------------|
| CS | Chip Select |
| SK | Serial Data Clock |
| DI | Serial Data Input |
| DO | Serial Data Output |
| GND | Ground |
| PE | Program Enable |
| Vcc | Power Supply |
| NC | Not Connected |

(note) The PE is internally pulled up to VCC (R = typ.2.5MΩ, VCC=5V).

Functional Description

The AK93C45A/55A/65A/75A has 4 instructions such as READ, WRITE, EWEN and EWDS. A valid instruction consists of a Start Bit (Logic"1"), the appropriate Op Code and the desired memory Address location.

The CS pin must be brought low for a minimum of 250ns (Tcs) between each instruction when the instruction is continuously executed.

| Instruction | Start Bit | Op Code | Address | Data | Comments |
|-------------|-----------|---------|---------|--------|--|
| READ | 1 | 10 | A5-A0 | D15-D0 | Reads data stored in memory, at specified address. |
| WRITE | 1 | 01 | A5-A0 | D15-D0 | Writes register. |
| EWEN | 1 | 00 | 11XXXX | | Write enable must precede all programming modes. |
| EWDS | 1 | 00 | 00XXXX | | Disables all programming instructions. |
| WRAL | 1 | 00 | 01XXXX | D15-D0 | Writes all registers. |

X: Don't care

table 1. Instruction Set for the AK93C45A

| Instruction | Start Bit | Op Code | Address | Data | Comments |
|-------------|-----------|---------|----------|--------|--|
| READ | 1 | 10 | X A6-A0 | D15-D0 | Reads data stored in memory, at specified address. |
| WRITE | 1 | 01 | X A6-A0 | D15-D0 | Writes register. |
| EWEN | 1 | 00 | 11XXXXXX | | Write enable must precede all programming modes. |
| EWDS | 1 | 00 | 00XXXXXX | | Disables all programming instructions. |
| WRAL | 1 | 00 | 01XXXXXX | D15-D0 | Writes all registers. |

X: Don't care

table 2. Instruction Set for the AK93C55A

| Instruction | Start Bit | Op Code | Address | Data | Comments |
|-------------|-----------|---------|----------|--------|--|
| READ | 1 | 10 | A7-A0 | D15-D0 | Reads data stored in memory, at specified address. |
| WRITE | 1 | 01 | A7-A0 | D15-D0 | Writes register. |
| EWEN | 1 | 00 | 11XXXXXX | | Write enable must precede all programming modes. |
| EWDS | 1 | 00 | 00XXXXXX | | Disables all programming instructions. |
| WRAL | 1 | 00 | 01XXXXXX | D15-D0 | Writes all registers. |

X: Don't care

table 3. Instruction Set for the AK93C65A

| Instruction | Start Bit | Op Code | Address | Data | Comments |
|-------------|-----------|---------|------------|--------|--|
| READ | 1 | 10 | XA8-A0 | D15-D0 | Reads data stored in memory, at specified address. |
| WRITE | 1 | 01 | XA8-A0 | D15-D0 | Writes register. |
| EWEN | 1 | 00 | 11XXXXXXXX | | Write enable must precede all programming modes. |
| EWDS | 1 | 00 | 00XXXXXXXX | | Disables all programming instructions. |
| WRAL | 1 | 00 | 01XXXXXXXX | D15-D0 | Writes all registers. |

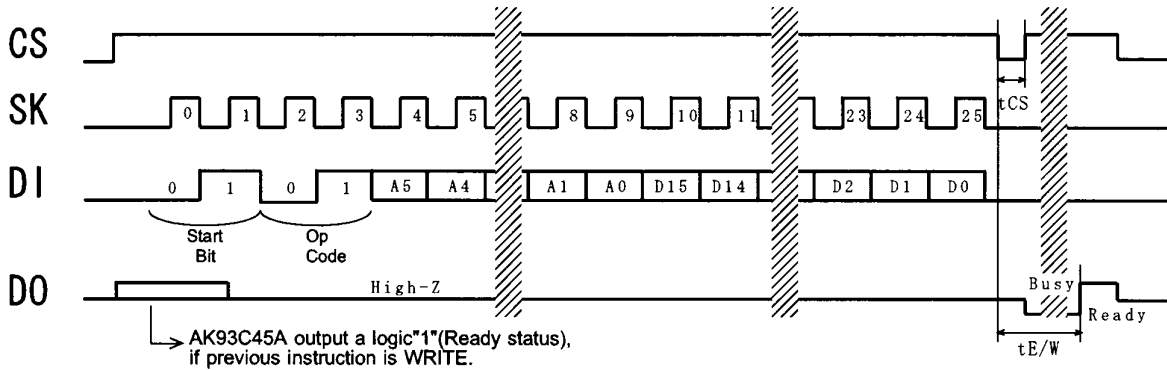
X: Don't care

table 4. Instruction Set for the AK93C75A

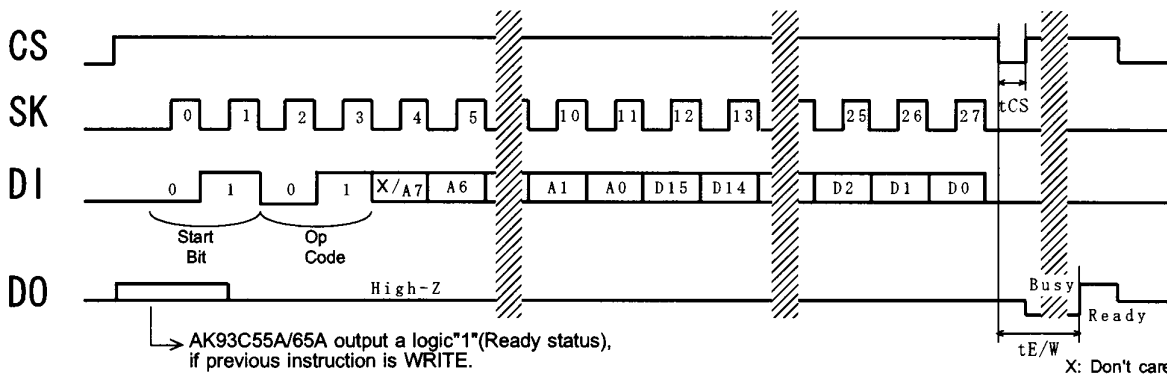
- (Note) • The WRAL instruction are used for factory function test only.
 User can't use the WRAL instruction.
 • The AK93C45A/55A/65A/75A perceives the start bit in the logic"1" and also "01".

Write

The write instruction is followed by 16 bits of data to be written into the specified address. After the last bit of data is put on the DI pin, the CS pin must be brought low before the next rising edge of the SK clock. This falling edge of the CS initiates the self-timed programming cycle. The DO indicates the $\overline{\text{Busy}}$ /Ready status of the chip if the CS is brought high after a minimum of 250ns (T_{cs}). DO=logical "0" indicates that programming is still in progress. DO=logical "1" indicates that the register at the address specified in the instruction has been written with the new data pattern contained in the instruction and the part is ready for a next instruction.

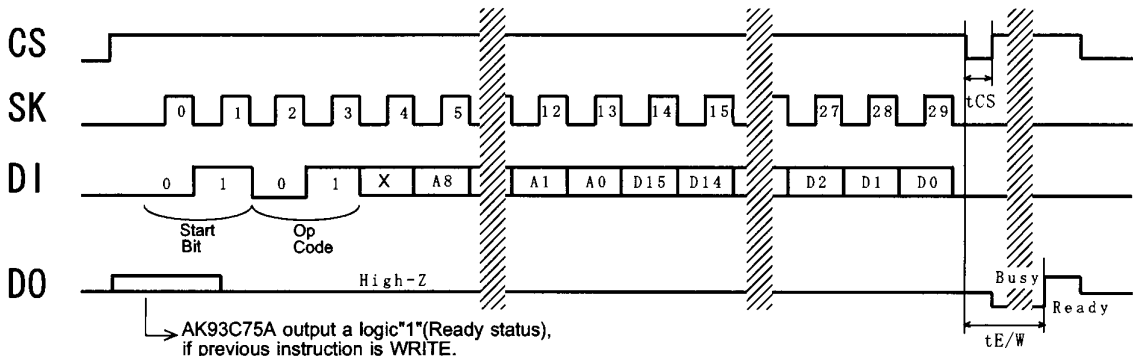


WRITE (AK93C45A)



*Address bit A7 becomes a "don't care" for AK93C55A.

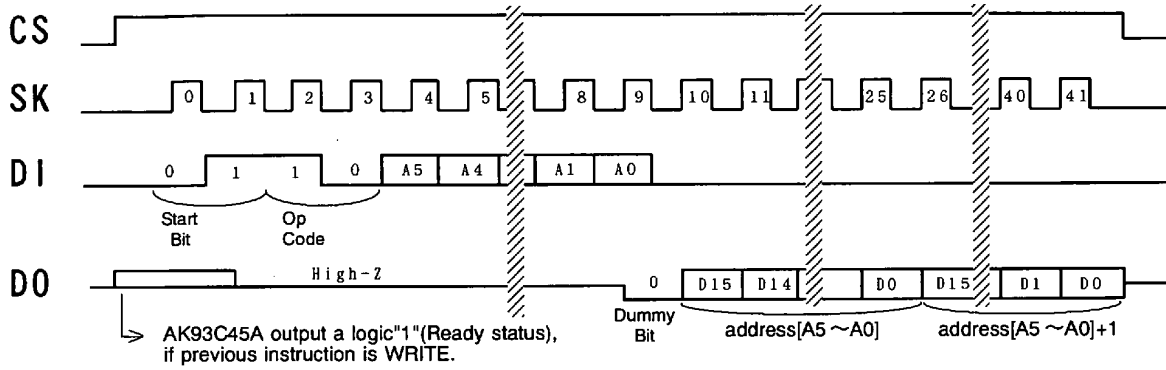
WRITE (AK93C55A/65A)



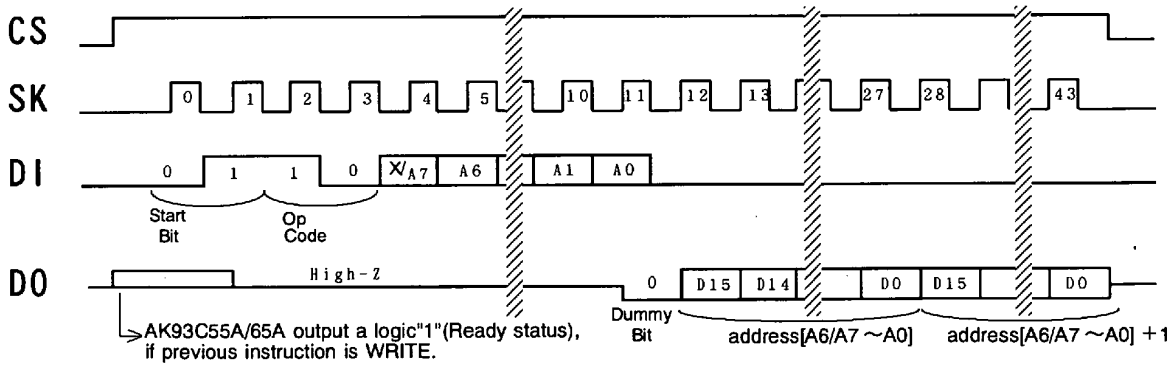
WRITE (AK93C75A)

Read

The read instruction is the only instruction which outputs serial data on the DO pin. Following the Start bit, first Op code and address are decoded, then the data from the selected memory location is available at the DO pin. A dummy bit (logical "0") precedes the 16-bit data from the selected memory location. The output data changes are synchronized with the rising edges of the serial clock (SK). The data in the next address can be read sequentially by continuing to provide clock. The address automatically cycles to the next higher address after the 16bit data shifted out. When the highest address is reached, the address counter rolls over to address \$00 or \$000 allowing the read cycle to be continued indefinitely.



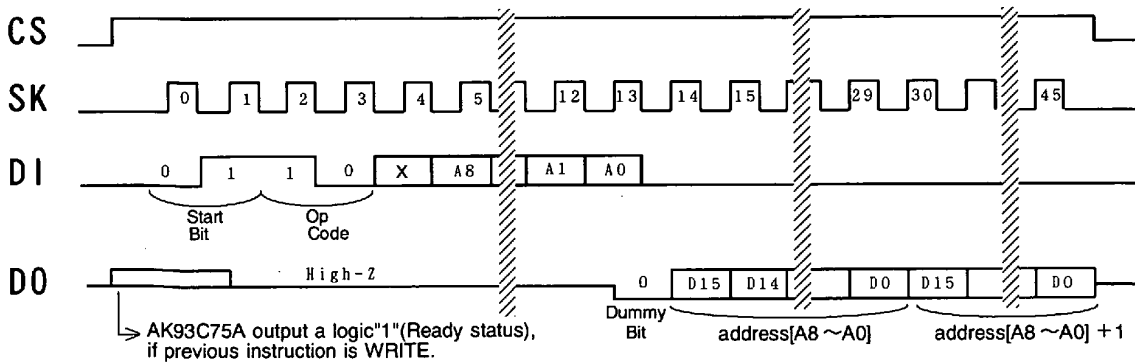
READ (AK93C45A)



X: Don't care

*Address bit A7 becomes a "don't care" for AK93C55A.

READ (AK93C55A/65A)



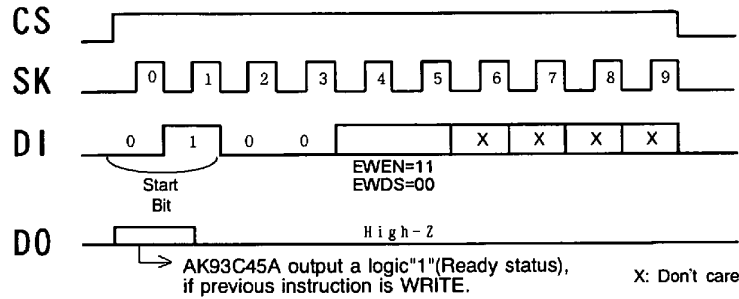
X: Don't care

READ (AK93C75A)

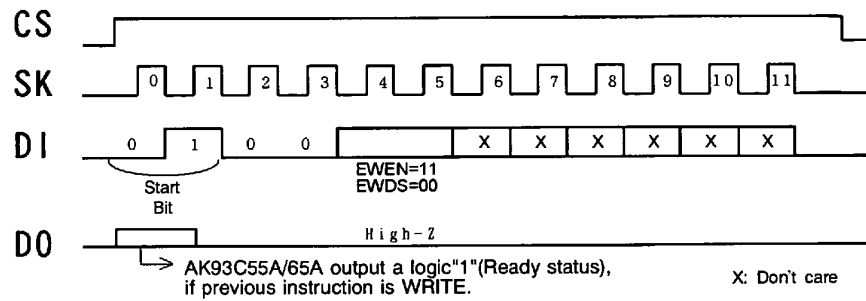
EWEN / EWDS

When Vcc is applied to the part, the part automatically powers up in the ERASE/WRITE Disable state. In the ERASE/WRITE disable state, execution of WRITE instruction is disable. Before WRITE instruction is executed, EWEN instruction must be executed. The ERASE/WRITE enable state continues until EWDS instruction is executed or Vcc is removed from the part.

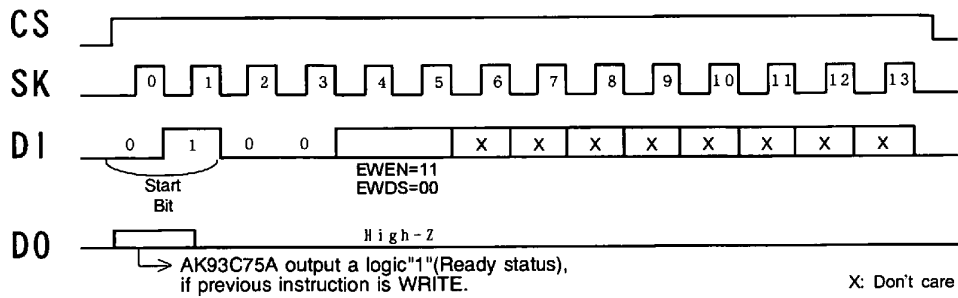
Execution of a read instruction is independent of both EWEN and EWDS instructions.



EWEN/EWDS (AK93C45A)



EWEN/EWDS (AK93C55A/65A)



EWEN/EWDS (AK93C75A)

| |
|---------------------------------|
| Absolute Maximum Ratings |
|---------------------------------|

| Parameter | Symbol | Min | Max | Unit |
|--|--------|------|---------|------|
| Power Supply | VCC | -0.6 | +7.0 | V |
| All Input Voltages with Respect to Ground | VIO | -0.6 | VCC+0.6 | V |
| Ambient storage temperature | Tst | -65 | +150 | °C |

Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum conditions for extended periods may affect device reliability.

| |
|--|
| Recommended Operating Condition |
|--|

| Parameter | Symbol | Min | Max | Unit |
|-------------------------------|--------|-----|-----|------|
| Power Supply | VCC | 1.8 | 5.5 | V |
| Ambient Operating Temperature | Ta | -40 | +85 | °C |

| |
|-----------------------------------|
| Electrical Characteristics |
|-----------------------------------|

(1) D.C. ELECTRICAL CHARACTERISTICS

◇ AK93C45A/55A/65A

(1.8V≤Vcc≤5.5V, -40°C≤Ta≤85°C, unless otherwise specified)

| Parameter | Symbol | Condition | Min. | Max. | Unit |
|---|--------|------------------------------|------------|----------|------|
| Current Dissipation (WRITE) | ICC1 | VCC=5.5V, tSKP=1us, *1 | | 4.0 | mA |
| | ICC2 | VCC=1.8V, tSK=4us,*1 | 93C45A | 1.5 | mA |
| | | | 93C55A/65A | 2.0 | mA |
| Current Dissipation (READ,EWEN,EWDS) | ICC3 | VCC=5.5V, tSKP=1us, *1 | | 0.5 | mA |
| | ICC4 | VCC=2.5V, tSKP=2us, *1 | | 0.2 | mA |
| | ICC5 | VCC=1.8V, tSKP=4us, *1 | | 0.1 | mA |
| Current Dissipation (Standby) | ICCSB | VCC=5.5V *2 | | 0.8 | uA |
| Input High Voltage | VIH1 | VCC=5V±10% | 2.0 | VCC+0.5 | V |
| | VIH2 | 2.5V≤VCC≤5.5V | 0.8×VCC | VCC+0.5 | V |
| | VIH3 | 1.8V≤VCC<2.5V | 0.8×VCC | VCC+0.5 | V |
| Input Low Voltage | VIL1 | VCC=5V±10% | -0.1 | 0.8 | V |
| | VIL2 | 2.5V≤VCC≤5.5V | -0.1 | 0.15×VCC | V |
| | VIL3 | 1.8V≤VCC<2.5V | -0.1 | 0.2×VCC | V |
| Output High Voltage | VOH1 | VCC=5V±10% IOH=-0.4mA | 2.2 | | V |
| | VOH2 | 2.5V≤VCC≤5.5V IOH=-0.1mA | 0.8×VCC | | V |
| | VOH3 | 1.8V≤VCC<2.5V IOH=-0.1mA | 0.8×VCC | | V |
| Output Low Voltage | VOL1 | VCC=5V±10% IOL=2.1mA | | 0.4 | V |
| | VOL2 | 2.5V≤VCC≤5.5V IOL=1.0mA | | 0.4 | V |
| | VOL3 | 1.8V≤VCC<2.5V IOL=0.1mA | | 0.4 | V |
| Input Leakage | ILI | VCC=5.5V,VIN=5.5V *3 | | ±1.0 | uA |
| Output Leakage | ILO | VCC=5.5V VOUT=5.5V,CS=GND | | ±1.0 | uA |

*1:VIN=VIH/VIL,DO=Open

*2:VIN=VCC/GND,CS=GND,DO=Open

*3:CS, SK, DI pin

◇ AK93C75A

(1.8V≤Vcc≤5.5V, -40°C≤Ta≤85°C, unless otherwise specified)

| Parameter | Symbol | Condition | Min. | Max. | Unit |
|---|--------|-------------------------------|-----------|-----------|------|
| Current Dissipation (WRITE) | ICC1 | VCC=5.5V, tSKP=1us, *4 | | 4.0 | mA |
| | ICC2 | VCC=1.8V, tSKP=4us, *4 | | 2.0 | mA |
| Current Dissipation (READ,EWEN,EWDS) | ICC3 | VCC=5.5V, tSKP=1us, *4 | | 0.4 | mA |
| | ICC4 | VCC=1.8V, tSKP=4us, *4 | | 0.1 | mA |
| Current Dissipation (Standby) | ICCSB | VCC=5.5V *5 | | 0.8 | uA |
| Input High Voltage | VIH | | 0.8 × VCC | VCC+0.5 | V |
| Input Low Voltage | VIL | | -0.1 | 0.2 × VCC | V |
| Output High Voltage | VOH1 | 2.5V≤VCC≤5.5V IOH=-0.1mA | 0.8 × VCC | | V |
| | VOH2 | 1.8V≤VCC<2.5V IOH=-0.1mA | 0.8 × VCC | | V |
| Output Low Voltage | VOL1 | 2.5V≤VCC≤5.5V IOL=1.0mA | | 0.4 | V |
| | VOL2 | 1.8V≤VCC<2.5V IOL=0.1mA | | 0.4 | V |
| Input Leakage | ILI | VCC=5.5V, VIN=5.5V *6 | | ±1.0 | uA |
| Output Leakage | ILO | VCC=5.5V VOUT=5.5V, CS=GND | | ±1.0 | uA |

*4: VIN=VIH/VIL, DO=Open

*5: VIN=VCC/GND, CS=GND, DO=Open

*6: CS, SK, DI pin

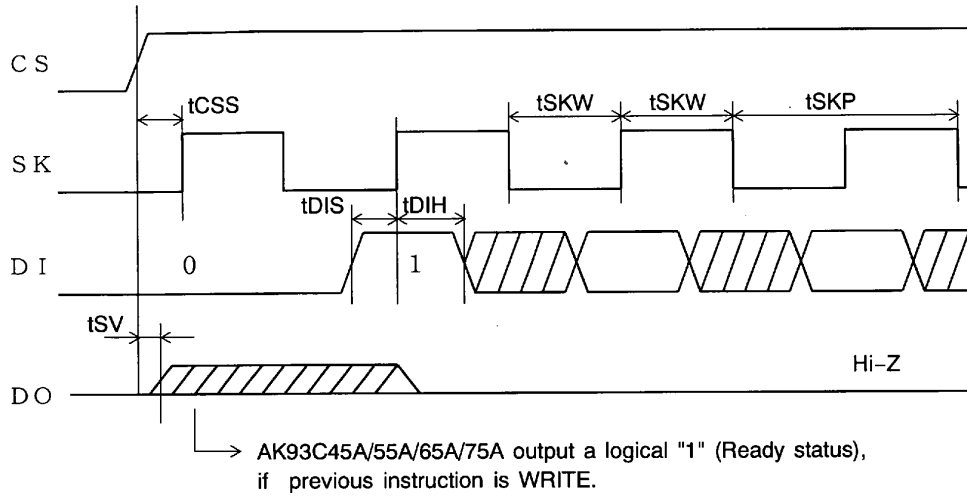
(2) A.C. ELECTRICAL CHARACTERISTICS

(1.8V≤VCC≤5.5V, -40°C≤Ta≤85°C, unless otherwise specified)

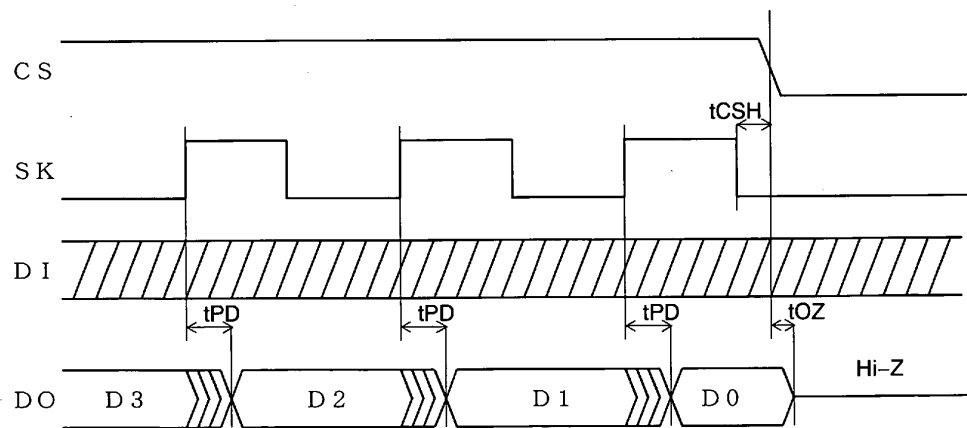
| Parameter | Symbol | Condition | Min. | Max. | Unit |
|-------------------------------|--------|----------------|---------------|------|------|
| SK Cycle Time | tSKP1 | 4.5V≤VCC≤5.5V | 1.0 | | us |
| | tSKP2 | 2.0V≤VCC<4.5V | 2.0 | | us |
| | tSKP3 | 1.8V≤VCC<2.0V | 4.0 | | us |
| SK Pulse Width | tSKW1 | 4.5V≤VCC≤5.5V | 500 | | ns |
| | tSKW2 | 2.0V≤VCC<4.5V | 1.0 | | us |
| | tSKW3 | 1.8V≤VCC<2.0V | 2.0 | | us |
| CS Setup Time | tCSS | | 100 | | ns |
| CS Hold Time | tCSH | | 0 | | ns |
| Data Setup Time | tDIS | | 200 | | ns |
| Data Hold Time | tDIH | | 200 | | ns |
| Output delay *7 | tPD1 | 4.5V≤VCC≤5.5V | | 500 | ns |
| | tPD2 | 2.0V≤VCC<4.5V | | 1.0 | us |
| | tPD3 | 1.8V≤VCC<2.0V | | 2.0 | us |
| Selftimed Programming Time | tE/W1 | 93C45A/55A/65A | | 10 | ms |
| | tE/W2 | 93C75A | 4.5V≤VCC≤5.5V | 8 | ms |
| | tE/W3 | | 1.8V≤VCC<4.5V | 10 | ms |
| Min CS Low Time | tCS | | 250 | | ns |
| CS to Status Valid | tSV | CL=100pF | | 500 | ns |
| CS to Output High-Z | tOZ1 | 2.0V≤VCC≤5.5V | | 100 | ns |
| | tOZ2 | 1.8V≤VCC<2.0V | | 250 | ns |

*7:CL=100pF

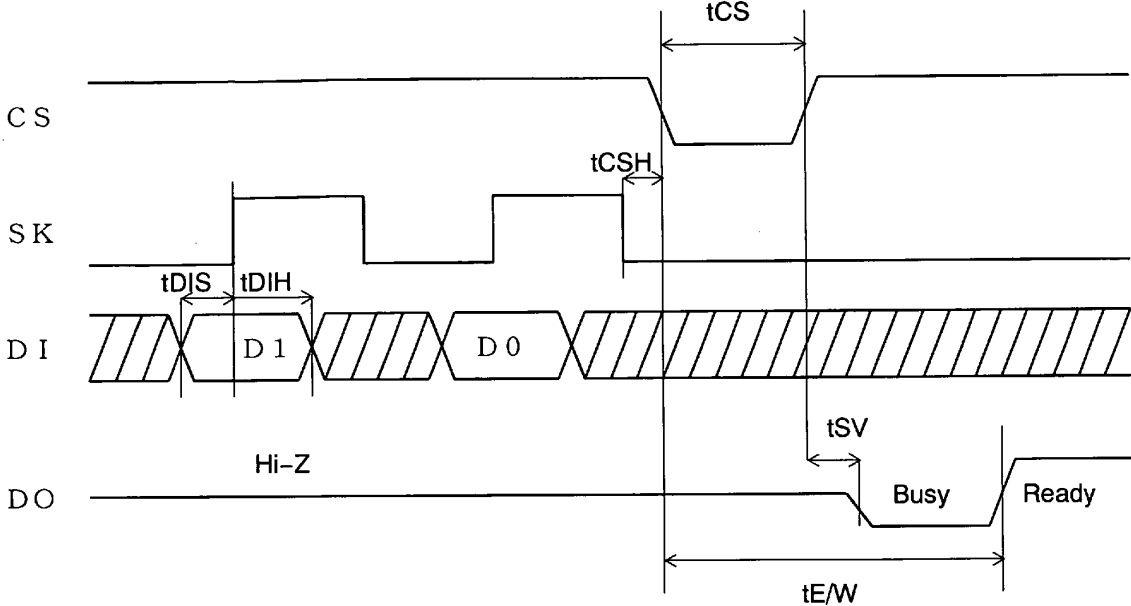
Synchronous Data Timing



The Start of Instruction



The End of Instruction



Busy/Ready Signal Output

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