Supertex inc.

AP01

T-43-25

8 Channel Power MOSFET Array
Monolithic P-channel Enchancement Mode

Ordering Information

BV_{DSS}/ BV_{DGS} (min)	$R_{DS(ON)}$ (max)	$I_{D(ON)}$ (min)	I_{DSS}** @ V_{DS} = -100V Max	I_{DSS}** @ V_{DS} = -250V Max	Order Number / Package			
					18-Lead Ceramic DIP	18-Lead Plastic DIP	Plastic SOW-20*	Die
-160V	700Ω	-15mA	-1.5nA	—	AP0116NB	AP0116NA	AP0116WG	AP0116ND
-200V	600Ω	-15mA	—	—	AP0120NB	AP0120NA	—	AP0120ND
-300V	600Ω	-15mA	—	—	AP0130NB	AP0130NA	—	AP0130ND
-320V	700Ω	-15mA	—	-1.5nA	AP0132NB	AP0132NA	AP0132WG	AP0132ND
-400V	700Ω	-15mA	—	—	AP0140NB	AP0140NA	AP0140WG	AP0140ND

*Same as SO-20 with 300 mil wide body.
**Average current per channel, measured with all eight channels connected in parallel.

Features

- ☐ Low drain to source leakage for AP0116 and AP0132
- ☐ 200-volt to 400-volt capability
- ☐ Interfaces directly to CMOS logic
- ☐ 8 independent channels
- ☐ Low crosstalk between channels
- ☐ Low power dissipation
- ☐ Pin compatible with industry standard driver array
- ☐ Freedom from secondary breakdown

Applications

- ☐ High voltage electroluminescent panel drivers
- ☐ High voltage electrostatic array drivers
- ☐ General multi-channel driver array

Absolute Maximum Ratings

Drain-to-Source Voltage	BV_{DSS}
Drain-to-Gate Voltage	BV_{DGS}
Gate-to-Source Voltage	± 20V
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature*	300°C
Channel-to-Channel Crosstalk	10mV/V

*Distance of 1.6 mm from case for 10 seconds.

General Description

The Supertex AP01 series of high voltage arrays is designed to provide the interface between MOS logic and loads requiring high voltages and intermediate currents. Each circuit consists of eight channels in a common-source configuration with open drains. This design minimizes the number of package leads needed.

The AP0116 and AP0132 are ideally suited for low leakage/high impedance measurement, providing excellent accuracy and resolution for Automatic Test Equipment.

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Thermal Characteristics

Package	I_D (continuous)*	I_D (pulsed)*	Power Dissipation @ T_C = 25°C	θ_{ja} °C/W	θ_{jc} °C/W	I_{DR}	I_{DRM}*
18 lead plastic	−15mA	−40mA	1.5W	135	83	−15mA	−40mA
18 lead Ceramic	−15mA	−40mA	2.0W	85	62	−15mA	−40mA

* I_D (continuous) is limited by max rated T_j.

Electrical Characteristics (@ 25°C unless otherwise specified)

(Notes 1, 2 and 3)

Symbol	Parameter		Min	Typ	Max	Unit	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	AP0116 AP0120 AP0130 AP0132 AP0140	−160 −200 −300 −320 −400			V	I_D = −100µA, V_{GS} = 0V
$V_{GS(th)}$	Gate Threshold Voltage		−2		−5	V	V_{GS} = V_{DS}, I_D = −1mA
$\Delta V_{GS(th)}$	Change in $V_{GS(th)}$ with Temperature			−3.5		mV/°C	V_{GS} = V_{DS}, I_D = −1mA
I_{GSS}	Gate Body Leakage	AP0120 AP0130 AP0140			−10	nA	V_{GS} = ±20V, V_{DS} = 0
		AP0116 AP0132			−1	nA	V_{GS} = ±20V, V_{DS} = 0 (Note 3)
I_{DSS}	Zero Gate Voltage Drain Current	AP0120			−1	µA	V_{GS} = 0, V_{DS} = Max Rating
		AP0130 AP0140			−1	mA	V_{GS} = 0, V_{DS} = 0.8 Max Rating T_A = 125°C
		AP0116			−1.5	nA	V_{GS} = 0, V_{DS} = −100V (Note 3)
					−1	mA	V_{GS} = 0, V_{DS} = 0.8 Max Rating T_A = 125°C
		AP0132			−1.5	nA	V_{GS} = 0, V_{DS} = −250V (Note 3)
					−1	mA	V_{GS} = 0, V_{DS} = 0.8 Max Rating T_A = 125°C
$I_{D(ON)}$	ON-State Drain Current		−15			mA	V_{GS} = −10V, V_{DS} = −25V
$R_{DS(ON)}$	Static Drain-to-Source ON-State Resistance	AP0120 AP0130			600	Ω	V_{GS} = −10V, I_D = −10mA
		AP0116 AP0132 AP0140			700	Ω	V_{GS} = −10V, I_D = −10mA
$\Delta R_{DS(ON)}$	Change in $R_{DS(ON)}$ with Temperature			0.8		%/°C	V_{GS} = −10V, I_D = −10mA
G_{FS}	Forward Transconductance		3.0	5.0		m℧	V_{DS} = −25V, I_D = −5mA
C_{ISS}	Input Capacitance			5.0	7.5	pF	V_{DS} = −25V, V_{GS} = 0 f = 1 MHz
C_{OSS}	Common Source Output Capacitance			3.0	5.0		
C_{RSS}	Reverse Transfer Capacitance			1.0	2.0		
$t_{d(ON)}$	Turn-ON Delay Time			3		ns	V_{DS} = −25V I_D = −10mA R_S = 50Ω, $V_{GS(ON)}$ = −10V
t_r	Rise Time			3			
$t_{d(OFF)}$	Turn-OFF Delay Time			5			
t_f	Fall Time			3			
V_{SD}	Diode Forward Voltage Drop				1.5	V	V_{GS} = 0, I_{SD} = −25mA

Note 1: All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300ms pulse, 2% duty cycle.)
Note 2: All A.C. parameters sample tested.
Note 3: Average current per channel, measured with all 8 channels connected in parallel.

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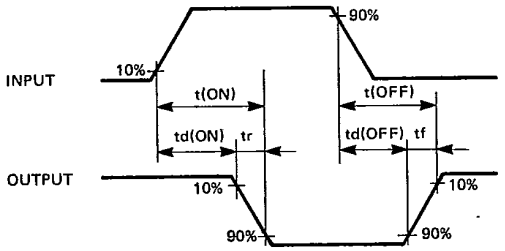
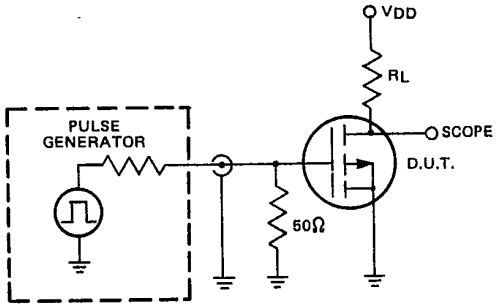
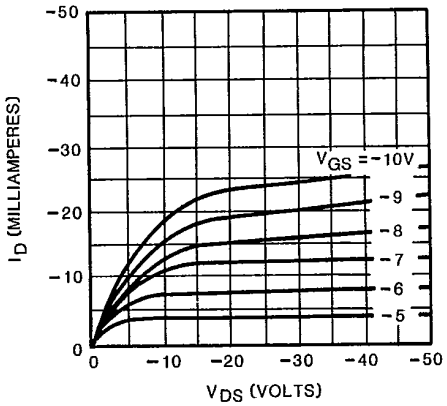
Switching Waveforms and Test Circuit



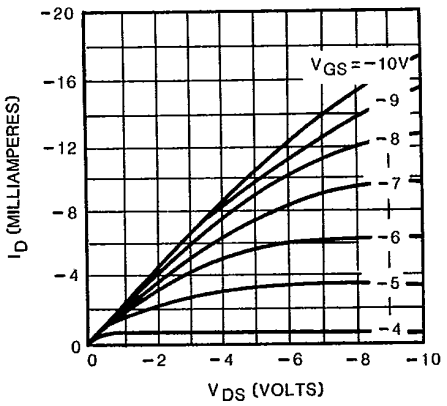


Typical Performance Curves

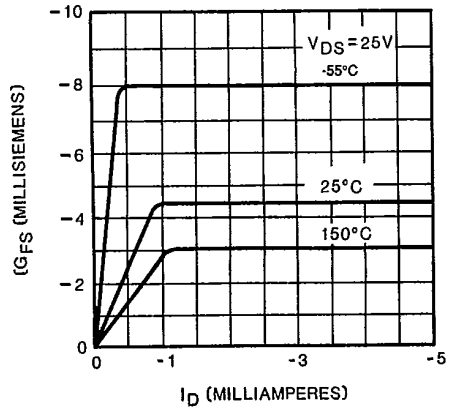
Output Characteristics



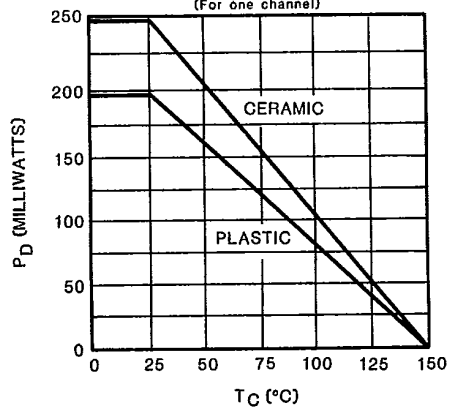
Saturation Characteristics



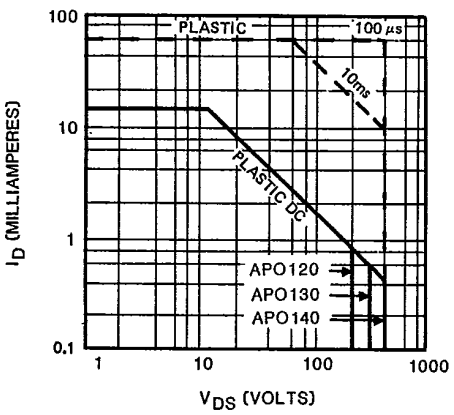
Transconductance Vs. Drain Current



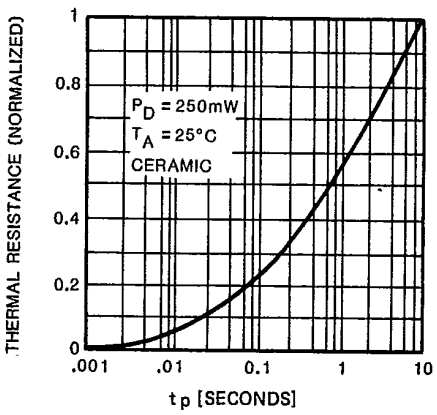
Power Dissipation Vs. Case Temperature
(For one channel)



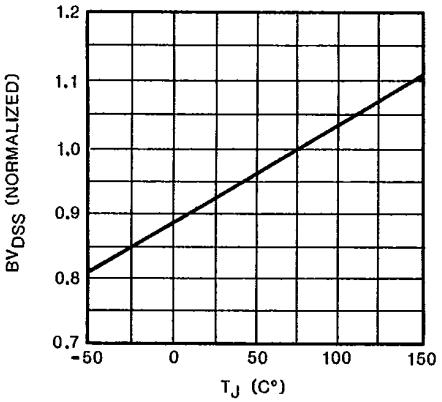
Maximum Rated Safe Operating Area



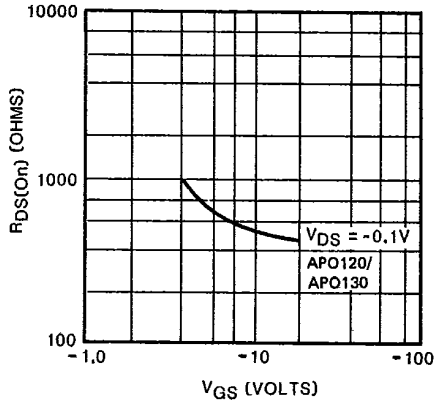
Thermal Response Characteristics



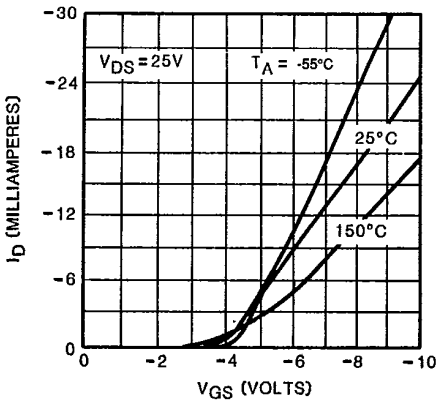
BVDSS Variation with Temperature



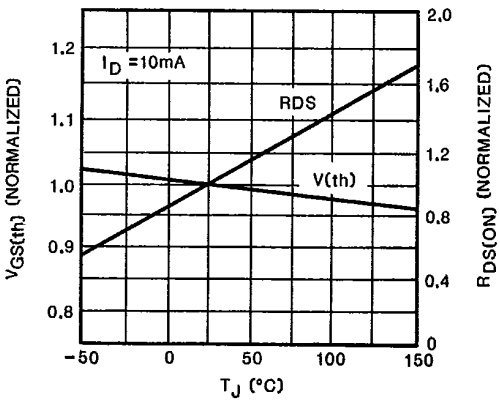
ON-Resistance Vs. Gate-to-Source Voltage



Transfer Characteristics



V(th) and RDS Variation with Temperature



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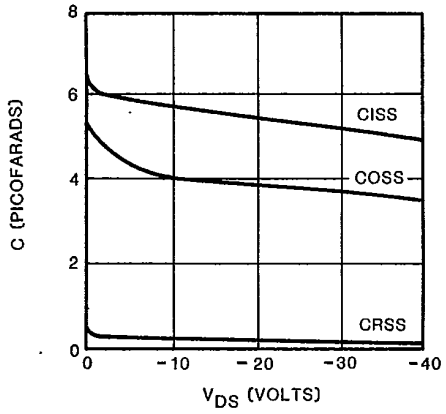
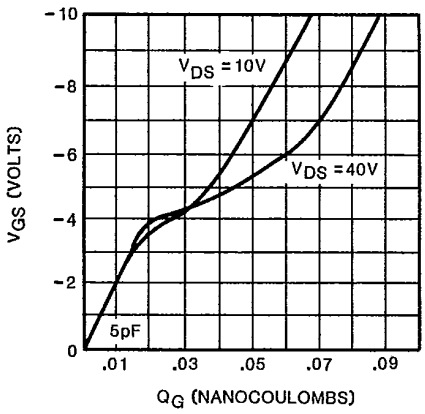
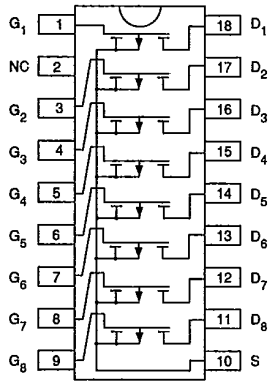
Capacitance Vs. Drain-to-Source Voltage



Gate Drive Dynamic Characteristics

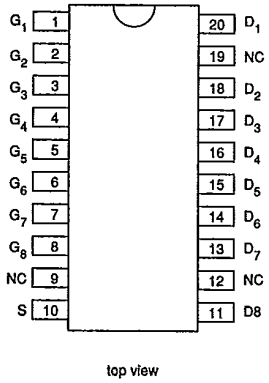


Pin Configuration and Schematic



top view

18-pin DIP



top view

SOW-20

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