Audio Mixer

Note:
If not otherwise designated the pin numbers mentioned refer to the 24–pin DIL package.

1. Introduction

The AMU 2481 Audio Mixer is a digital real–time signal processor in NMOS technology, housed in a 24–pin Dil plastic package or in a 44–pin PLCC package. It is designed to perform digital processing of both TV audio information and digital audio data supplied by the DMA 2271 D2–MAC Decoder. The architecture of the AMU 2481 combines two main blocks:

– I/O blocks

– DSP block

The I/O blocks are used to manage the input and output of audio information. The DSP block consists of a mask–programmable digital signal processor, whose software can be controlled by a microprocessor (CCU) via the IM bus. So parameters like coefficients can be modified during performance. By means of the DSP software, audio functions, such as deemphasis, oversampling mixing and volume control are performed. Fig. 1–1 gives an overview over the AMU's functions.

1.1. Application of the AMU 2481

The AMU 2481 Audio Mixer is designed to interface with ITT's ADC 2311 E Audio A/D Converter, DMA 2271 D2–MAC Decoder on the input side, and with the APU 2471 or the ACP 2371 Audio Processors on the output side. It can receive digital audio data in two different formats:

Via the PDM inputs, the AMU 2481 is supplied with two 1–bit PDM data streams produced by the ADC 2311 E Audio A/D Converter which receives analog audio information either from the SCART interface (Euro connector), which is used, e.g., for video recorder connection, or from any terrestrial TV transmission. For this input format, decimation filters are provided in the AMU 2481, which convert each PDM stream into a 16–bit word at a sampling rate of approximately 32 kHz.

Via the S bus interface the AMU 2481 receives serial audio data, provided, e.g., by the DMA 2271 D2–MAC Decoder.

Fig. 1–2 shows how the AMU 2481 can be used together with the mentioned ICs of ITT to realize multistandard audio processing with PAL and D2–MAC signals. In the following descriptions data coming from the ADC will be called "PDM data" and data coming from the DMA will be called "S data".

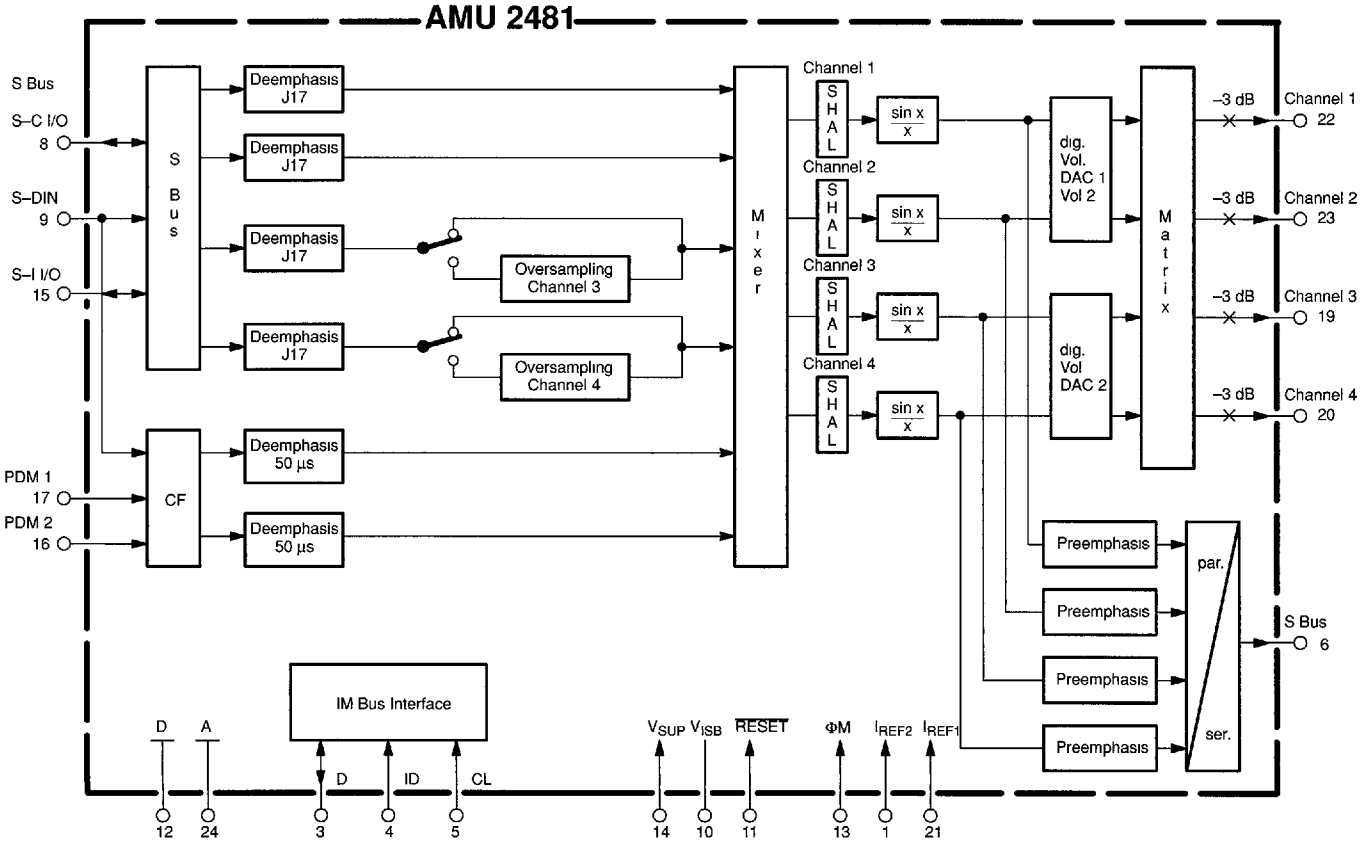


Fig. 1–1: Functional block diagram of the AMU 2481

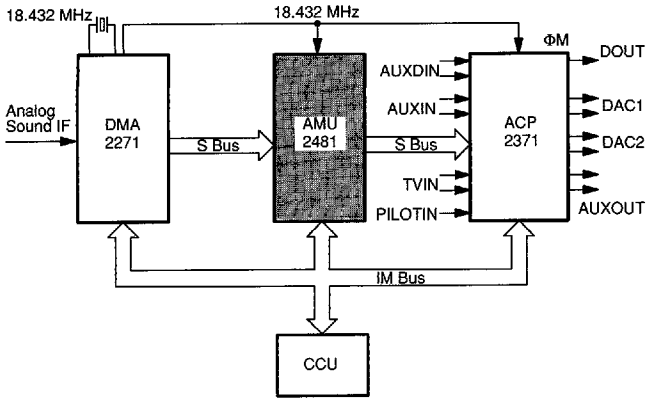


Fig. 1–2: Multistandard audio system with AMU 2481

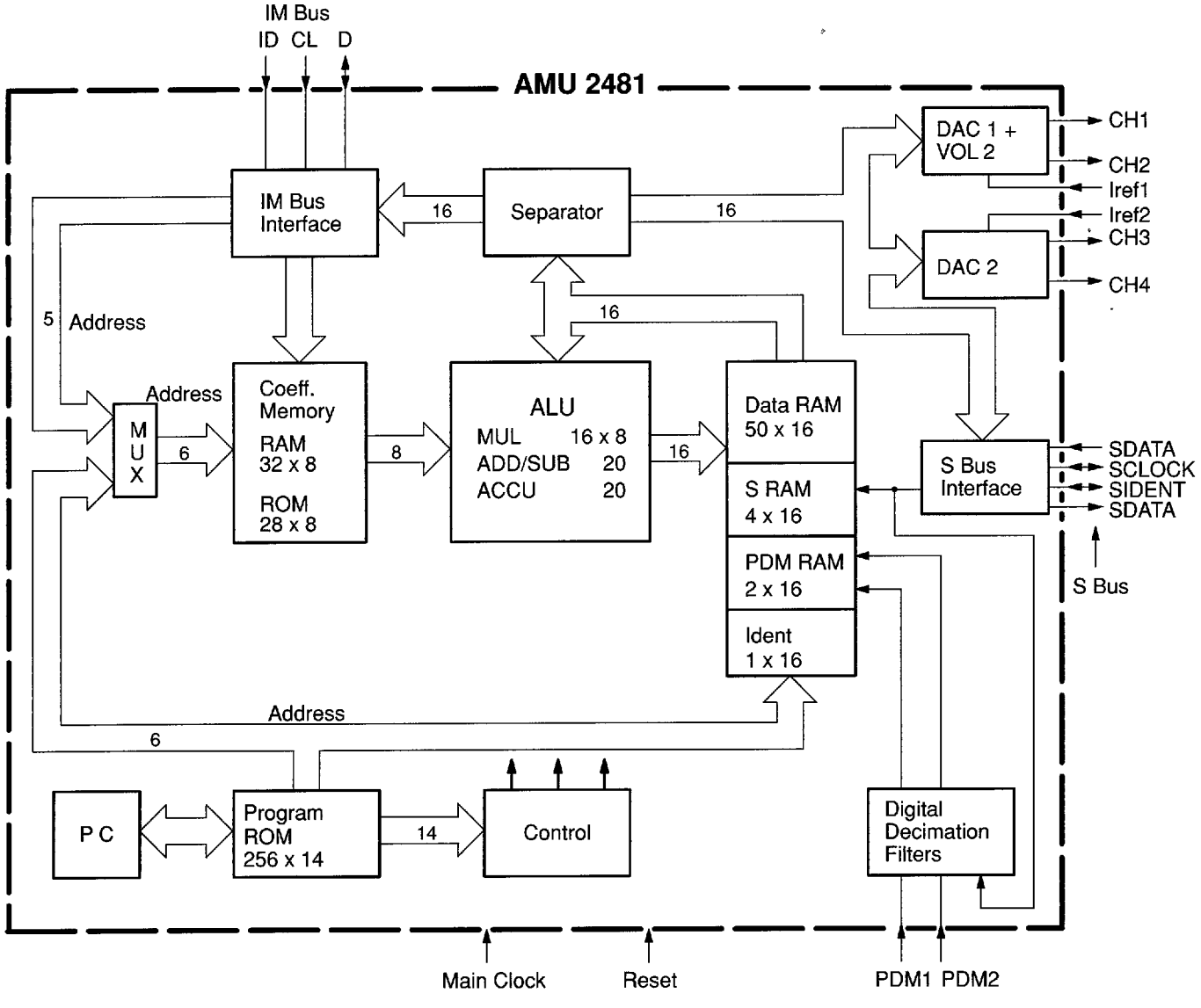


Fig. 1–3: AMU 2481 architecture

2. Architecture of the AMU 2481 and Functional Description

As already mentioned in section 1., the AMU 2481 architecture combines two main parts, the I/O blocks and the DSP core. Fig. 1–3 shows a block diagram of the architecture.

2.1. I/O Blocks

2.1.1. Digital Decimation Filters

The digital decimation filters are cascades of transversal and recursive lowpass filters. They are required to convert the two 1–bit PDM data streams by stepwise reduction of bandwidth and word rate (sampling rate) into two PCM data streams with 16 bit word length and a sampling rate of approximately 32 kHz, which in the following are called PCM data 1 and 2. They are temporarily stored in the corresponding locations of the AMU's data RAM.

As the two PDM data streams at the input of the decimation filters have no separate clock signal, the decimation filters are equipped with a synchronization facility. This feature also supplies the AMU software with the sampling clock (approx. 32 kHz), which is called "I/O Sync" or IOSYNC. More details on data/clock timing can be found in section 2.3.

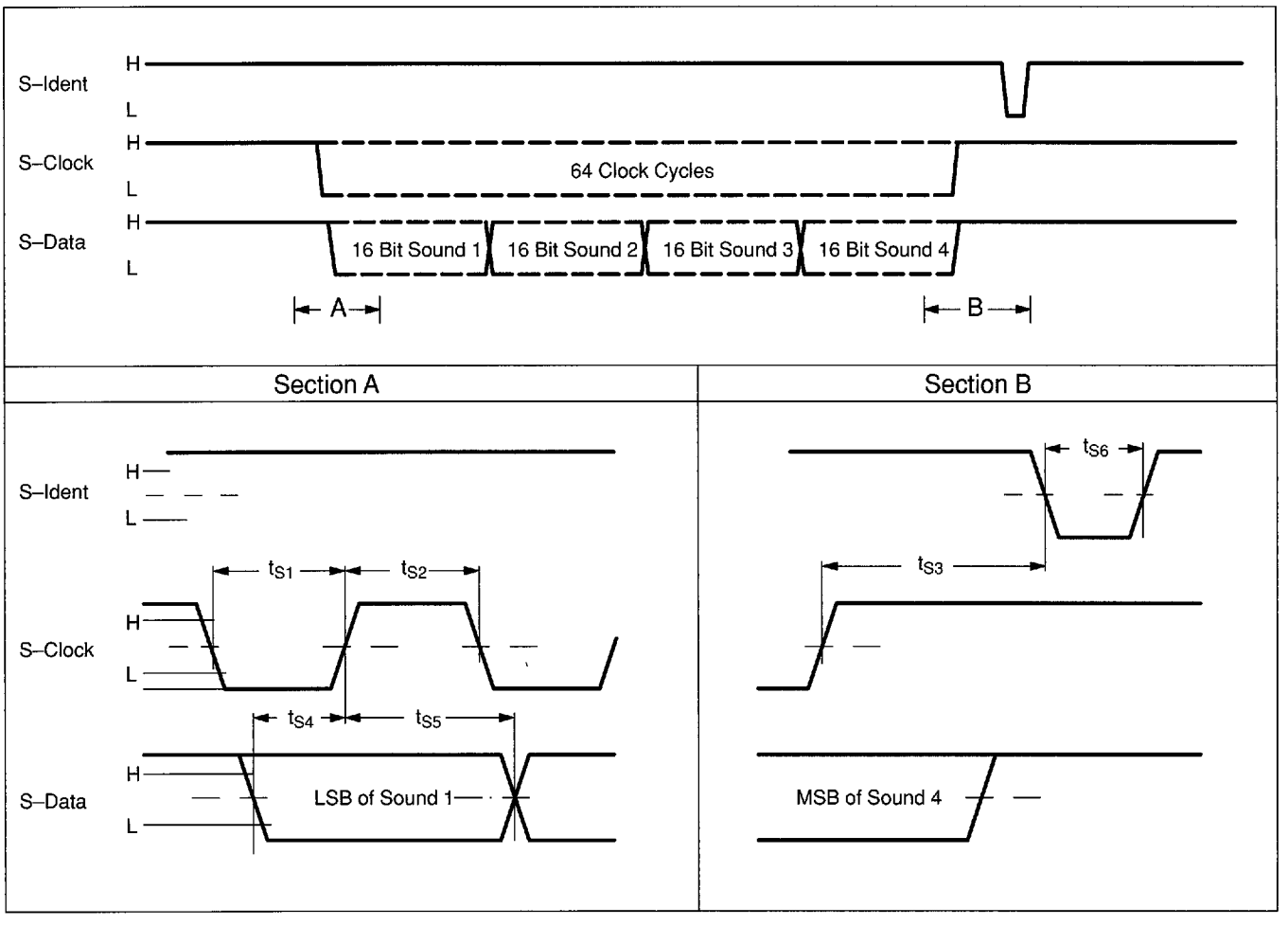


Fig. 2–1: S bus waveforms

2.1.2. S–Bus Interface and S–Bus

2.1.2.1. Description of the S–Bus

The S–bus was designed to connect the digital sound output of the DMA 2271 D2/MAC Decoder to audio–processing ICs such as the AMU 2481 Audio Mixer or the APU 2471 Audio Processor etc., and to connect these ICs with each other. The S–bus is an unidirectional, digital bus which transmits the sound information in one direction only, so that it is not necessary to solve priority problems on the bus.

The S–bus consists of the three lines S–Clock, S–Ident and S–Data. The DMA 2271 generates the signals S–Clock and S–Ident, which control the data transfer to and between the various processors which follow the DMA 2271. For this, the S–Clock and S–Ident inputs of all processors in the system are connected to the S–Clock and S–Ident outputs of the DMA 2271. S–data output of the DMA 2271 is connected to the S–Data input of the next following AMU, the AMU's S–Data output is connected to the APU's S–Data input and so on.

The sound information is transmitted in frames of 64 bits, divided into four successive 16–bit samples. Each sample represents one sound channel. The timing of a complete transmission of four samples is shown in Fig. 2–1, the times are specified in "Recommended Operating Conditions". The transmission starts with the LSB of the first sample. The S–Clock signal is used to write the data into the receiver's input register. The S–Ident signal marks the end of one frame of 64 bits and is used as latch pulse for the input register. The repetition rate of the S–Ident pulses is identical to the sampling rate of the D2–MAC sound signal; thus it is possible to transfer four sound channels simultaneously.

2.1.2.2. The S–Bus Interface

The S–bus interface of the AMU 2481 mainly consists of an input and an output register, each 64–bit wide. The timing to write or read bit by bit is supplied by the S–Clock signal. In the case of an S–Ident pulse, the contents of the input register are transferred to the data RAM (see section 2.2.1.) and the contents of the output register are written to the S–Data output.

The S–Ident is also used as the sampling rate reference for the DSP software in the case of digital source mode. In this mode the IOSYNC generated by the decimation filters is locked to the S–Ident. This allows a mixed mode: S–Data and PDM Data can be processed simultaneously. In this case, however, there must be the same audio sample rate of PDM data and S–bus data (see 2.3.). If this is not the case, the S–Ident line has to be disabled.

By means of coefficient k33 (see section 3.13.) the AMU 2481 can be switched to an S–bus slave mode (bit 4 = 0) or to an S–bus master mode (bit 4 = 1). The slave mode is required in an application as shown in Fig. 1–2 where the DMA 2271 D2–MAC Decoder acts as master on the S–bus, i.e. the DMA 2271 supplies the S–Clock and S–Ident signals as well as the S–Data input signal.

To enable parallel cascading of AMUs without external switches, (e.g. NICAM to SCART and D2MAC to TV) in the 44–PLCC package, the SBUS signals S–Ident and S–Clock, (and the Main Clock, see section 2.3.) can be passed through the AMU 2481. The corresponding open–drain outputs can be switched to high impedance, which is the default status after power–on reset. To switch them on or off (high imp.), use the same bit that controls the SBUS data output:

k33 bit3 = 0 outputs = active
= 1 outputs = high impedance

2.1.3. IM Bus Interface and IM Bus

2.1.3.1. Description of the IM Bus

The INTERMETALL Bus (IM Bus for short) was designed to control the DIGIT 2000 ICs by the CCU Central Control Unit. Via this bus the CCU can write data to the ICs or read data from them. This means the CCU acts as a master whereas all controlled ICs are slaves.The IM bus consists of three lines for the signals Ident (ID), Clock (CL) and Data (D). The clock frequency range is 50 Hz to 170 kHz. Ident and clock are unidirectional from the CCU to the slave ICs, Data is bidirectional. Bidirectionality is achieved by using open–drain outputs with On–resistances of 150 Ohm maximum. The 2.5 kOhm pull–up resistor common to all outputs is incorporated in the CCU.The timing of a complete IM bus transaction is shown in Fig. 2–2 and in the "Recommended Operating Conditions". In the non–operative state the signals of all three bus lines are High. To start a transaction the CCU sets the ID signal to Low level, indicating an address transmission, then sets the CL signal to Low level and switches the first bit on the Data line.Then eight address bits are transmitted, beginning with the LSB. Data takeover in the slave ICs occurs at the positive edge of the clock signal. At the end of the address byte the ID signal goes High, initiating the address comparison in the slave circuits. In the addressed slave the IM bus interface switches over to Data read or write, because these functions are correlated to the address.

Also controlled by the address the CCU now transmits eight or sixteen clock pulses, and accordingly one or two Bytes of data are written into the addressed IC or read out from it, beginning with the LSB. The completion of the bus transaction is signalled by a short Low state pulse of the ID signal. This initiates the storing of the transferred data.

It is permissible to interrupt a bus transaction for up to 10 ms.

For future software compatibility, the CCU must write a zero into all bits not used at present. When reading undefined or unused bits, the CCU must adopt "don't care" behavior.

2.1.3.2. IM Bus Interface

To write coefficient value(s) into the AMU2481 registers the following steps have to be taken:

1. addressing the AMU2481 (allows multiprocessor system)
2. writing of 8 bit data into the IM bus interface registers

After having completed step 1, step 2 can be performed as often as the communication between AMU 2481 and CCU is required, on the condition that the processor address has not been changed by the CCU.

Comments to the steps mentioned above: The syntax of step 1 is identical to that of step 2. The CCU transmits an 8–bit address to the IM bus interface of the AMU 2481, addressing a certain register or C–RAM location of the AMU. The IM bus interface has to check this address and if necessary, to store it and the following 8 data bits into special IM bus interface registers. Transfer of the data bits to the corresponding C–RAM locations is then performed by the AMU hardware at the sampling rate. Transmission of one Byte (8 bits) takes 100 µs. A spacing of 30 µs must be provided between the end of one transmission and the start of the next one.

In the case of addressing the AMU 2481 (step 1 above), the address transmitted first is 102 (= select register). If the following 8–bit data is identical to 15, the AMU 2481 will accept further IM bus data. This kind of selective addressing allows controlling of different AMU and APU types (e.g. "selectword" of APU 2471 = 00, "selectword of AMU 2481 VS = 14) in a multi–APU system without using different address ranges. Each APU/AMU type will have its own mask–programmed "selectword".

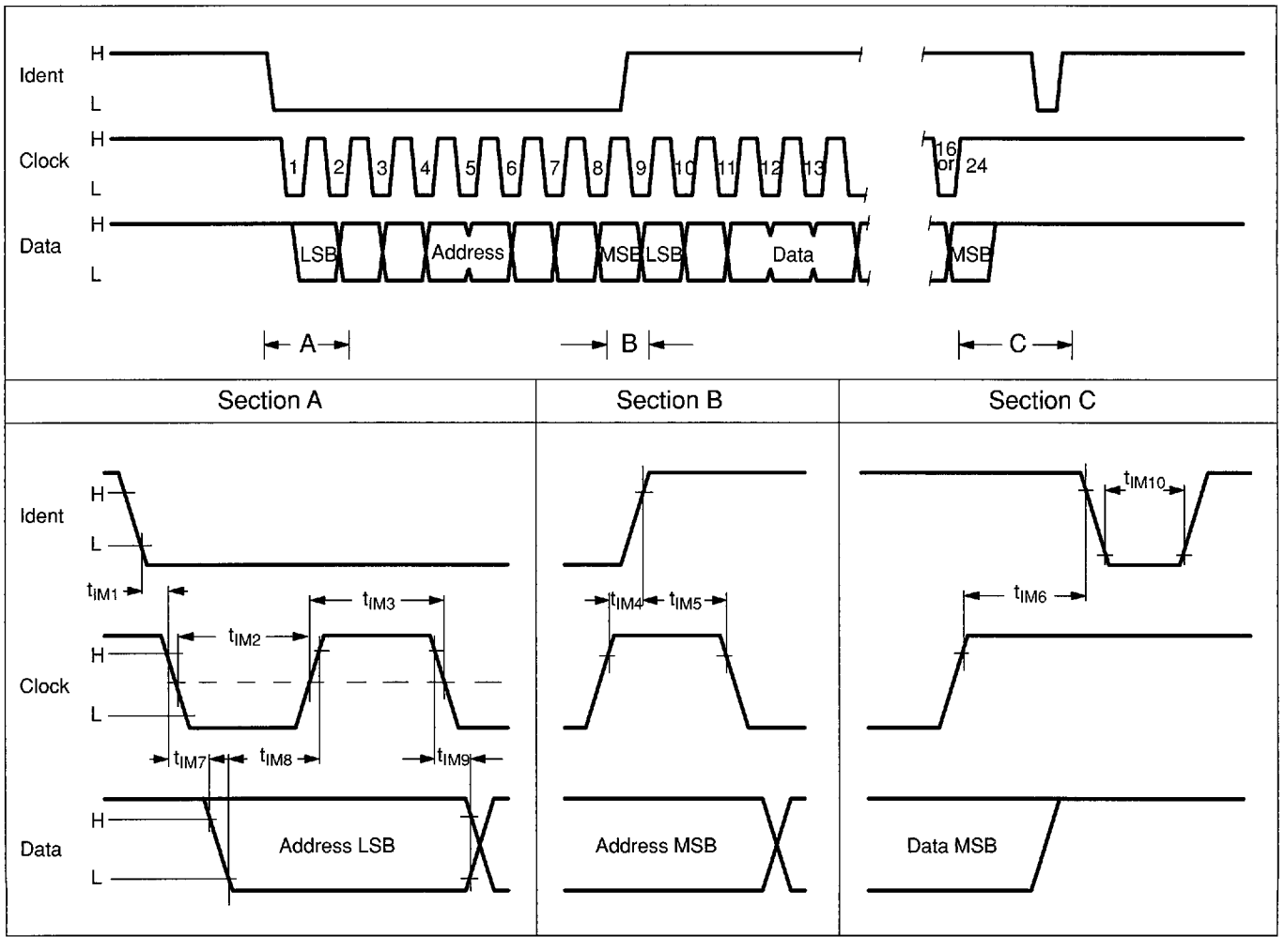


Fig. 2–2: IM bus waveforms

2.1.4. Digital/Analog Converter (DAC) and Volume 2

Digital to analog conversion is performed by four special conversion circuits. The channels 1 and 2 are assigned to DAC 1, channels 3 and 4 to DAC 2. At any time, the current level of the output signals depends on the value of the reference currents, which are fed to pin 21 (for DAC 1) and to pin 1 (for DAC 2). Fig. 2–3 gives application diagrams for the DAC circuits. The RC network connected to the outputs is required for suppressing the clock from the D/A conversion (1 nF). To achieve an analog deemphasis of 50 µs, the 1 nF capacitors must be enlarged to the 10 nF. To improve the signal–to–noise ratio of the AMU 2481 (especially for low volume settings) an additional volume control facility (Vol 2) is provided after the DAC 1 D/A converters. A digitally–adjusted attenuator acts in 29 steps of 1 dB each.

Note:
There is an application restriction with these converters: The clock rate of the AMU must meet the following clock condition:

Clock rate = sampling rate · n · 16

n must be an integer value. In section 2.3. all clocks relevant for the AMU application are listed. They fulfill that condition.

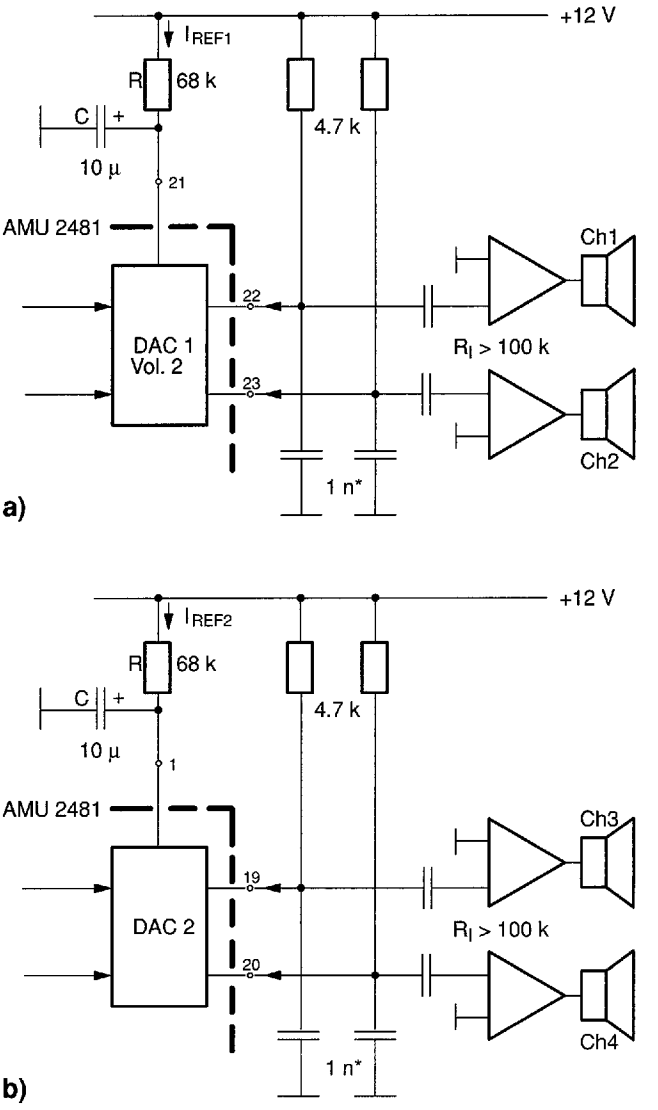


Fig. 2–3: DAC application diagrams
a) DAC 1 Interface
b) DAC 2 Interface

*) optionally 10 nF for 50 µs analog deemphasis

2.2. DSP Block

The AMU 2481 contains a complete mask–programmable digital signal processor with the blocks as described in the following sections.

2.2.1. C–RAM, C–ROM and Data RAM

Coefficients and control parameters for digital processing of audio data are either fixed or variable by means of the CCU. The coefficient (C) memory is therefore divided into two parts:

C–RAM, containing 32 locations of 8 bits each, which can be loaded by the CCU via the IM bus interface. The AMU software needs 32 variable parameters, and for proper processing all locations must be loaded with the corresponding values.

C–ROM, containing 28 locations of 8 bits each, which are loaded with fixed values, required for the DSP software. For the user there is no possibility to change coefficients in the C–ROM. Input data and intermediate results can be stored in the AMU's Data RAM whose locations have 16 bits each. This RAM is arranged in the following way:

– 50 locations for intermediate results and output data

– 4 locations for S bus input channels

– 2 locations for 2 PDM channels from the decimation filters

2.2.2. Program ROM, Program Counter and Control Block

The DSP software of the AMU 2481 is stored in the program ROM. Its size is 256 · 14 bits, and its content cannot be modified by the user because it is mask–programmed. Program ROM is addressed by the program counter (P.C.), which is a preset table counter.

Instruction decoding and coordinating of all time functions is performed by the control block. Multiplexing of the two busses, addressing the coefficient memory and controlling the separator are also tasks of the control block. By means of the separator, data are transferred to the DACs.

2.2.3. Arithmetic Logic Unit (ALU)

The core of the DSP block is the ALU. Multiplication of 16 · 8 bit, addition using a 20–bit accumulator, and shift operations are performed in the ALU. Accumulation is done according to a saturation characteristic (see section 3.1.).

2.3. System Clock ΦM and PDM Sampling Rate

The clock at the AMU's ΦM input is dependent on the current TV standard. The AMU is mainly provided for the German TV stereo system PAL and digital source standard (e.g. D2–MAC). In all cases, the physical source of the AMU's system clock is the DMA 2271 D2–MAC Decoder (Fig.1–2):

Table 2–1: Selection of operation mode by k33

Mode	k 33, Bit 6
PAL D2–MAC	0 1

1. For **PAL mode**, the system clock ΦM is derived from the color carrier frequency, for example in the MCU 2600 Clock Generator IC, and transferred to the DMA 2271 to be passed on to the AMU. In the ADC, as well as in the AMU, the ΦM clock is divided by four to produce the PDM rate, and by 128 to generate the sampling rate.

2. For **digital source** (S bus) operation, the AMU system clock ΦM is generated in the DMA 2271 in such a way that it is a multiple of the D2–MAC typical audio sampling frequency. The S bus signals S–Clock and S–Ident are then derived from this clock.

Table 2–2 gives details about the clock requirements of the above operation modes. Selection of the operation mode (clock dividers) has to be transmitted by the CCU by means of coefficient k33, Bit 6 (see table 2–1, also section 3.13.).

To enable parallel cascading of AMUs without external switches, (e.g. NICAM to SCART and D2MAC to TV) in the 44–PLCC package, the main clock (the S–Clock and the S–Ident, see section 2.1.2.2.) can be passed through the AMU 2481. The push–pull output can be switched to high impedance, which is the default status after power–on reset. To switch it on or off, use the same bit that controls the SBUS output:

k33 bit3 = 0 outputs = active
= 1 outputs = high impedance

Table 2–2: AMU system clock ΦM and derived sampling rates

TV Standard	AMU ΦM	PDM Rate	Sampling Rate
PAL D2–MAC	17.73 MHz 18.432 MHz	:4 = 4.43 MHz –	:128 = 34.63 kHz :576 = 32 kHz

3. Functions Solved by DSP Software

3.1. Representation of Numbers

The AMU 2481 has a two's complement, fixed point arithmetic with decimal point being left-hand and the MSB being the sign bit. The word lengths are defined as follows:

coefficients:	8 bits including sign bit
data at multiplier input:	16 bits including sign bit
intermediate results:	20 bits including sign bit

Table 3–1 shows as an example the range of the 8–bit coefficients, resulting from the conditions mentioned above. From the view of the CCU programmer this might be the most interesting case. Three formats are used to express the coefficient values: Integer decimal, integer hexadecimal and normalized.

Coefficient values must be transferred from the CCU to the AMU via the IM bus in binary format; therefore in most tables of this data sheet the values will be presented in HEX and additionally in the normalized format, to make the digital signal processing background more understandable. To save space the normalized values will be rounded.

3.2. DC Offset Suppression (only for PDM–Data)

To avoid audible distortions caused by volume changes the DC part of the signals coming from the decimation filters has to be minimized. Therefore DC suppression for both channels is performed by the following steps:

1. calculation of the DC levels in two separate measure paths, i.e. down–sampling of both channels to about 1 kHz
2. lowpass filtering
3. subtracting the resulting DC signals from the original channels (= DC compensation)

Note: The feature DC offset suppression is not controllable by the CCU, e.d. all coefficients are fixed and stored in the AMU's C–ROM.

3.3. 50 µs Digital Deemphasis (for PDM–Data Only).

A digital deemphasis is applied to the PDM inputs in order to process preemphasized audio signals (e.g. FM TV). So it is not necessary to realize the 50 µs deemphasis by analog networks at the AMU's outputs as shown in Fig. 2–3 (or at the APU's output with complete systems, as shown in Fig. 1–2). In the case of processing SCART signals or if an analog deemphasis at the DAC outputs is preferred, the digital deemphasis can be switched off (linear frequency response). Fig. 3–1 shows the 50 µs deemphasis frequency response. The control procedure is:

50 µs deemphasis on:

Φ Main Clock	18.432 MHz	17.732 MHz
KRDEEM (k26)	69 (0.5390)	73 (0.5703)

50 µs deemphasis off:

Φ Main Clock	18.432 MHz	17.732 MHz
KRDEEM (k26)	0 (0.0)	0 (0.0)

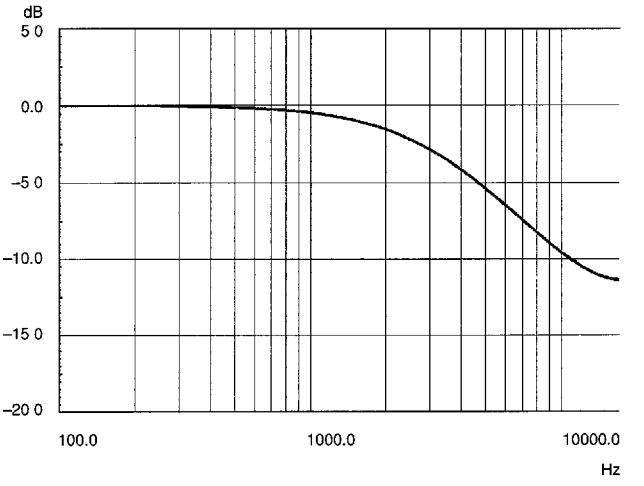


Fig. 3–1: 50 µs digital deemphasis frequency response

Table 3–1: Range of an 8–bit coefficient value

Coefficient	AMU Internal Presentation	HEX	DEC	Normalized
Max. Value	0111 1111	7F	127	0.9921875
Min. Positive Number	0000 0001	01	001	0.0078125
Max. Negative Number	1111 1111	FF	255	–0.0078125
Min. Number	1000 0000	80	128	–1.0

Note: Coefficients kij have to be determined such that any overflow in the AMU arithmetic is excluded. Nevertheless, if overflow occurs, the ALU will deal it according to a saturation characteristic. Considering this restriction, for good S/N ratio the digital range must be optimally used.

3.4. J17 Digital Deemphasis (Only for S–Data)

A J17 digital deemphasis is included in all S bus channels. This is important in the case of D2–MAC mode. For test purposes or for future digital sources without J17 preemphasis this function can be switched off (linear frequency response). Fig. 3–2 shows the frequency response. The control procedure is:

J17 deemphasis on:

Φ Main Clock	18.432 MHz	17.732 MHz
KRJ17 (k28)	116 (0.90625)	117 (0.9140625)
KNJ17 (k29)	11 (0.0859375)	10 (0.078125)

J17 deemphasis off:

Φ Main Clock	18.432 MHz	17.732 MHz
KRJ17 (k28)	0 (0.0)	0 (0.0)
KNJ17 (k29)	118 (0.921875)	118 (0.921875)

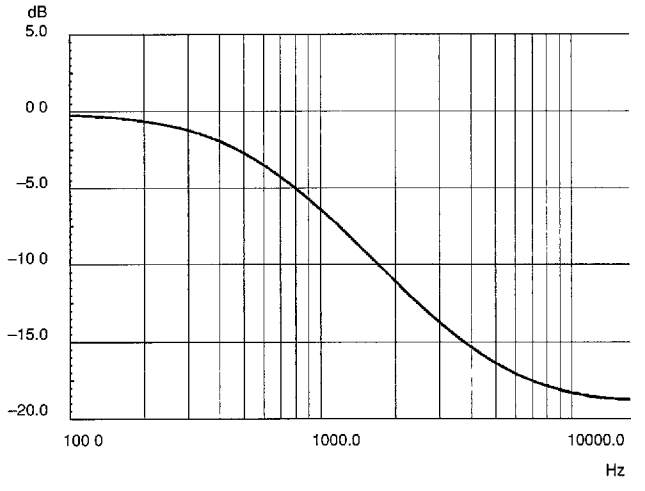


Fig. 3–2: J17 deemphasis frequency response

3.5. Medium Quality Oversampling Filter

Two oversampling filters in the S bus channels 3 and 4 allow to mix the D2–MAC medium–quality signals (16 kHz sampling rate) with the high–quality signals (32 kHz sampling rate). It is a third–order Cauer–type lowpass with a stopband attenuation of 40 dB. The frequency response is shown in Fig. 3–3. There are three selection modes regarding the oversampling filters:

both filters switched on:
KOVERS (k30) = 129 (–0.992 1875)

both filters switched off:
KOVERS (k30) = 127 (0.992 187 5)

one filter is switched on channel 3:
KOVERS (k30) = 0 (0.0)

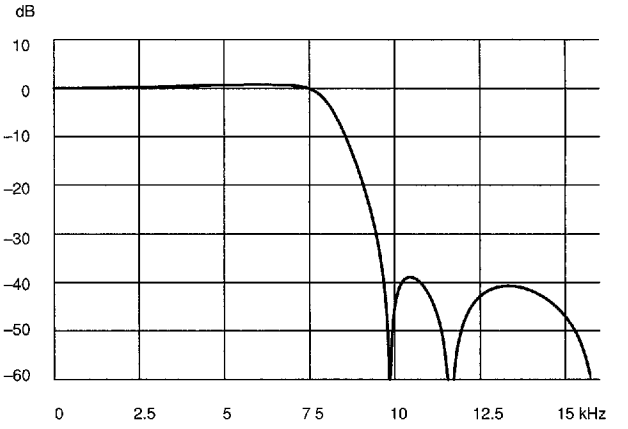


Fig. 3–3: Oversampling filter frequency response

3.6. Audio Mixing Section

This basic feature allows to route any input to every output and of course to mix different–weighted input channels. Due to the three shift–left (SHAL) at the matrix output a coefficient of 16 (= 0.125) corresponds to a 1:1 ratio of input to output. Table 3–2 shows the coefficients and their meaning.

Table 3–2: Output matrix coefficients

Output Channel	Coefficient	Connection to Source
Ch1:	KS1L1 (k02)	S bus channel 1
	KS2L1 (k03)	S bus channel 2
	KS3L1 (k04)	S bus channel 3
	KS4L1 (k05)	S bus channel 4
	KP1L1 (k06)	PDM 1
	KP2L1 (k07)	PDM 2
Ch2:	KS1R1 (k08)	S bus channel 1
	KS2R1 (k09)	S bus channel 2
	KS3R1 (k10)	S bus channel 3
	KS4R1 (k11)	S bus channel 4
	KP1R1 (k12)	PDM 1
	KP2R1 (k13)	PDM 2
Ch3:	KS1L2 (k14)	S bus channel 1
	KS2L2 (k15)	S bus channel 2
	KS3L2 (k16)	S bus channel 3
	KS4L2 (k17)	S bus channel 4
	KP1L2 (k18)	PDM 1
	KP2L2 (k19)	PDM 2
Ch4:	KS1R2 (k20)	S bus channel 1
	KS2R2 (k21)	S bus channel 2
	KS3R2 (k22)	S bus channel 3
	KS4R2 (k23)	S bus channel 4
	KP1R2 (k24)	PDM 1
	KP2R2 (k25)	PDM 2

3.7. Sin x/x Compensation

The sin x/x compensation results in an improved frequency response. It is a precompensation of the 4 dB loss at half the sampling rate, that happens due to the D/A conversion. Fig.3–4 shows the frequency response of the sin x/x compensation. This function is always active, and no controller activity is required.

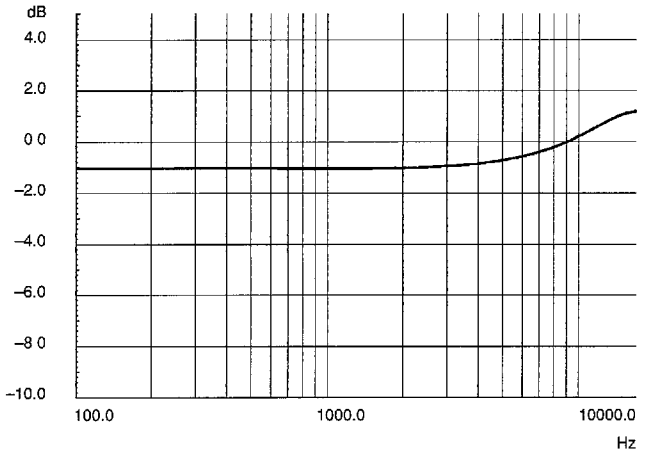


Fig. 3–4: Frequency response of the sin x/x compensation

3.8. Volume Control

The volume control facility works on the DAC 1 and DAC 2 analog outputs only.

The adjustment procedure for the output channels 1 and 2 (DAC 1) is performed by means of coefficient k0 and gives a dynamic range of 42 dB:

range: KVOL12 (k0) = 0 to 127 (0.0 to 0.992 187 5)

mute condition: KVOL12 (k0) = 0 (0.0)

In addition to this volume control, there is an additional analog volume adjustment (Vol 2) after the DAC 1 (see section 2.1.4.). The output channels 1 and 2 are controlled by a digitally–adjusted attenuator, which is controlled by k34 in steps of 1 dB each, and the total number of steps is 29.

range: k34 = 0 to 29 (0.0 to 0.265 625)
The adjustment procedure for the channels 3 and 4 (DAC 2) is performed by means of coefficient k1 and results in a dynamic range of 42 dB, too. There is no analog Vol 2 adjustment for the channels 3 and 4 (DAC 2) outputs.
range: KVOL34 (k1) = 0 to 127 (0.0 to 0.992 187 5)

mute condition: KVOL34 (k1) = 0 (0.0)

3.9. Matrix

The matrix defines the configuration between the four input channels and the D/A converter section. This means that channels 1 and 2 can be allocated to the DAC1 converters or to the DAC2 D/A converters and the same for channels 3 and 4. The matrix allows no mixing. The matrix feature is important to have a freely programmable selection of main speaker, headphones and SCART output. Control coefficient is k31:

KOUT (k31) = 127 (0.992 187 5) selects:

Matrix Input	to	Matrix Output
Channel 1		Channel 1
Channel 2		Channel 2
Channel 3		Channel 3
Channel 4		Channel 4

KOUT (k31) = 128 (–1.0) selects:

Matrix Input	to	Matrix Output
Channel 1		Channel 3
Channel 2		Channel 4
Channel 3		Channel 1
Channel 4		Channel 2

3.10. 50 µs Digital Preemphasis

The 50 µs digital preemphasis feature has been implemented to get compatibility to the former concept using the analog deemphasis network connected to the DAC outputs of the AMU or APU. In the case of D2–MAC operation mode, this analog deemphasis has to be precompensated. In the combined system shown in Fig. 1–2, the 50 µs deemphasis is now realized in the ACP 2371 by digital means, so that the preemphasis is not needed. For this case, it is possible to switch off the preemphasis by means of coefficient k27:

50 µs preemphasis on:

Φ Main Clock	18.432 MHz	17.732 MHz
KPRE (k27)	187 (–0.5390625)	183 (–0.5703125)

50 µs preemphasis off:

Φ Main Clock	18.432 MHz	17.732 MHz
KPRE (k27)	0 (0.0)	0 (0.0)

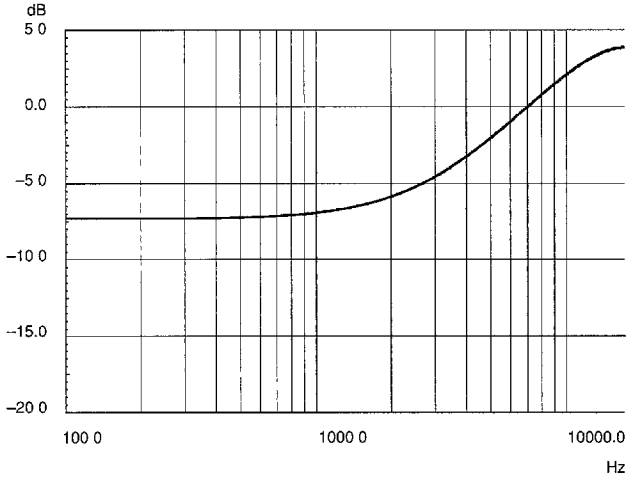


Fig. 3–5: 50 µs digital preemphasis frequency response

3.11. Oversampling Filter for Ch1 and Ch2

Two oversampling filters in channels 1 and 2 are implemented. The oversampling factor is two. Fig.3–6 shows the frequency response of the filters. Due to the fact that it is a software oversampling, the clock frequency must be fixed at 18.432 MHz.

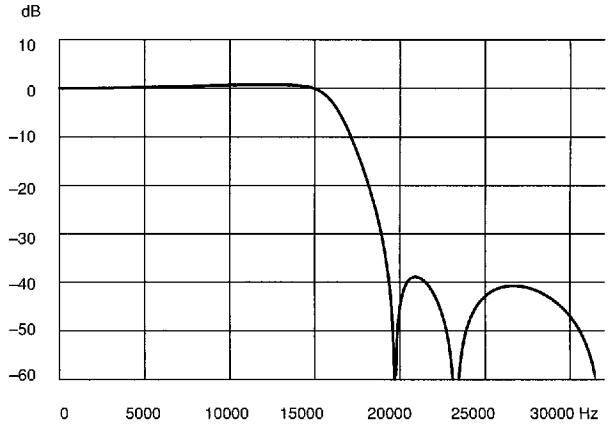


Fig. 3–6: Frequency response of the oversampling filter

3.12. AMU 2481 Initialization

- After switching–on the power or after reset, the AMU 2481 requires a certain startup time (Fig. 3–7) to accept coefficients and valid audio data.
- Immediately after a reset the volume (k0 and k1) is automatically set to zero.
- After a delay of another 0.5 s (or 0.6 s after power–on) a complete set of coefficients is transferred by the CCU via the IM bus, keeping volume (k0, k1) to zero.
- 20 ms later the mute function is switched off by the CCU.

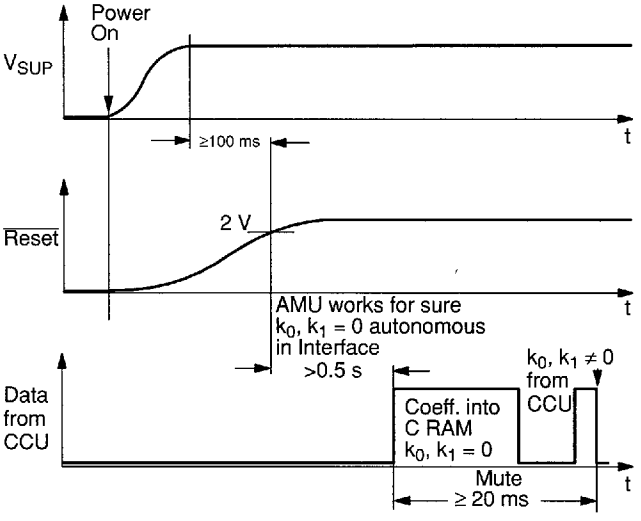


Fig. 3–7: Initialization of the AMU 2481

3.13. Complete Coefficient Table

Table 3–3 details all coefficients and control words which can be influenced by the CCU. Notes see page following Table 3–3.

Table 3–3: Available addresses in the AMU's C–RAM and their applications

Address	Coefficient		Description
64	KVOL12	k00	digital volume DAC1
65	KVOL34	k01	digital volume DAC2
66	KS1L1	k02	channel 1 source switch
67	KS2L1	k03	channel 1 source switch
68	KS3L1	k04	channel 1 source switch
69	KS4L1	k05	channel 1 source switch
70	KP1L1	k06	channel 1 source switch
71	KP2L1	k07	channel 1 source switch
72	KS1R1	k08	channel 2 source switch
73	KS2R1	k09	channel 2 source switch
74	KS3R1	k10	channel 2 source switch
75	KS4R1	k11	channel 2 source switch
76	KP1R1	k12	channel 2 source switch
77	KP2R1	k13	channel 2 source switch
78	KS1L2	k14	channel 3 source switch
79	KS2L2	k15	channel 3 source switch
80	KS3L2	k16	channel 3 source switch
81	KS4L2	k17	channel 3 source switch
82	KP1L2	k18	channel 3 source switch
83	KP2L2	k19	channel 3 source switch
84	KS1R2	k20	channel 4 source switch
85	KS2R2	k21	channel 4 source switch
86	KS3R2	k22	channel 4 source switch
87	KS4R2	k23	channel 4 source switch
88	KP1R2	k24	channel 4 source switch
89	KP2R2	k25	channel 4 source switch
90	KRDEEM	k26	deemphasis for PDM input
91	KPRE	k27	preemphasis for S bus output
92	KRJ17	k28	deemphasis for S bus input
93	KNJ17	k29	deemphasis for S bus input
94	KOVERS	k30	oversampling switch
95	KOUT	k31	output changing switch
96		k32	ADC coefficient (see ADC data sheet)
97		k33	control word for standard selection
98		k34	VOL2; analog volume control
102	Select Reg.		processor selection

Notes to Table 3–3:

Cascading of two or more AMUs for future applications need additional control information concerning the S bus. This is done by means of k33 and to ensure upward compatibility all bits are defined as follows:

k33: Bit 7 = 0* clock divider = 4 (section 2.3.)
= 1 clock divider = 3 (section 2.3.)

Bit 6 = 0* sampling rate is derived from system clock (section 2.3.)
= 1 sampling clock according to digital source (section 2.3.)

Bit 5 = 0* normal mode
= 1 test mode

concerning the S bus the AMU 2481 is:

Bit 4 = 0* slave
= 1 master

Bit 3 = 0 S bus data output active (section 2.3.)
= 1* S bus data output = high impedance (section 2.3.)

Bit 2 = 0* Pal mode
= 1 D2MAC/NICAM mode

Bit 1 = 0* normal S bus operation
= 1 S bus access to conversion filter for MSP FM mode

Bit 0 = 0 not used, for compatibility must be set to 0.

*) reset status

4. Specifications

4.1. Outline Dimensions

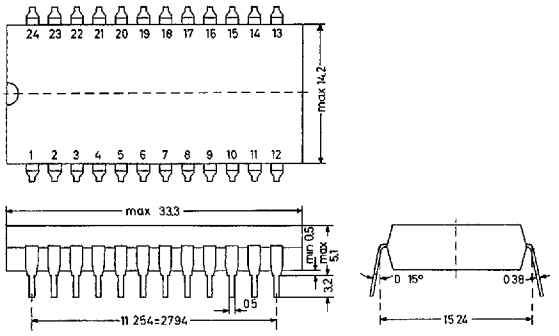


Fig. 4–1: AMU 2481 in 24–pin Dil Plastic Package, 20 B 24 according to DIN 41 870

Weight approx. 4.5 g Dimensions in mm

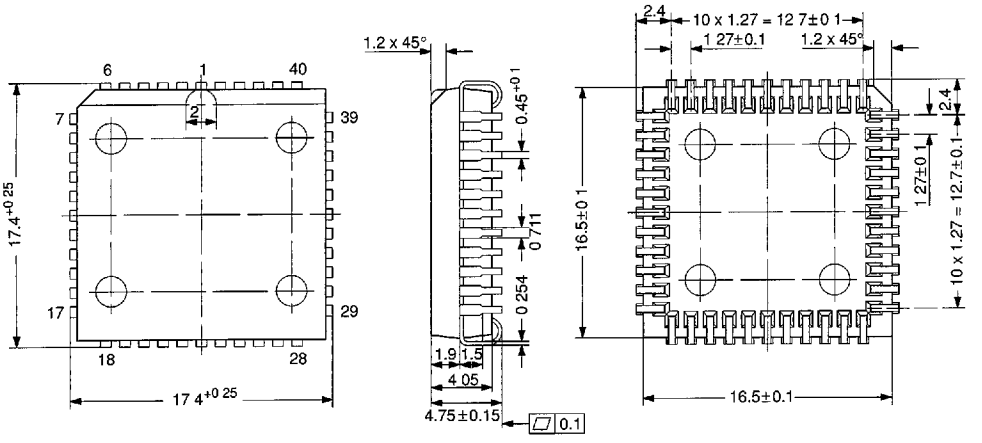


Fig. 4–2: AMU 2481 in 44–pin PLCC Package, Weight approx. 2.2 g Dimensions in mm

4.2. Pin Connections

4.2.1. 24–Pin DIL Package

1	I_{REF2} Reference Current Input (for DAC 2)
2	Leave Vacant
3	IM Bus Data Input/Output
4	IM Bus Ident Input
5	IM Bus Clock Input
6	S–Data Output
7	Leave Vacant
8	S–Clock Input/Output
9	S–Data Input
10	V_{ISB} Internal Substrate Bias Voltage
11	$\overline{\text{Reset}}$ Input
12	Ground (Digital)
13	ΦM Clock Input
14	V_{SUP}
15	S–Ident Input/Output
16	PDM2 Digital Input (R)
17	PDM1 Digital Input (L)
18	Leave Vacant

19 DAC2 Output Ch3

20 DAC 2 Output Ch 4

21 I_{REF1} Reference Current Input (for DAC1)

22 DAC1 Output Ch1

23 DAC1 Output Ch2

24 Ground (Analog)

4.2.2. 44–Pin PLCC Package

1 ΦM Main Clock Input

2 Leave Vacant

3 Leave Vacant

4 Leave Vacant

5 Leave Vacant

6 Leave Vacant

7 S–Ident Input/Output

8 S–Ident Output 2**

9 PDM2 Digital Input (R)

10 Leave Vacant

11 PDM1 Digital Input (L)

12 Vacant*

13 DAC2 Output Ch3

14 Vacant*

15 DAC2 Output Ch4

16 Vacant*

17 I_{REF1} Reference Current Input (for DAC1)

18 DAC1 Output Ch1

19 Vacant*

20 DAC1 Output Ch2

21 Leave Vacant

22 Ground (Analog)

23 V_{ISB} Internal Substrate Bias Voltage

24 I_{REF2} Reference Current Input (for DAC2)

25 Leave Vacant

26 Leave Vacant

27 IM Bus Data Input/Output

28 Leave Vacant

29 IM Bus Ident Input

30 Leave Vacant

31 IM Bus Clock Input

32 Leave Vacant

33 S–Data Output

34 Leave Vacant

35 V_{SUP}

36 Ground Supply

37 S–Clock Input/Output

38 Leave Vacant

39 S–Data Input

40 Leave Vacant

41 Leave Vacant

42 $\overline{\text{Reset}}$ Input

43 S–Clock Output 2**

44 ΦM Main Clock Output**

* = In order to minimize crosstalk, these pins should be appropriately grounded.

** = additional outputs compared to 24–pin Dil package pins 8, 43 see section 2.1.2.2.; pin 44 see section 2.3.

4.3. Pin Descriptions (pin numbers for 24–pin DIL package)

Pins 1 and 21 – Reference Current Inputs (Fig. 4–3)
These inputs require a current of 150 µA called reference current I_{REF} and serving for volume adjustment in the DAC interfaces.

Pin 12 – Digital Ground, 0
This pin must be connected to the negative of the supply. It must be used for ground connections in conjunction with digital signals.

Pin 3 – IM Bus Input/Output (Fig. 4–8)
Via this pin, the AMU 2481 is connected to the IM bus and communicates with the CCU.

Pins 4 and 5 – IM Bus Inputs (Fig. 4–4)
Via these pins, the AMU 2481 is connected to the IM bus and receives instructions from the CCU.

Pins 6, 8, 9 and 15 – Serial Audio Interface (S Bus)
Pin 9 is the S– Data input (Fig. 4–7) and pin 6 the S– Data output (Fig. 4–9). Pins 8 and 15 are S–Clock and S–Ident inputs/outputs (Fig. 4–10), the status depending on bit 4 in coefficient k33 (see sections 2.1.2.2. and 3.13.).

Pin 14 – V_{SUP} Supply Voltage
This pin must be connected to the positive of the supply.

Pin 10 – V_{ISB} Internal Substrate Bias Voltage
The AMU 2481 has an on–chip substrate bias generator which produces a negative bias voltage of about 3.4 V. Pin 10 should have a 0.1 µF capacitor to ground.

Pin 11 – $\overline{\text{Reset}}$ Input (Fig. 4–4)
In the steady state, high level is required at pin 11. A low level normalizes the AMU 2481. Initialization is described in section 3.12.

Pin 13 – ΦM Main Clock Input (Fig. 4–5)
This pin receives the required main clock signal from the MCU 2600 or MCU 2632 Clock Generator IC or from the DMA 2271 D2–MAC Decoder or the MSP 2410 Multistandard Sound Processor.

Pins 16 and 17 – $\overline{\text{PDM2}}$ and $\overline{\text{PDM1}}$ Digital Input (Fig. 4–6)
These pins receive the pulse–density modulated output signals of the ADC 2311 E.

Pins 19 and 20 – DAC2 Outputs Ch3 and Ch4 (Fig. 4–9)
These pins supply the audio output signals as output currents whose amplitude is determined by the reference current I_{REF2} fed to pin 1. The output signal of pins 19 and 20 is only influenced by the VOL1 volume control.

Pins 22 and 23 – DAC 1 Outputs Ch1 and Ch2 (Fig. 4–9)
These pins supply the audio output signals as output currents whose amplitude is determined by the reference current I_{REF1} fed to pin 21. The output signal of pins 22 and 23 is influenced by the VOL 1 and VOL 2 volume control facilities.

Pin 24 – Analog Ground 0
This pin must be connected to the negative of the supply. It serves as ground connection for analog signals.

4.4. Pin Circuits (pin numbers for 24–pin DIL package)

The following figures schematically show the circuitry at the various pins. The integrated protection structures are not shown. The letter " E" means enhancement, the letter "D" depletion.

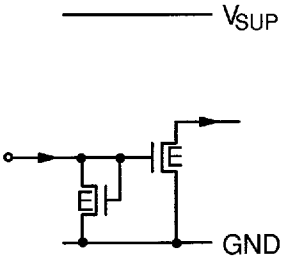


Fig. 4–3:
Input Pins 1, 21

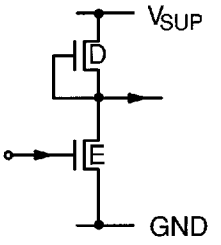


Fig. 4–4:
Input Pins 4, 5, 11

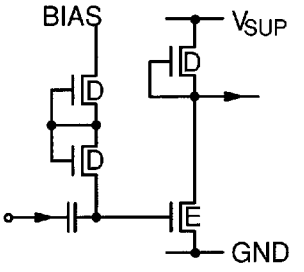


Fig. 4–5:
Input Pin 13

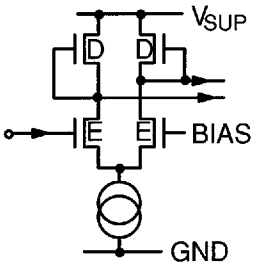


Fig. 4–6:
Input Pins 16, 17

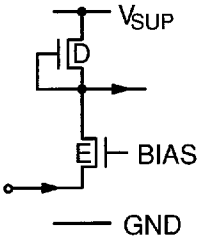


Fig. 4–7:
Input Pin 9

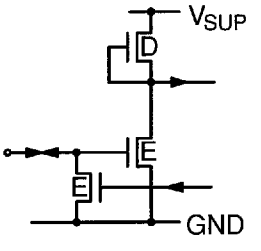


Fig. 4–8:
Input/Output Pin 3

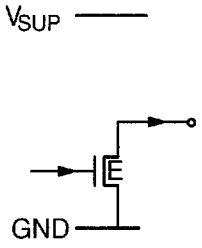


Fig. 4–9:
Output Pin 6,19, 20, 22

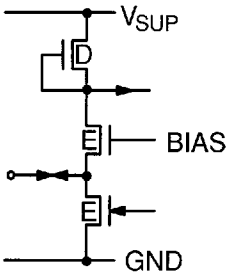


Fig. 4–10:
Input/Output Pins 8, 15

4.5. Electrical Characteristics (pin numbers for 24–pin DIL package)

All voltages are referred to ground.

4.5.1. Absolute Maximum Ratings

Symbol	Parameter	Pin No.	Min.	Max.	Unit
T_A	Ambient Operating Temperature	–	0	65	°C
T_S	Storage Temperature	–	–40	+125	°C
V_{SUP}	Supply Voltage	14	–	6	V
V_I	Input Voltage, all Inputs	–	–0.3 V	V_{SUP}	–
V_{DO}	DAC Output Voltage	19, 20, 22, 23	–0.3	+12	V
V_{SO}	S–Bus Output Voltage	6, 8, 15	–0.3 V	V_{SUP}	–
I_{DSO}	DAC and S–Bus Output Current	6, 8, 15, 19, 20, 22, 23	–	10	mA

4.5.2. Recommended Operating Conditions at T_A = 0 to 65 °C, $f_{\Phi M}$ = 14.3 to 18.4 MHz

Symbol	Parameter	Pin No.	Min.	Typ.	Max.	Unit
V_{SUP}	Supply Voltage	14	4.75	5.0	5.25	V
$V_{\Phi MIDC}$	ΦM Clock Input D.C. Voltage	13	1.5	–	3.5	V
$V_{\Phi MIAC}$	ΦM Clock Input A.C. Voltage (p–p)		0.8	–	2.5	V
$\frac{t_{\Phi MIH}}{t_{\Phi MIL}}$	ΦM Clock Input High/Low Ratio		0.9	1.0	1.1	–
$t_{\Phi MIHL}$	ΦM Clock Input High to Low Transition Time		–	–	$\frac{0.15}{f_{\Phi M}}$	–
V_{REIL}	Reset Input Low Voltage	11	–	–	1.2	V
V_{REIH}	Reset Input High Voltage		2.4	–	–	V
I_{REF}	Reference Input Current	1, 21	–	0.15	–	mA
V_{IMIL}	IM Bus Input Low Voltage	3 to 5	–	–	0.8	V
V_{IMIH}	IM Bus Input High Voltage		2.4	–	–	V
$f_{\Phi I}$	ΦI IM Bus Clock Frequency		0.05	–	170	kHz

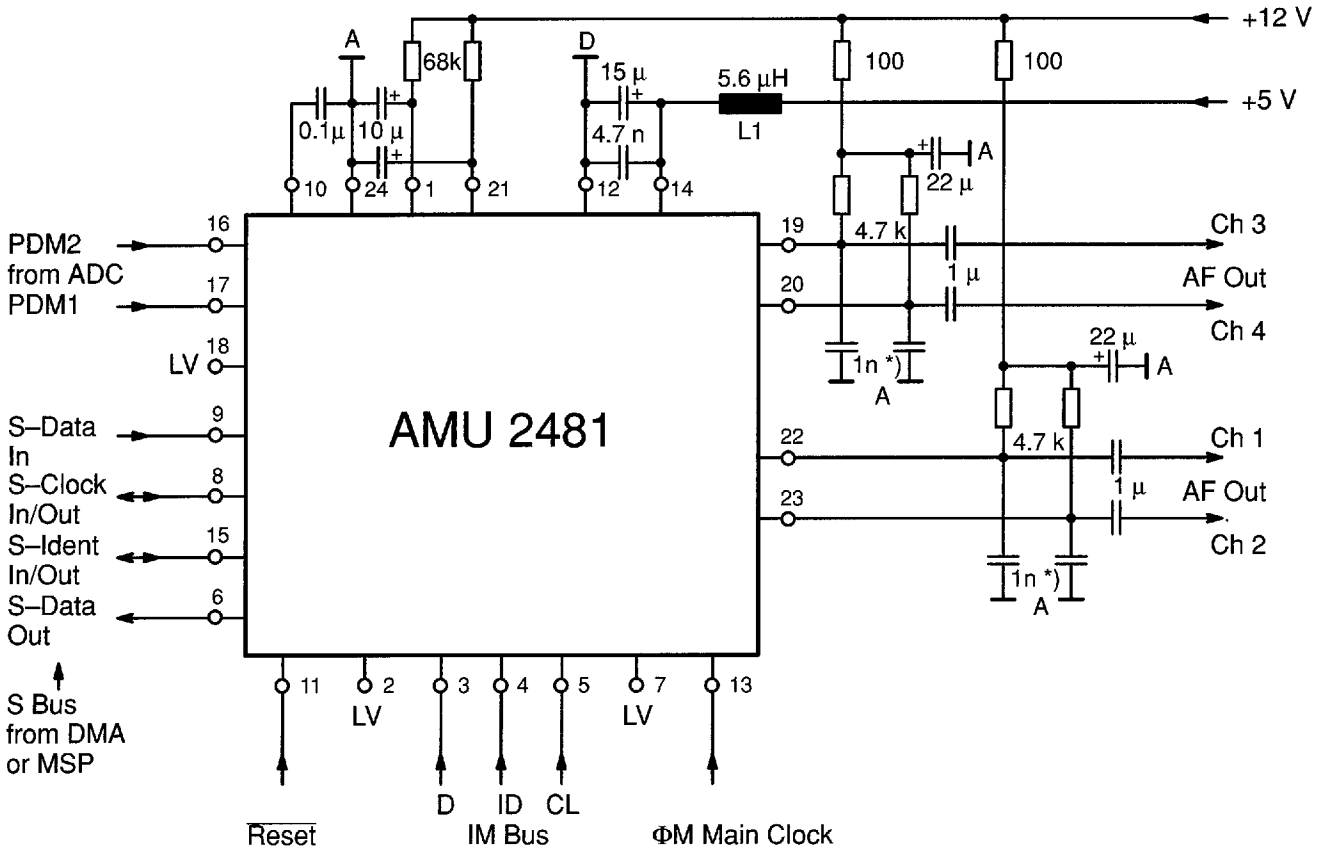
Recommended Operating Conditions, continued

Symbol	Parameter	Pin No.	Min.	Typ.	Max.	Unit
t_{IM1}	ΦI Clock Input Delay Time after IM Bus Ident Input	3 to 5	0	–	–	–
t_{IM2}	ΦI Clock Input Low Pulse Time		3.0	–	–	µs
t_{IM3}	ΦI Clock Input High Pulse Time		3.0	–	–	µs
t_{IM4}	ΦI Clock Input Setup Time before Ident Input High		0	–	–	–
t_{IM5}	ΦI Clock Input Hold Time after Ident Input High		1.5	–	–	µs
t_{IM6}	ΦI Clock Input Setup Time before Ident End–Pulse Input		6.0	–	–	µs
t_{IM7}	IM Bus Data Input Delay Time after ΦI Clock Input		0	–	–	–
t_{IM8}	IM Bus Data Input Setup Time before ΦI Clock Input		0	–	–	–
t_{IM9}	IM Bus Data Input Hold Time after ΦI Clock Input		0	–	–	–
t_{IM10}	IM Bus Ident End–Pulse Low Time		3.0	–	–	µs
V_{SIL}	S Bus Input Low Voltage	8, 9, 15	–	–	0.4	V
$-I_{SIH}$	S Bus Input High Current		–	–	20	µA
f_{IS}	ΦS Clock Input Frequency	8	–	$\frac{f_{\Phi M}}{4}$	–	–
$\frac{t_{S2}}{t_{S1}}$	ΦS Clock Input High/Low Ratio		0.8	1	1.2	–
t_{S3}	ΦS Clock Input Setup Time before Ident End–Pulse Input	8, 15	150	–	–	ns
t_{S4}	S Bus Data Input Setup Time before ΦS Clock Input	8, 9	50	–	–	ns
t_{S5}	S Bus Data Input Hold Time after ΦS Clock Input		50	–	–	ns
t_{S6}	S Bus Ident End–Pulse Input Low Time	15	150	–	–	ns
V_{DIL}	Digital Input Low Voltage	16, 17	–	–	$0.5 \cdot V_{SUP} - 0.3\ V$	–
V_{DIH}	Digital Input High Voltage		$0.5 \cdot V_{SUP} + 0.3\ V$	–	–	–
C_{ISB}	Internal Substrate Bias Voltage Filter Capacitor	10	–	100	–	nF

4.5.3. Characteristics at T_A = 0 to 65 °C, V_{SUP} = 4.75 to 5.25 V, $f_{\Phi M}$ = 14.3 to 18.4 MHz

Symbol	Parameter	Pin No.	Min.	Typ.	Max.	Unit	Test Conditions
I_{SUP}	Supply Current	14	–	140	170	mA	
V_{IMOL}	IM Bus Output Low Voltage	3	–	–	0.4	V	I_{IMO} = 3 mA
I_{IMOH}	IM Bus Output High Current		–	–	10	µA	V_{IMO} = 5 V
$-I_{SIL}$	S–Clock/Ident/Data Input Low Current	8, 9, 15	–	1	2.7	mA	V_{SI} = 0.3 V
V_{SIH}	S–Clock/Ident/Data Input High Voltage		–	–	1.2	V	I_{SI} = 0
V_{SOL}	S–Bus Output Low Voltage	8, 9, 15	–	–	0.3	V	I_{SO} = 6 mA
I_{SOH}	S–Data Output High Current	6	–	–	10	µA	V_{SO} = 5 V
I_{OMAIN}	DAC1 Output Peak–to–Peak Current	22, 23	–	0.81	–	mA	I_{REF1} =0.15 mA, VOL2 = 0 dB
			–	25	–	µA	I_{REF1} =0.15 mA, VOL2 = –30 dB
I_{OAUX}	DAC2 Output Peak–to–Peak Current	19, 20	–	0.81	–	mA	I_{REF2} =0.15 mA
THD	Total Hamonic Distortion of DAC Output	19, 20, 22, 23	–	–	0.1	%	
V_{ISB}	Internal Substrate Bias Voltage	10	–	–3.4	–	V	C_{ISB} = 100 nF
V_{REF1}	Reference Input Voltage Drop	21	–	2.5	–	V	R_{REF1} = 68 kOhm from +12 V, VOL2 = 0 dB
			–	0.45	–	V	R_{REF1} = 68 kOhm from +12 V, VOL2 = –30 dB
V_{REF2}	Reference Input Voltage Drop	1	–	2.5	–	V	R_{REF2} = 68 kOhm from +12 V

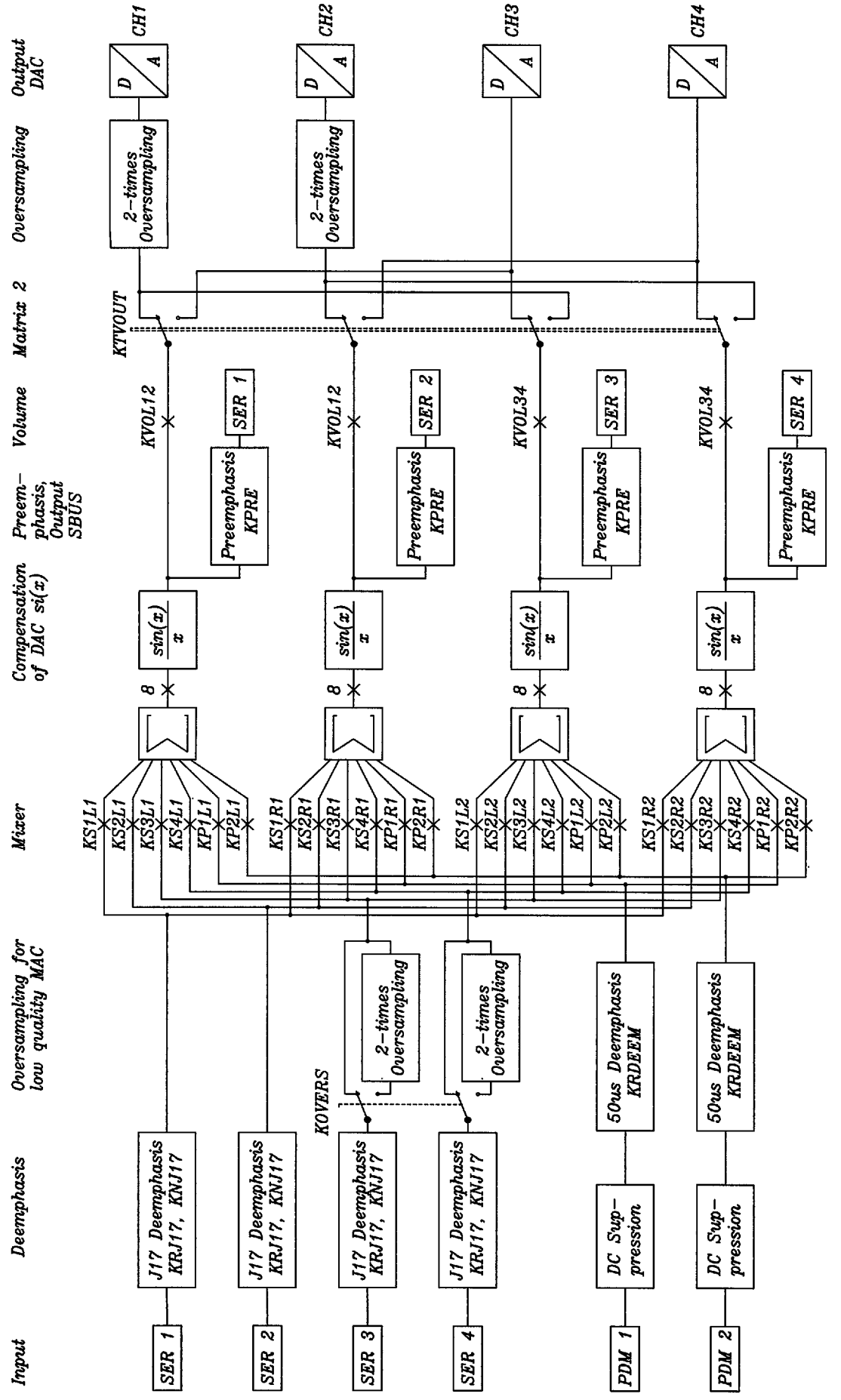
5. Appendix 1: Application Circuit (pin numbers for 24–pin Dil package)



*optionally 10 nF for 50 µs analog deemphasis

Fig. 5–1: Application circuit

6. Appendix 2: Program Structure



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