

# AN7291SC, AN7291FBP

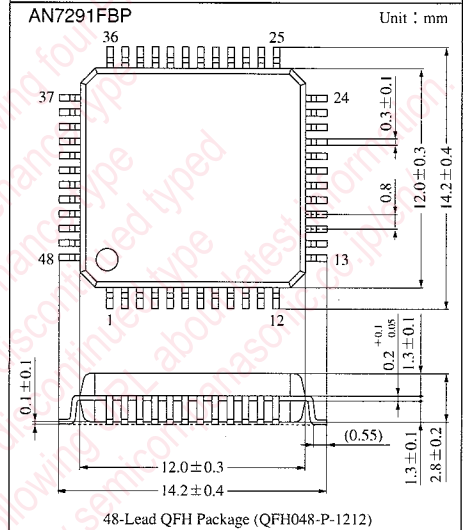
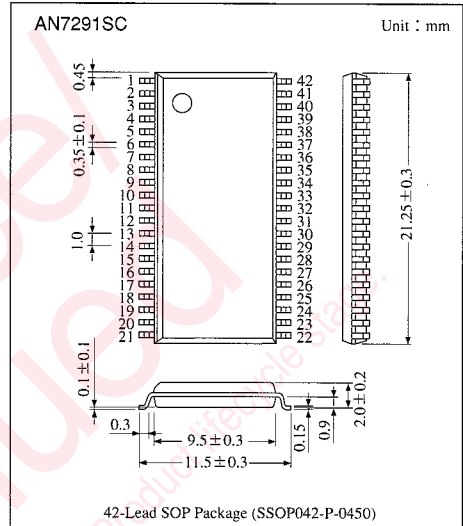
FM—IF, Detection, Noise Canceller, MPX Demodulation IC

### Overview

The AN7291SC, AN7291FBP are IC integrated FM—IF/Det., PNL, MPX into a single chip. PNL, MPX is basically the same configuration as previous AN7465S, but VCO is adjustment-free by using ceramic lock.

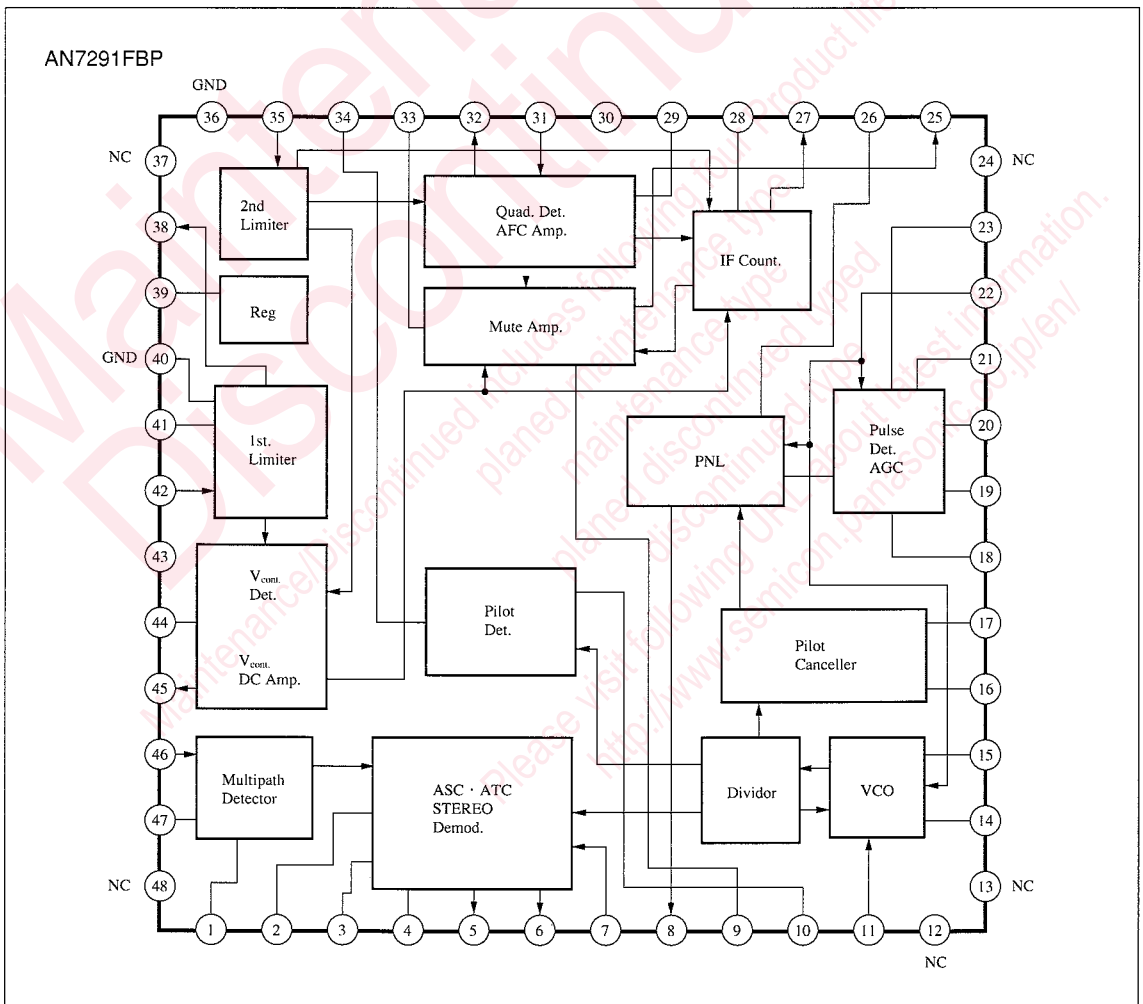
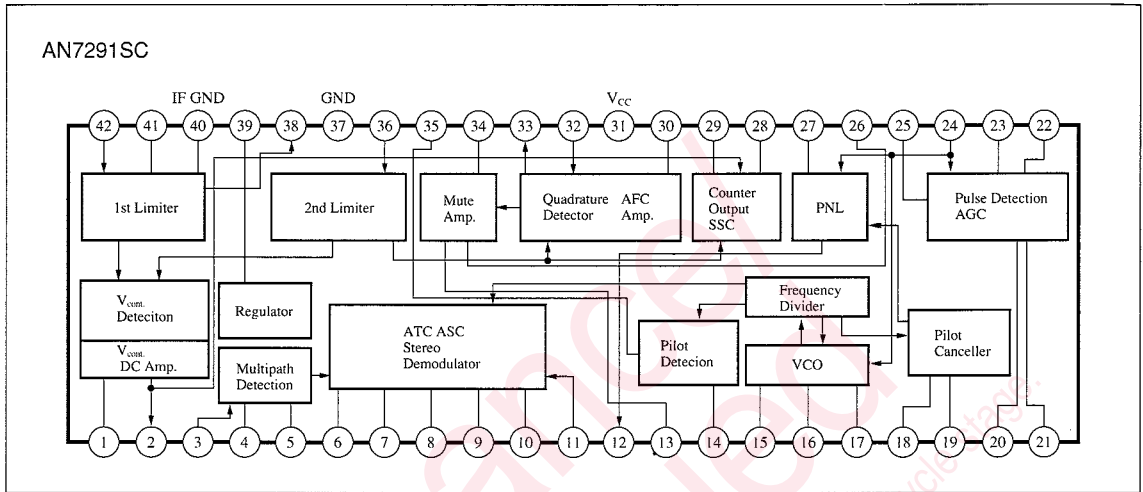
### Features

- Integration previous 2-chip (IF/Det., PNL/MPX) into a single chip
- High IF sensitivity
- With IF counter output, SEEK sensitivity adjustment
- Adjustment-free VCO (ceramic lock 912kHz)
- Fewer external parts (Fewer large capacitance capacitor)
- Good control voltage linearity, wide adjusting range
- Multipath detection amp. built-in



ICs for Tuner

■ Block Diagram



### ■ Absolute Maximum Ratings (Ta=25°C)

Parameter	Symbol	Rating	Unit
Supply Voltage	V <sub>CC</sub>	9.6	V
Supply Current	I <sub>CC</sub>	43	mA
Power Dissipation (Ta=75°C)	P <sub>D</sub>	787 <sup>Note1)</sup> /670 <sup>Note2)</sup>	mW
Operating Ambient Temperature	T <sub>opr</sub>	-30 ~ +80	°C
Storage Temperature	T <sub>stg</sub>	-55 ~ +125	°C

Note 1) AN7291SC Note 2) AN7291FBP

### ■ Recommended Operating Range (Ta=25°C)

Parameter	Symbol	Range
Operating Supply Voltage Range	V <sub>CC</sub>	7.2V ~ 9.6V

\* The AN7291SC pin numbers are used below. For the AN7291FBP, refer to Pin No. Correspondence Table.

### ■ Electrical Characteristics (V<sub>CC</sub>=8V, f<sub>in</sub>=10.7MHz, f<sub>Mod.</sub>=1kHz 30%FM, Ta=25°C)

Parameter	Symbol	Condition	min.	typ.	max.	Unit
Control Voltage (1)	V <sub>C1</sub>	No input Pin②DC voltage	0.1	0.5	0.9	V
Control Voltage (2)	V <sub>C2</sub>	V <sub>in</sub> =40dBμ, Pin②DC voltage	1.25	1.55	1.85	V
Control Voltage (3)	V <sub>C3</sub>	V <sub>in</sub> =70dBμ, Pin②DC voltage	2.8	3.3	3.8	V
Control Voltage (4)	V <sub>C4</sub>	V <sub>in</sub> =100dBμ, Pin②DC voltage	4.5	5.15	5.7	V
Control Voltage (5)	V <sub>C5</sub>	V <sub>C5</sub> =V <sub>C3</sub> -V <sub>C2</sub>	1.5	1.7	1.9	V
Control Voltage (6)	V <sub>C6</sub>	V <sub>C6</sub> =V <sub>C4</sub> -V <sub>C3</sub>	1.6	1.8	2	V
AFC Offset Voltage	V <sub>AFC</sub>	No signal input DC voltage between Pin⑩ and ⑪	-0.2	0	0.2	V
Output Level L	V <sub>OL</sub>	V <sub>in</sub> =70dBμ, Pin⑩AC voltage	125	145	165	mVrms
Output Level R	V <sub>OR</sub>	V <sub>in</sub> =70dBμ, Pin⑨AC voltage	125	145	165	mVrms
Channel Balance	CB	CB=20log (V <sub>OL</sub> /V <sub>OR</sub> )	-1	0	1	dB
Limiting Sensitivity	V <sub>lim</sub>	V <sub>OL</sub> =0dB, Input Pin⑩AC voltage decreases by 3dB	21	24	27	dBμV
Residual Pilot Voltage	V <sub>PC</sub>	V <sub>in</sub> =70dBμ pilot signal 10% modulation Pin⑫AC voltage	—	7	14	mVrms
Stereo Lamp ON Level	Lamp <sub>(ON)</sub>	Modulation only by pilot signal. Pin⑬ DC voltage = less than 2V	2.6	4.7	6.3	%
Stereo Lamp OFF Level	Lamp <sub>(OFF)</sub>	Modulation only by pilot signal. Stereo lamp ON/OFF level ratio	2	4.5	7	dB
Separation Lch	Sep. L	V <sub>in</sub> =70dBμ, L+R=90% Pilot 10%	22	35	—	dB
Separation Rch	Sep. R	V <sub>in</sub> =70dBμ, L+R=90% Pilot 10%	22	35	—	dB
Capture Range	CR	V <sub>in</sub> =70dBμ, pilot signal 8% modulation	+0.6 -0.45	±1	—	%
Counter Output Level (1)	V <sub>IF1</sub>	V <sub>in</sub> =70dBμ, Pin⑭=0V, Pin⑮10.7MHz output voltage	0	1	10	mVrms
Counter Output Level (2)	V <sub>IF2</sub>	V <sub>in</sub> =70dBμ, Pin⑭=V <sub>CC</sub> , Pin⑮AC output voltage	80	100	120	mVrms
Supply Current	I <sub>tot</sub>	No input, Pin⑰=0V	28	35	40	mA
Monaural THD (Lch)	THDL	Monaural input 400mV, 1kHz Lch distortion rate	—	0.15	0.3	%
Monaural THD (Rch)	THDR	Monaural input 400mV, 1kHz Rch distortion rate	—	0.15	0.3	%

ICs for  
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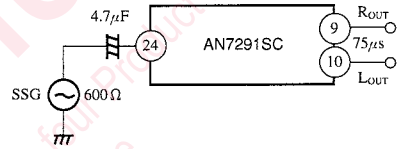
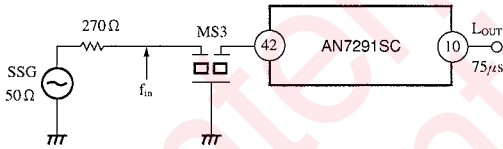
**Electrical Characteristics (Cont.)** ( $V_{CC}=8V$ ,  $f_{in}=10.7MHz$ ,  $f_{Mod.}=1kHz$  30% FM,  $T_a=25^{\circ}C$ )

Parameter	Symbol	Condition	min.	typ.	max.	Unit
Stereo THD (Lch)	THD SL	Stereo, L + R = 360mV, $V_p=40mV$ , Lch distortion rate	—	0.15	0.3	%
Stereo THD (Rch)	THD SR	Stereo, L + R = 360mV, $V_p=40mV$ , Rch distortion rate	—	0.15	0.3	%
AGC Voltage (1)	$V_{AGC1}$	Input = 0mVrms, $R_s=600\Omega$ , Pin② DC voltage	—	0	0.4	V
AGC Voltage (2)	$V_{AGC2}$	Input $V_{in2}=2mVrms$ , 150kHz, Pin② DC voltage	1.3	1.48	1.65	V
Noise Detection Voltage	$V_{Det.}$	$V_{in2}=100mVrms$ , 150kHz, Pin② DC voltage	—	0	0.3	V
Gate Pulse Width	PW	$V_{in2}=0.3V_{P-P}$ , $tw=1\mu s$ , $f=1kHz$ , Pin⑩ output	19	24	29	$\mu s$
Residual Noise Voltage	$V_{NR}$	$V_{in2}=1V_{P-P}$ , $tw=10\mu s$ , $f=1kHz$ , Input through LPF. Lch output	—	0	0.7	mVrms

**Characteristics Curve**

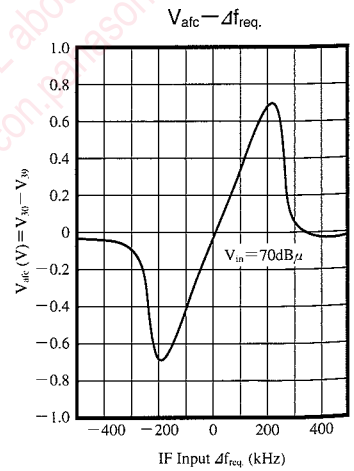
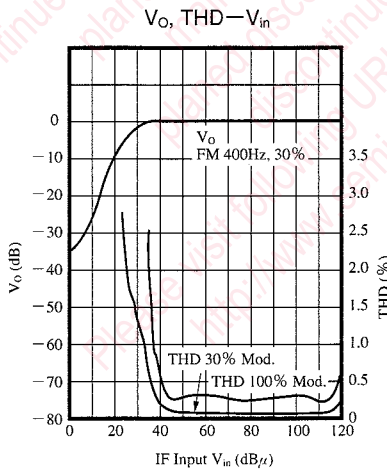
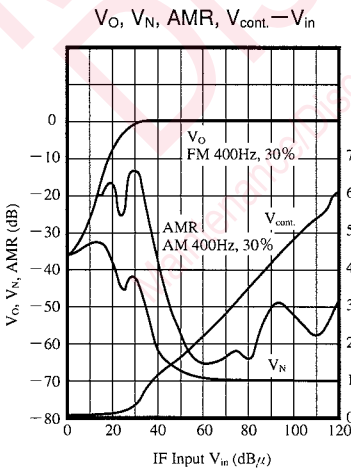
① Measuring Condition at IF Input

② Measuring Condition at NC Input

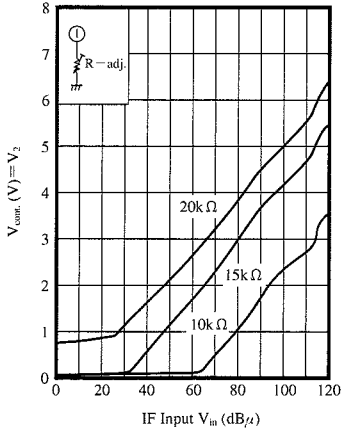


Unless otherwise specified,  $V_{CC}=8V$ ,  $f_{in}=10.7MHz$   
 FM Modulation 30%, 400Hz,  
 $V_{in}=70dB\mu$

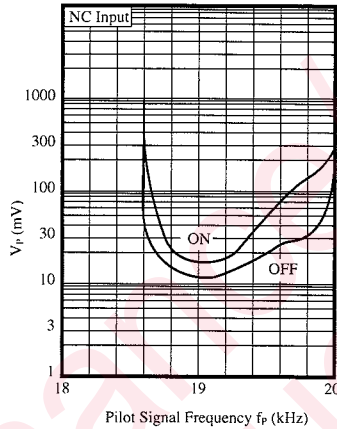
Unless otherwise specified,  $V_{CC}=8V$ ,  $f_{in}=1kHz$ ,  
 $V_{in}=400mV$  (Monaural)  
 L + R = 360mV (Stereo)  
 $V_p=40mV$  (Stereo)



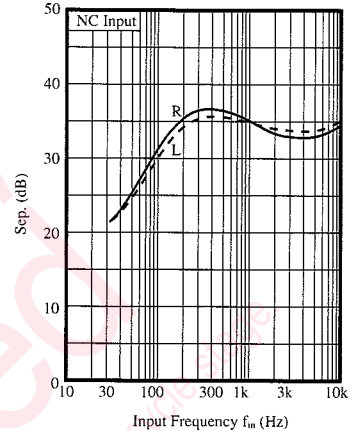
Control Voltage  
Control Example



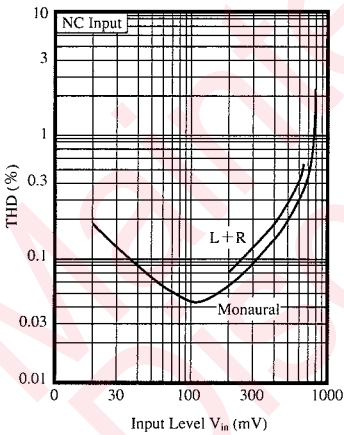
Lamp ON/OFF— $f_p$



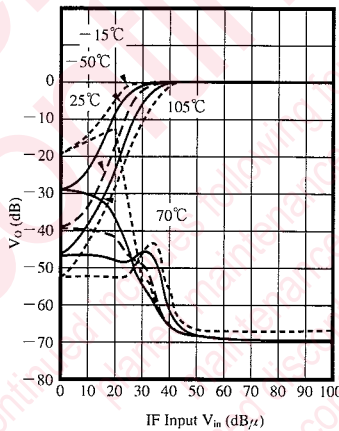
Sep.— $f_{in}$



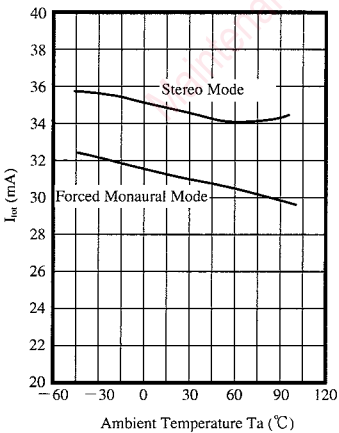
THD— $V_{in}$



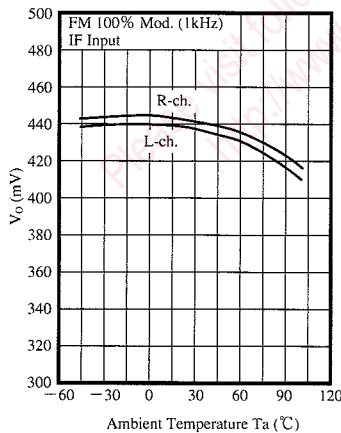
Input/Output Characteristics



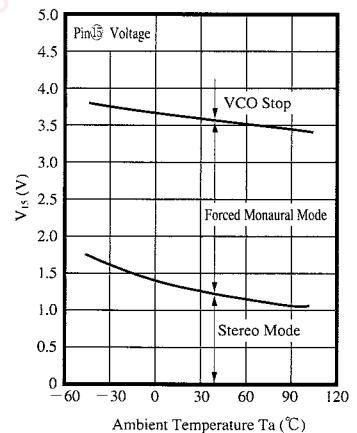
$I_{tot}$ — $T_a$

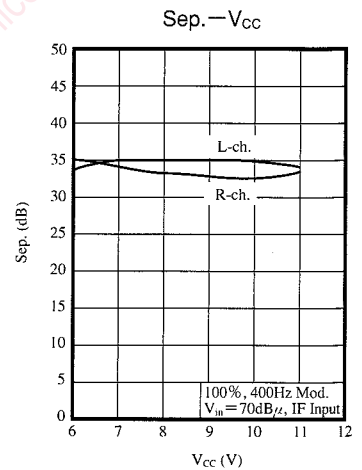
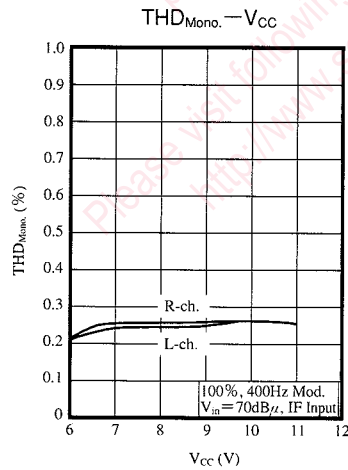
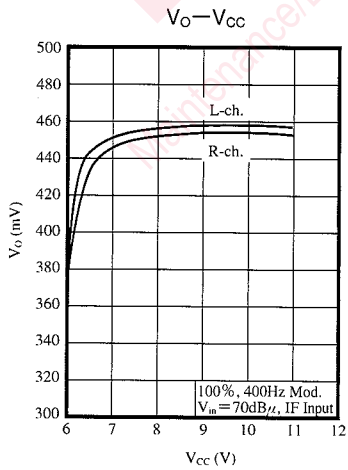
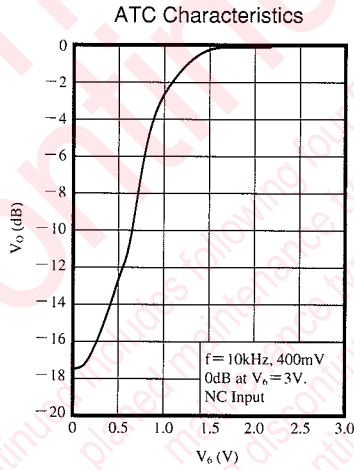
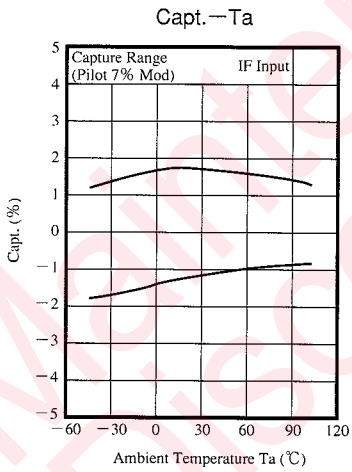
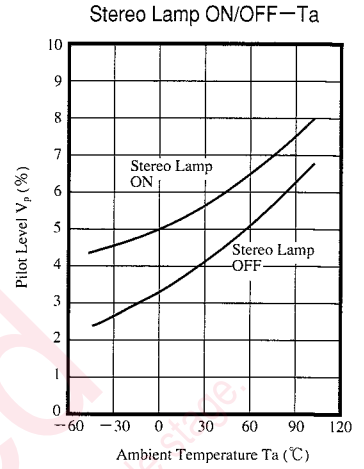
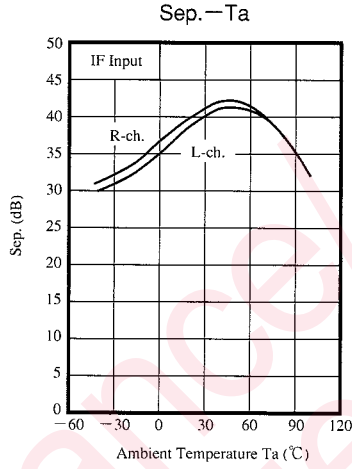
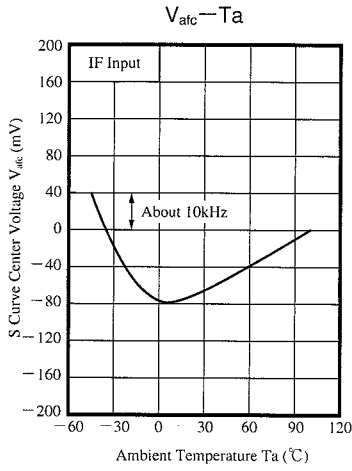


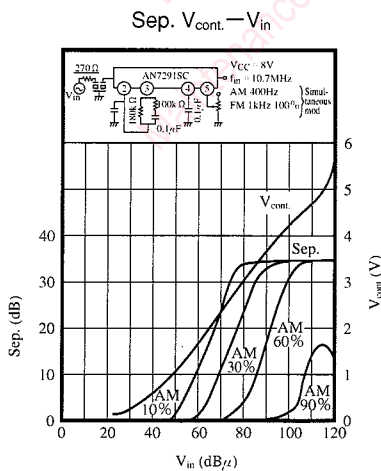
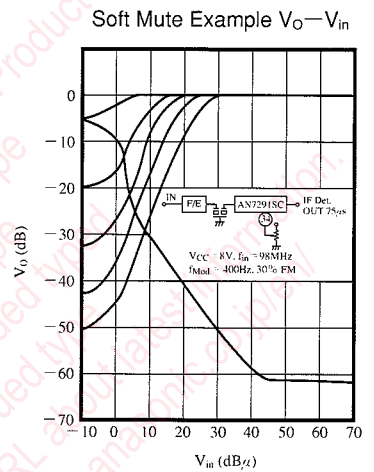
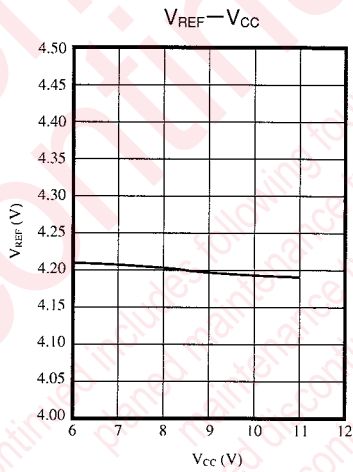
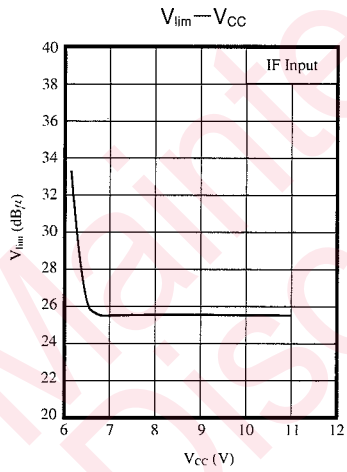
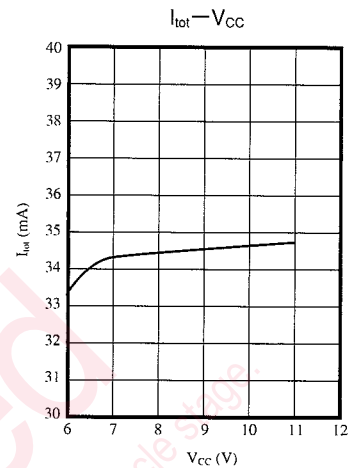
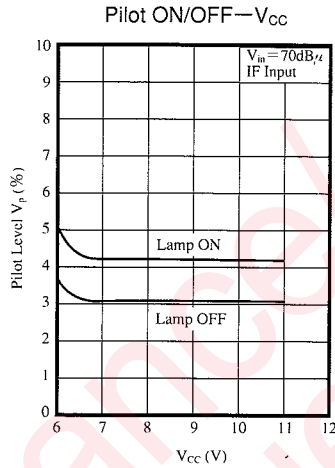
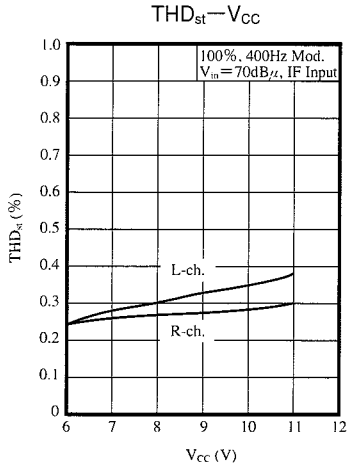
$V_o$ — $T_a$



Forced Monaural  
Operation Voltage— $T_a$

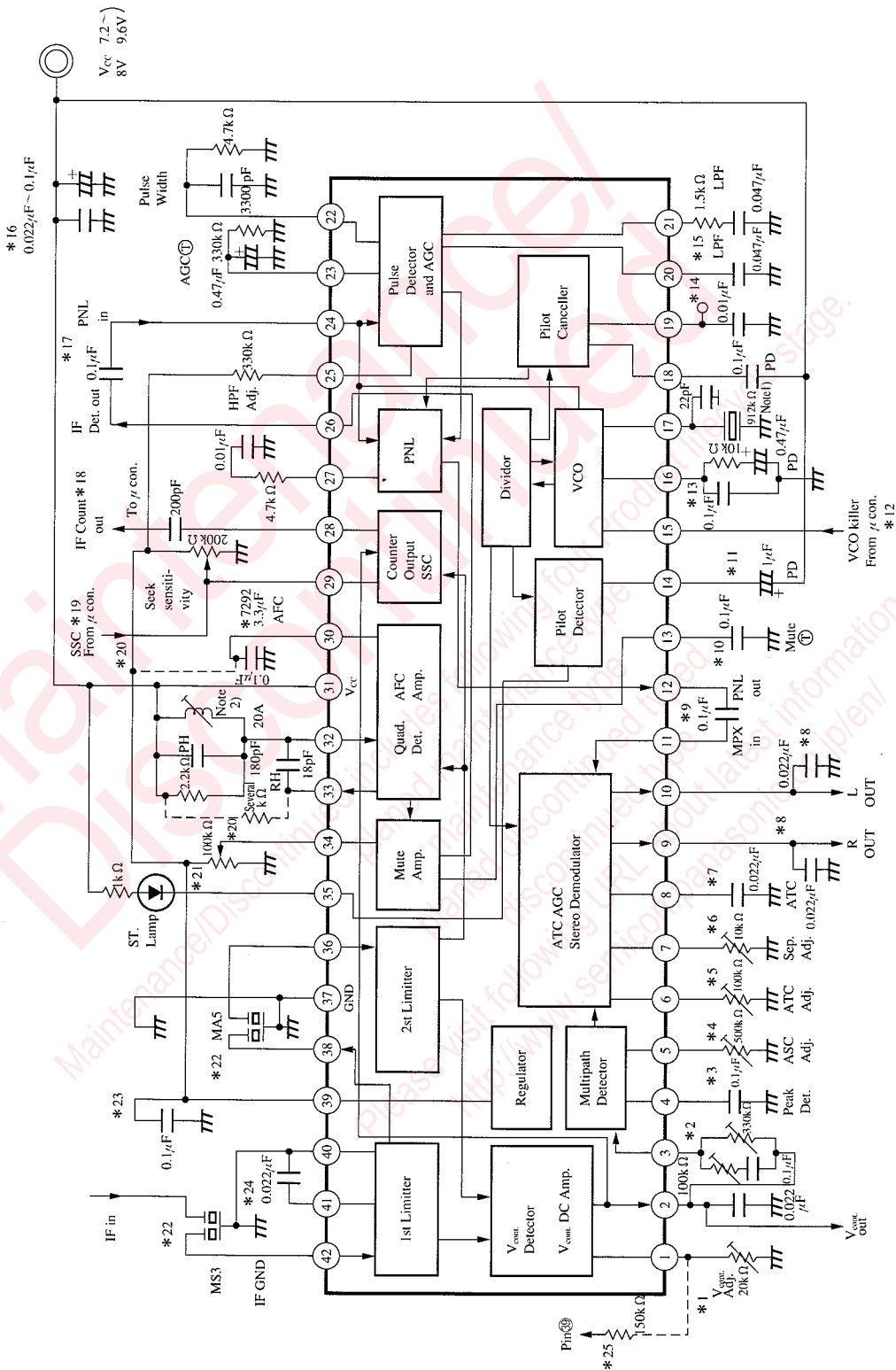






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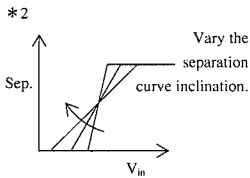
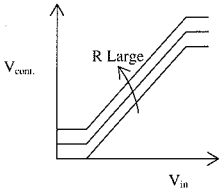
Application Circuit (Example of AN7291SC)



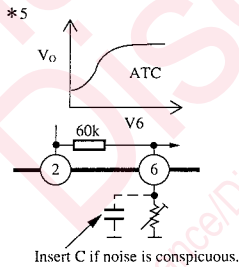
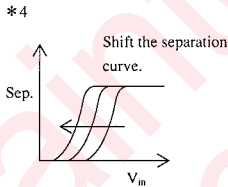
Note 1) Ceramic lock CSB912JF101 (by Murata Manufacturing Co., Ltd.), Note 2) IFT ZIF-5EB020A (by Matsushita)

■ Description on Pins Shown in Application Circuit Diagram

\*1 Control voltage adj.



\*3 At multipath detection  
Capacitor for  
Detection : up to 1μF



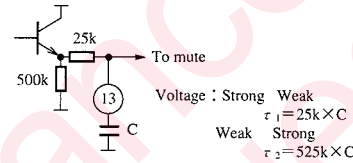
\*6 Adjust the separation max. value.

\*7 Capacitor of 0.01 to 0.022μF  
for determining ATCF time

\*8 0.022μ is C. for de-emphasis.  
Inside 3.3kΩ

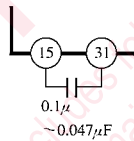
\*9 Pin⑬ input impedance is 400kΩ.  
At 0.1μF, high frequency band Sep.  
is lowered, but can be used.  
The larger the better. 0.1μ is min.

\*10 Vary the soft mute time constant.



\*11 Pilot Detection  
Phase Detection Filter  
Small...Lamp malfunction due to noise  
Large...Lamp ON speed high

\*12 VCO stop  $3.9 < V_{15} < V_{CC}$   
Forced monaural  $1.7 < V_{15} < 3.2$   
Stereo mode  $0 < V_{15} < 1.0$   
• When Pin⑬ is not used, preferably  
insert C between  $V_{CC}$ .



\*13 VOC For phase detection  
Lag lead filter

\*14 For pilot canceller Pseudo sine wave  
output : Capacitance =  $0.0068\mu \sim 0.015\mu$

\*15 PNL noise amp. Path control

\*16 (Put it at the possible nearest position to IC pin.)

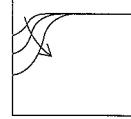
\*17 Pin⑳ input impedance is 500kΩ.  
0.1μF is min. value.  
The larger the better.

\*18 IF counter output Take care for routing.  
(Keep it away from input)

\*19 SSC  
 $V_{29} > 1V \dots$  Counter OUT  
 $V_{29} \approx 0V \dots$  IF counter OFF

\*20 THD improved

\*21 Soft mute adj.



\*22 For domestic use, vary the  
frequency band according  
to applications.

\*23 Regulator by-pass Take  
care for GND location.

\*24 1st limiter path control

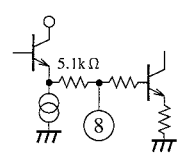
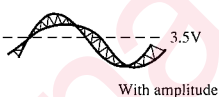
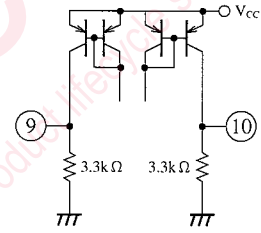
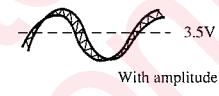
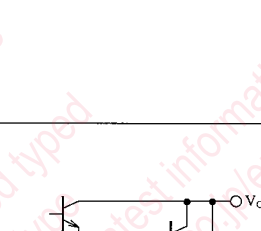
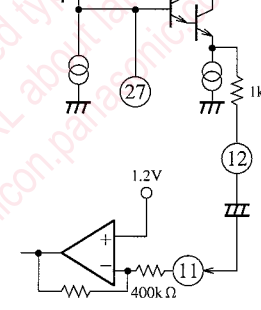
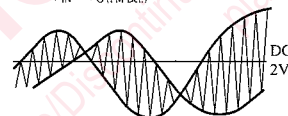
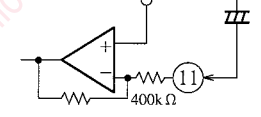
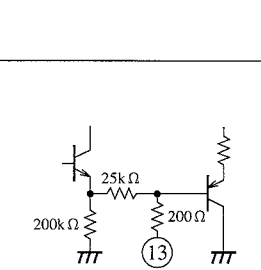
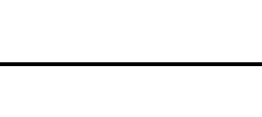
\*25 S-meter in hot condition improved



■ Pin Descriptions (Example of AN7291SC)

Pin No.	Pin Name	Pin Waveform, Voltage	I/O Impedance	Equivalent Circuit
1	V <sub>CONT.</sub> Adj.	DC ≈ 3.5V	Low	
2	V <sub>CONT.</sub> OUT (Level Meter)		200 Ω	
6	ATC Adj.	$V_{\text{⑥}} = \frac{R_{\text{⑥}}}{57\text{k}\Omega + R_{\text{⑥}}} V_{\text{②}}$	57k Ω	
3	AMDC IN	DC about 1.9V	Low	
4	AMDC Peak Det.		Rise Low Fall 330k Ω	
5	AMDC Adj.	DC about 2.3V	14.5k Ω	
Note) AMDC: Automatic Multi Path Distortion Canceller				
7	Separation Adj.	DC (max.) ≈ 1.2V AC = 0 ~ V <sub>Ⓡ</sub>	2k Ω	

Pin Descriptions (Example of AN7291SC) (Cont.)

Pin No.	Pin Name	Pin Waveform, Voltage	I/O Impedance	Equivalent Circuit
8	ATC L. P. F.	Same as $V_{\text{IF}}$ , level higher than external capacitor down.	5.1k $\Omega$	
9	L-ch. OUT	AC varies with input condition.  With amplitude	3.3k $\Omega$	
10	R-ch. OUT	AC varies with input condition.  With amplitude	3.3k $\Omega$	
11	MPX. IN	AC=Same as Pin 12. DC=1.3V	400k $\Omega$	
12	NC. OUT	$\approx V_{\text{IN}} \approx V_{\text{O (FM Det.)}}$  DC 2V	1k $\Omega$	
27	NC. Hold	$V_{\text{(AC)}} \approx V_{\text{IF}}$ $V_{\text{(DC)}} \approx 3.3\text{V}$	1.5k $\Omega$	
13	Soft Mute Time Const.	DC $\approx 0\text{V} \sim 4.1\text{V}$	25k $\Omega$	

ICs for Tuner

■ Pin Descriptions (Example of AN7291SC) (Cont.)

Pin No.	Pin Name	Pin Waveform, Voltage	I/O Impedance	Equivalent Circuit																				
14	Pilot Det. L. P. F	DC ≈ V <sub>CC</sub> - 1.4V	R = 36k Ω																					
18	Pi. Can. Control L. P. F	DC ≈ V <sub>CC</sub> - 1.4V	R = 68k Ω																					
15	ST/Mono. Control	<table border="1"> <thead> <tr> <th>Pin Voltage</th> <th>Demodulation</th> <th>LED</th> <th>Pilot Can.</th> <th>VCO</th> </tr> </thead> <tbody> <tr> <td>0V ~ 1V</td> <td>○</td> <td>○</td> <td>○</td> <td>○</td> </tr> <tr> <td>1.7V ~ 3.2V</td> <td>×</td> <td>×</td> <td>○</td> <td>○</td> </tr> <tr> <td>3.9V ~ V<sub>CC</sub></td> <td>×</td> <td>×</td> <td>×</td> <td>×</td> </tr> </tbody> </table>	Pin Voltage	Demodulation	LED	Pilot Can.	VCO	0V ~ 1V	○	○	○	○	1.7V ~ 3.2V	×	×	○	○	3.9V ~ V <sub>CC</sub>	×	×	×	×	High	
Pin Voltage	Demodulation	LED	Pilot Can.	VCO																				
0V ~ 1V	○	○	○	○																				
1.7V ~ 3.2V	×	×	○	○																				
3.9V ~ V <sub>CC</sub>	×	×	×	×																				
16	PLL L. P. F	DC ≈ 4.3V	R = 66k Ω																					
17	VCO (Ceramic Lock Pin)	 f = 912kHz AC ≈ 3V <sub>p-p</sub>	High																					
19	Pi. Can. Quasi-sin	 f = 19kHz AC ≈ 100mV <sub>p-p</sub>	—																					

■ Pin Descriptions (Example of AN7291SC) (Cont.)

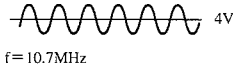
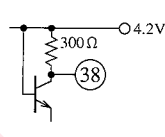
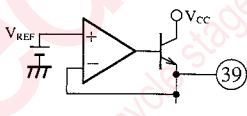
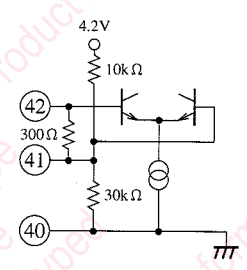
Pin No.	Pin Name	Pin Waveform, Voltage	I/O Impedance	Equivalent Circuit
20	AGC Amp. L. P. F	DC≈3.5V AC is noise	6.2kΩ	
21	Pulse Amp. L. P. F	DC≈4.2V AC is noise	2.7kΩ	
22	Gate Time Adj.		Usually High Low at Operation	
23	Noise Amp. AGC		Rise 15kΩ Fall High	
24	NC IN		500kΩ	
25	NC H. P. F	Level lower than Pin 24 waveform down. DC is determined by external voltage (4.2V).	High	
26	IF Det. OUT	 (Vary with input condition)	3.3kΩ	
28	IF Count Out	DC≈4V AC≈80mVrms (Normal AC is OFF)	1kΩ	

ICs for  
Tuner

■ Pin Descriptions (Example of AN7291SC) (Cont.)

Pin No.	Pin Name	Pin Waveform, Voltage	I/O Impedance	Equivalent Circuit
29	SCC { Seek Sence. Adj. }	Apply bias voltage from outside.	200kΩ	
30	AFC OUT		26kΩ	
31	V <sub>cc</sub>	8V	Low	
32	Quad. IN	DC=8V (Determined by outside.) <90° phase shift	High	
33	Limiter OUT		500Ω	
34	Soft Mute Adj.	Voltage input from outside 0V~V <sub>REF</sub> (4.2V)	High	
35	LED Driver	At stereo DC=0V~0.5V	Low	
		At monaural Determined by external voltage.	High	
36	2nd IF IN	≈0V	300Ω	

■ Pin Descriptions (Example of AN7291SC) (Cont.)

Pin No.	Pin Name	Pin Waveform, Voltage	I/O Impedance	Equivalent Circuit
37	System GND	0V	Low	—————
38	IF1 Limiter OUT	 4V f = 10.7MHz	300Ω	
39	V <sub>REF</sub>	4.2V constant voltage	Low	
40	IF GND	—————	Low	
41	IF Amp. Bypass	DC = 3.1V	7.5kΩ	
42	IF IN	DC = 3.1V AC = V <sub>in(IF)</sub>	300Ω	

ICs for Tuner

■ Supplementary Explanation

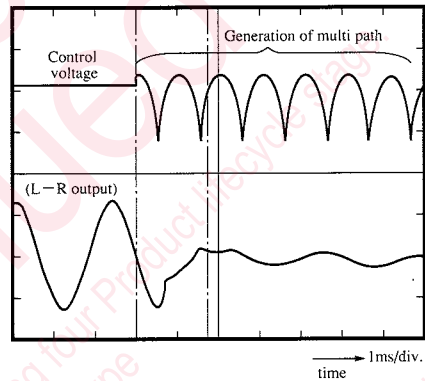
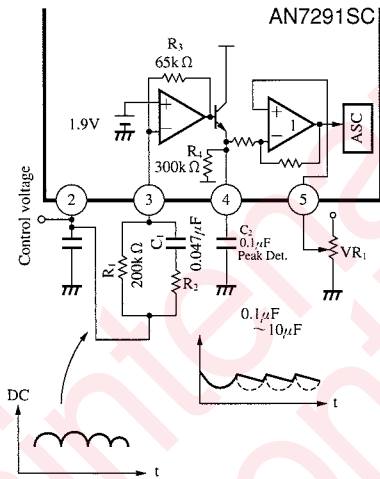
(1) On Multi path Distortion Preventive Circuit  
(AN7291SC pin numbers are used in the following explanation.)

1. Principle

Multi path distortion is apt to increase especially in the stereo receiving mode. In consideration of this phenomenon, the AN7291SC has been designed so as to suppress the feeling of physical disorder incidental to multi path noise by degrading the separation against multi path distortion.

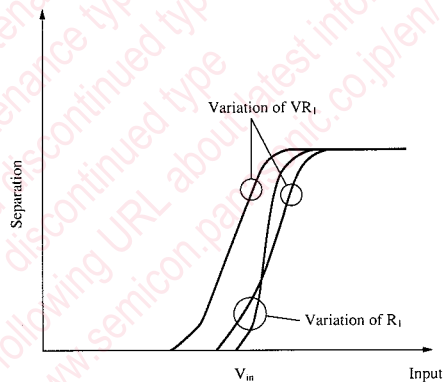
Detection method...Detection of AM components included in control voltage (level meter) output

Separation control...Operation of conventional ASC circuit by conversion of detected AM components into DC voltage



(1) Operation in a state free from multi path  
(Operation as ASC)

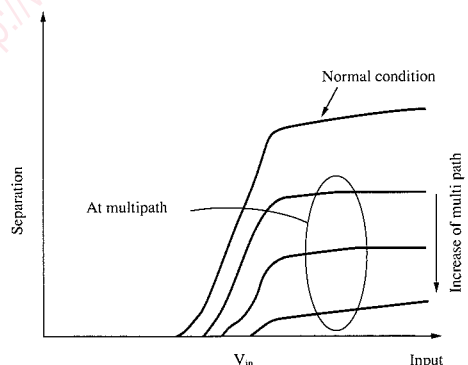
The control voltage of ② is sent to the ASC through the two operational amplifiers. The gradient of the characteristics curve can be set by  $R_3/R_1$ , and the start point can be set by  $VR_1$ .



(2) Operation in a state exposed to multi path

The variation to appear in the control voltage on account of multi path distortion is put to AM detection, and the DC voltage to the ASC is suitably lowered to degrade the separation.

The frequency characteristics of the AM components are adjusted through  $C_1$  shown in the sketch, and the AM components are put to peak value detection by  $R_4$  and  $C_2$ .



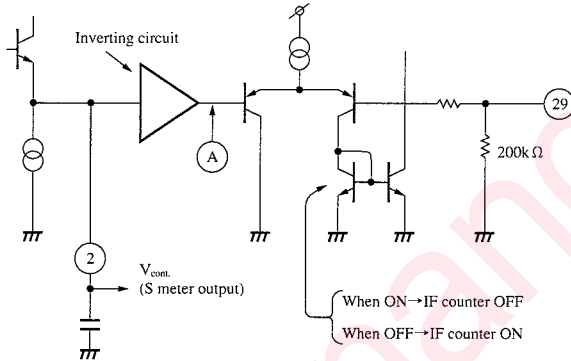
**(2) On SSC Pin (AN7291SC pin numbers are used in the following explanation.)**

1. What is SSC?

SSC is the acronym of Search Stop Clear, and it usually denotes the search stop clear control.

In AN7291SC, the IF count output is obtained on the SSC pin only in the search mode.

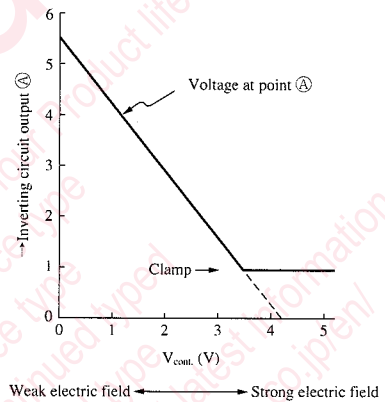
2. Internal Equivalent Circuit of SSC Pin<sup>Ⓐ</sup>



3. Operational Description

The inverting circuit has the gain of about 1.3 times, and its input-output characteristics changes as shown in the right sketch. (Calculated values)

This inverting circuit generates the IF count output only when the voltage at point <sup>Ⓐ</sup> is lower than the set voltage of Pin<sup>Ⓐ</sup>.



[3] Selection Standard of Noise Canceler Resistance Value  
(AN7291SC pin numbers are used in the following explanation.)

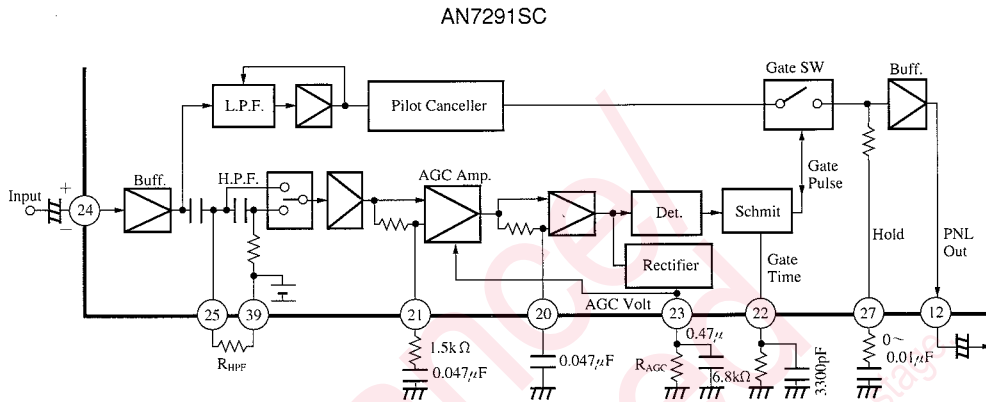


Fig.1 Pulse Noise Limiter (PNL) Block Diagram

(1) Relation to field strength

1. In weak electric field

In a weak electric field where noise is apt to increase, the AGC effectively controls the PNL operation.

- a) In case operation error is frequently caused by white noise, suitably increase the value of Pin 23  $R_{AGC}$  (220kΩ to 1MΩ).
- b) In case operation error is frequently caused by overmodulation, suitably increase the value of  $R_{HPF}$  between Pin 25 and Pin 39 (47kΩ to 470kΩ).

2. In medium to strong electric field

In a medium to strong electric field relatively free from noise generation, the AGC becomes less effective and noise is detected almost at the maximum sensitivity.

- a) In case the detection sensitivity is too high, suitably decrease the value of  $R_{HPF}$  between Pin 25 and Pin 39 (10kΩ to 47kΩ)

3. In every electric field

- a) In case the detection sensitivity is excellent but the PNL effect deteriorated due to holding level fluctuation by noise, suitably increase the resistance value of the resistor connected in series with the Pin 27 holding capacitor (10kΩ to 4.7kΩ).
- b) In case the noise of the gate pulse itself is conspicuous, suitably narrow the gate pulse width by decreasing the resistance value of the Pin 22 resistor (3kΩ to 6.8kΩ).

(2) Selection of AGC Resistor  $R_{AGC}$  Pin 23

Pin 23 is the AGC LPF, and enables AGC effective level adjustment. The equivalent circuit in the vicinity of this pin has been so constituted as shown in Fig.2, and the output impedance at the charging time is 15kΩ while the input impedance at the discharging time is about 1MΩ.

The standard value of  $R_{AGC}$  is 330kΩ, but in case operation error is frequently caused in a weak electric field by white noise, selectively increase the value of  $R_{AGC}$  to a suitable level between 200kΩ and 1MΩ. So long as the value of  $R_{AGC}$  was properly increased, the AGC voltage proportionally becomes higher to prolong the discharging time constant, and the rate of operation error sharply drops with decrease of the gain of the AGC Amp. (Though Pin 23, the noise components are put to peak (envelope) detection. Even if the value of  $R_{AGC}$  was increased, the charging time and voltage remain almost unchanged because  $Z_O = 15kΩ$ ).

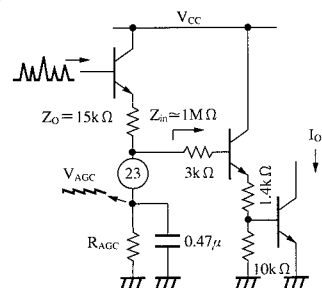
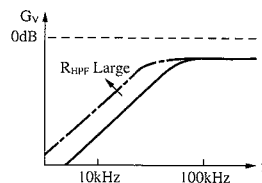


Fig.2

(3) Selection of HPF Resistor  $R_{HPF}$  Pin<sup>25</sup>

When the resistance value  $R_{HPF}$  of the resistor between Pin<sup>25</sup> and <sup>33</sup> was increased, the cut-off frequency of the HPF proportionally becomes lower.

The standard value of  $R_{HPF}$  is  $330k\Omega$ , but in case the operation error is frequently caused in a weak electric field by white noise at the modulation time or non-modulation time, selectively increase this  $R_{HPF}$  to a suitable value not exceeding  $470k\Omega$ .



[4] Cautions on Use of PLN (AN7291SC pin numbers are used in the following explanation.)

Care should be taken to use the PNL, because under the following conditions, in the PNL circuit of this IC, the output wave form may be distorted due to the oscillation of the PNL circuit.

1. Oscillation conditions

When the PNL is used under the conditions described in the following items (1) to (3) and the PNL – AGC voltage (Pin<sup>23</sup> voltage) becomes 2.3 V or more, oscillation may occur.

- (1) The PNL input frequency is 15 kHz or more and 500 mVrms is exceeded.
- (2) The voltage of AGC pin (Pin<sup>23</sup>) is forced to exceed the above voltage.
- (3) The voltage AC or DC of  $\pm$  several ten mV or more is directly applied to the PNL filter pins (Pin<sup>20</sup> and Pin<sup>21</sup>).

The oscillation occurrence depends on  $V_{CC}$ .

The oscillation can not be stopped unless  $V_{CC}$  is much increased, if it occurs.

The above three conditions are not given under the normal operation, and therefore oscillation problems are not suffered in practical use. In the review stage, keep in mind that oscillation may occur when the above conditions are given.

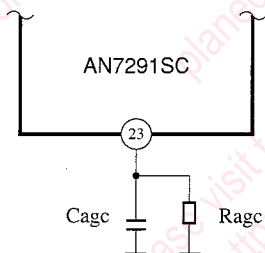
2. Effect by external components

The PNL circuit oscillation depends on an external resistor and capacitor of AGC pin.

- (1)  $C_{agc}$  is currently set to  $0.47\mu F$ . The larger it is, the less frequently oscillation occurs.
- (2)  $R_{agc}$  is  $330k\Omega$ . The smaller it is, the less frequently oscillation occurs.

When the above values are changed, take particular consideration for setting characteristics.

Also, when the use under the special conditions is expected, review the countermeasures against oscillation.



■ Pin No. Correspondence Table

AN7291SC	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21
AN7291FBP	44	45	46	47	1	2	3	4	5	6	7	8	9	10	11	14	15	16	17	18	19
AN7291SC	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42
AN7291FBP	20	21	22	23	25	26	27	28	29	30	31	32	33	34	35	36	38	39	40	41	42

\* Pins 12, 13, 24, 37, 43 and 48 for the AN7291FBP are NC.

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