

AN7292NSC, AN7292NFBP

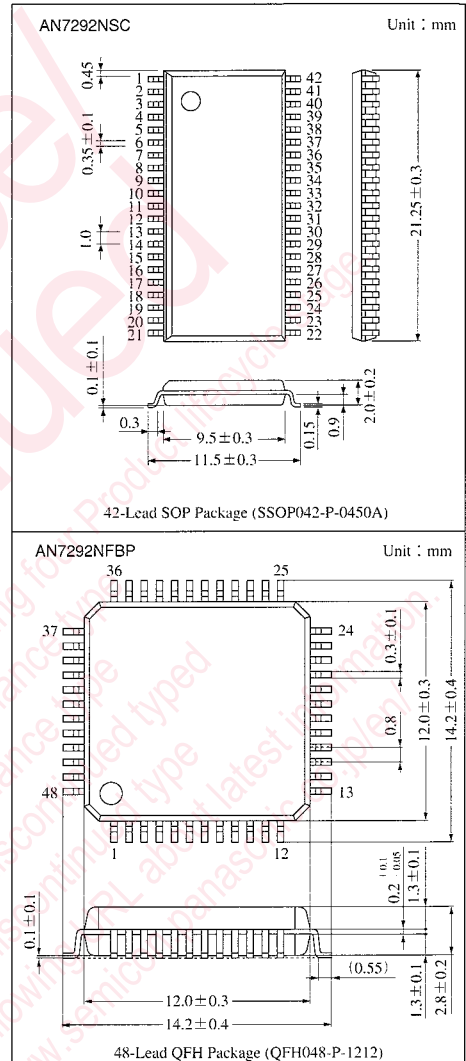
FM-IF, Detector, Noise Canceler, MPX Demodulator IC

Overview

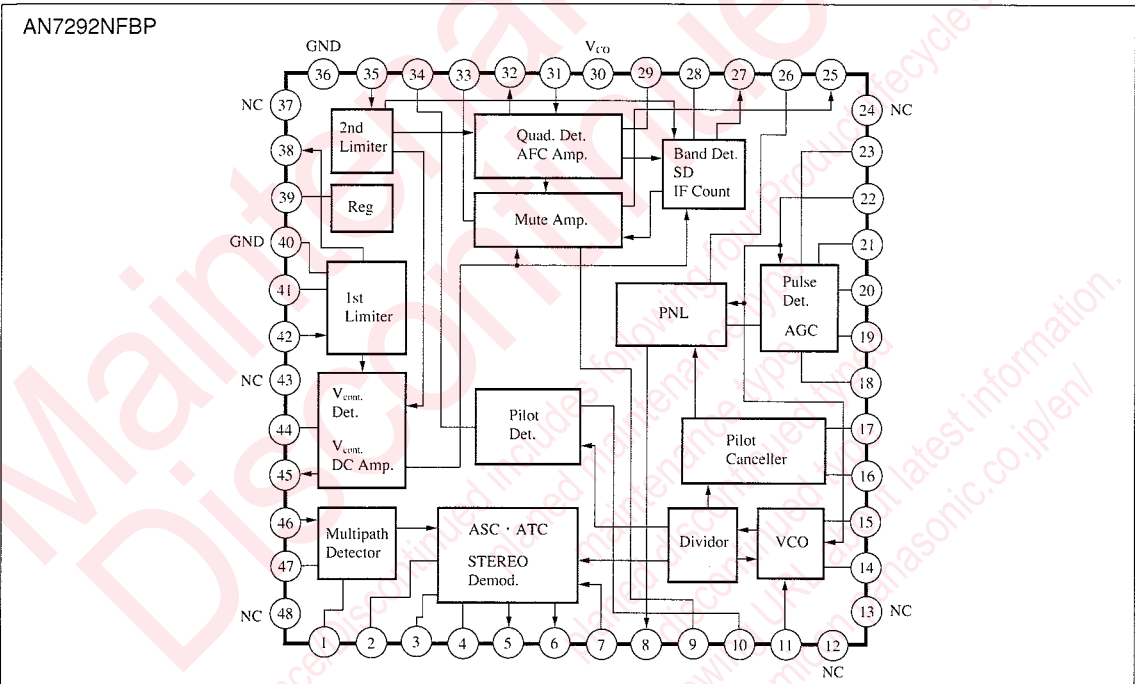
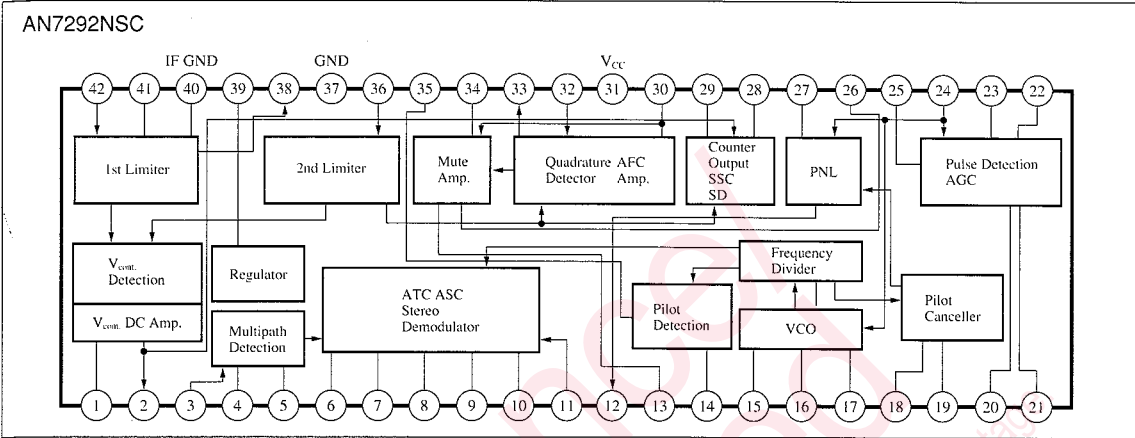
The AN7292NSC and AN7292NFBP are ICs, incorporating FM-IF/Det. for car radio, PNL, MPX section into a single chip. The SD and frequency band mute function are added to their basic-construction same as of the AN7291SC/FBP and they have also some improved temperature characteristics.

Features

- Functions conventionally separated in two chips (IF/Det., PNL/MPX) incorporated into a single chip
- High IF sensitivity
- With IF counter output, SD output, SEEK sensitivity adjuster
- Adjustment-free VCO (Ceramic lock 912kHz)
- Fewer external components required (fewer capacitors with large capacitance)
- Good linearity of control voltage and wide adjustable range
- Amp. for multipath detection built-in
- Frequency band mute function



Block Diagram



Pin No. Correspondence Table

AN7292NSC	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21
AN7292NFBP	44	45	46	47	1	2	3	4	5	6	7	8	9	10	11	14	15	16	17	18	19
AN7292NSC	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42
AN7292NFBP	20	21	22	23	25	26	27	28	29	30	31	32	33	34	35	36	38	39	40	41	42

* Pin 12,13,24,37,43 and 48 of the AN7292NFBP are NC.

Absolute Maximum Ratings (Ta = 25°C)

Parameter	Symbol	Rating	Unit
Supply Voltage	V _{CC}	9.6	V
Supply Current	I _{CC}	43	mA
Power Dissipation (Ta = 75°C)	P _D	787 ^{Note1)} / 670 ^{Note2)}	mW
Operating Ambient Temperature	T _{opr}	-30 ~ +80	°C
Storage Temperature	T _{stg}	-55 ~ +125	°C

Note1) AN7292NSC Note2) AN7292NFBP

■ Recommended Operating Range (Ta = 25°C)

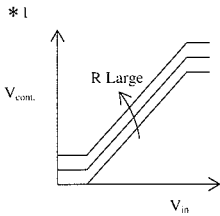
Parameter	Symbol	Range
Operating Supply Voltage Range	V _{CC}	7.2V ~ 9.6V

* Pin numbers used below are for the AN7292NSC. For the AN7292NFBP, refer to Pin No. Correspondence Table.

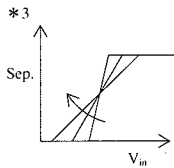
■ Electrical Characteristics (V_{CC} = 8V, f_{in} = 10.7MHz, f_{Mod.} = 1kHz 30%FM, Ta = 25°C)

Parameter	Symbol	Condition	min.	typ.	max.	Unit
Control Voltage (1)	V _{C1}	No input, Pin② DC voltage	0.1	0.5	0.9	V
Control Voltage (2)	V _{C2}	V _{in} = 40dBμ, Pin② DC voltage	1.05	1.50	1.95	V
Control Voltage (3)	V _{C3}	V _{in} = 70dBμ, Pin② DC voltage	2.55	3.25	3.95	V
Control Voltage (4)	V _{C4}	V _{in} = 100dBμ, Pin② DC voltage	4.15	5.10	5.95	V
Control Voltage (5)	V _{C5}	V _{C5} = V _{C3} - V _{C2}	1.55	1.75	1.95	V
Control Voltage (6)	V _{C6}	V _{C6} = V _{C4} - V _{C3}	1.65	1.85	2.05	V
AFC Offset Voltage	V _{AFC}	No signal input. DC voltage between Pin⑩ and ⑨	-0.065	0	0.065	V
Output Level L	V _{OL}	V _{in} = 70dBμ, Pin⑩ AC voltage	105	125	145	mVrms
Output Level R	V _{OR}	V _{in} = 70dBμ, Pin⑨ AC voltage	105	125	145	mVrms
Channel Balance	CB	CB = 20log (V _{OL} /V _{OR})	-1	0	1	dB
Limiting Sensitivity	V _{lim}	V _{OL} = 0dB, Input level at which input Pin⑩ AC voltage decreases by 3dB	18	24	28	dBμV
Residual Pilot Voltage	V _{PC}	V _{in} = 70dBμ, Pilot signal 10% modulation, Pin⑫ AC voltage	—	7	14	mVrms
Stereo Lamp ON Level	Lamp _(ON)	Modulation only by pilot signal. Pin⑮ DC voltage < 2V	2.0	4.7	6.3	%
Stereo Lamp OFF Level	Lamp _(OFF)	Modulation only by pilot signal. Stereo lamp ON/OFF level ratio	2	4.5	7	dB
Separation Lch	Sep. L	V _{in} = 70dBμ, L + R = 90% Pilot 10%	22	35	—	dB
Separation Rch	Sep. R	V _{in} = 70dBμ, L + R = 90% Pilot 10%	22	35	—	dB
Capture range	CR	V _{in} = 70dBμ, Pilot signal 8% modulation	±0.45	±1	—	%
Counter Output Level (1)	V _{IF1}	V _{in} = 70dBμ, Pin⑲ = 0V, Pin⑳ 10.7MHz output voltage	0	1	5	mVrms
Counter Output Level (2)	V _{IF2}	V _{in} = 70dBμ, Pin⑲ = V _{CC} , Pin⑳ AC output voltage	50	65	80	mVrms
Supply Current	I _{tot}	No input, Pin⑮ = 0V	29.5	36.5	43.5	mA
Monaural THD (Lch)	THDL	Monaural input 400mV, 1kHz, Lch distortion	—	0.15	0.3	%
Monaural THD (Rch)	THDR	Monaural input 400mV, 1kHz, Rch distortion	—	0.15	0.3	%
Stereo THD (Lch)	THD SL	Stereo, L + R = 360mV, V _p = 40mV, Lch distortion	—	0.15	0.3	%
Stereo THD (Rch)	THD SR	Stereo, L + R = 360mV, V _p = 40mV, Rch distortion	—	0.15	0.3	%
AGC Voltage (1)	V _{AGC1}	Input = 0mVrms, R _S = 600Ω, Pin㉓ DC voltage	—	0	0.4	V
AGC Voltage (2)	V _{AGC2}	Input V _{in2} = 2mVrms, 150kHz, Pin㉓ DC voltage	1.3	1.48	1.65	V
Noise Detection Voltage	V _{DET}	V _{in2} = 100mVrms, 150kHz, Pin㉓ DC voltage	—	0	0.3	V
Gate Pulse Width	PW	V _{in2} = 0.3V _{p-p} , tw = 1μs, f = 1kHz, Pin⑫ output	23	28	33	μs
Residual Noise Voltage	V _{NR}	V _{in2} = 1V _{p-p} , tw = 10μs, f = 1kHz, Input through LPF, Lch output	—	0	0.7	mVrms
SD Frequency Band Width	SDW	Frequency band width when SD output is 4.5V or more (V ₂₉ = 2V)	60	100	140	kHz
SD Sensitivity	SDS	Input when SD output is 4.5V or more (V ₂₉ = 2V)	38	44	56	dBμ

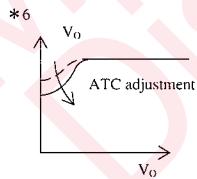
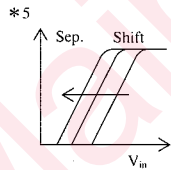
■ Description on Pins Show in the Diagram of the Application Circuit



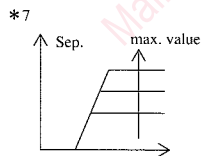
*2 HPF for multipath detection
Too low f_c decreases Sep. at high modulation



*4 Capacitor for S-meter detection 0.1 to 1 μ F at multipath detection



Insert C if noise is conspicuous.

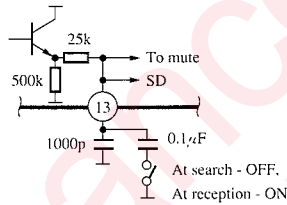


*8 f (time) setting at ATC ON

*9 75 μ s for de-emphasis

*10 Pin 11 input Amp. $\approx 400k \Omega$
0.1 μ is min.
The larger the better

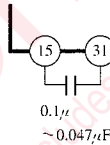
*11 1 Soft mute time constant setting
2 SD rise time constant



*12 For pilot detection
If small, lamp on.
malfunction

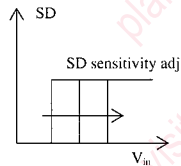
*13 3.9V < V_{15} < V_{CC} ... V_{CC} stop
1.7V < V_{15} < 3.2V ... Forced monaural
0V < V_{15} < 1.0V ... Stereo mode

When Pin 15 is not used, preferably insert C between V_{CC} .



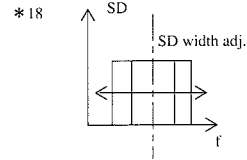
*14 For pilot canceler
Pseudo sine wave output : $c = 6800pF$ to 0.015 μ F

*15

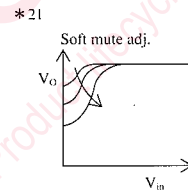
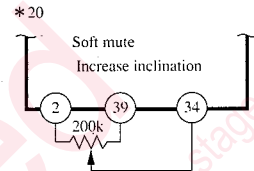


*16 IF counter output (Keep it away from input)

*17 $V_{29} < 0.2V$... IF counter OFF
 $V_{29} > 1V$... IF counter ON



*19 Several k Ω THD improved



*22 Regulator by-pass
(Pay attention to GND location)

*23 Change to applications.

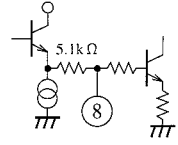
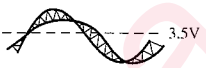
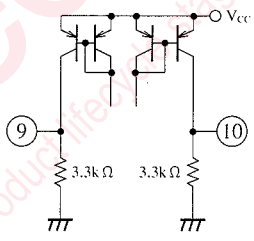

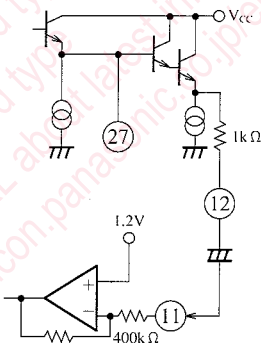

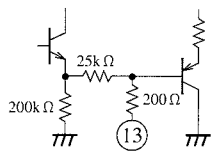
*24 1st limiter bypass
(Pay attention to GND location)

Pin Description (AN7292NSC)

Pin No.	Pin Name	Pin Waveform, Voltage	I/O Impedance	Equivalent Circuit
1	V _{CONT.} Adj.	DC ≈ 3.5V	Low	
2	V _{CONT.} OUT (Level Meter)		200 Ω	
6	ATC Adj.	$V_6 = \frac{R_6}{57k\Omega + R_6} V_2$	57k Ω	
3	AMDC IN	DC about 1.9V	Low	
4	AMDC Peak Det.		Rise Low Fall 330k Ω	
5	AMDC Adj.	DC about 2.3V or less	14.5k Ω	
NOTE) AMDC: Automatic Multi Path Distortion Canceller				
7	Separation Adj.	DC (max.) ≈ 1.2V AC = 0 ~ V _{ii}	2k Ω	

ICs for Tuner

Pin Description (Cont.) (AN7292NSC)

Pin No.	Pin Name	Pin Waveform, Voltage	I/O Impedance	Equivalent Circuit
8	ATC L. P. F	Same as V_{11} , however level of high frequency band down by external capacitor $V_{DC} \approx 2V$	5.1k Ω	
9	L-ch. OUT	AC varies with input condition. 	3.3k Ω	
10	R-ch. OUT	AC varies with input condition. 	3.3k Ω	
11	MPX. IN	AC : Same as for Pin 12 DC = 1.3V	400k Ω	
12	NC. OUT	$\approx V_{IN} = V_{O(FM\ DECT)}$ 	1k Ω	
27	NC. Hold	$V_{(AC)} \approx V_{12}$ $V_{(DC)} \approx 3.3V$	Low	
13	Soft Mute Time Const.	DC $\approx 0V \sim 4.1V$	25k Ω	

■ Pin Description (Cont.) (AN7292NSC)

Pin No.	Pin Name	Pin Waveform, Voltage	I/O Impedance	Equivalent Circuit																				
14	Pilot Det. L. P. F	$DC \approx V_{CC} - 1.4V$	$R = 36k\Omega$																					
18	Pi. Can. Control L. P. F	$DC \approx V_{CC} - 1.4V$	$R = 68k\Omega$																					
15	ST/Mono. Control	<table border="1"> <thead> <tr> <th>Pin Voltage</th> <th>Demodulation</th> <th>LED</th> <th>Pilot Can.</th> <th>VCO</th> </tr> </thead> <tbody> <tr> <td>0V ~ 1V</td> <td>○</td> <td>○</td> <td>○</td> <td>○</td> </tr> <tr> <td>1.7V ~ 3.2V</td> <td>×</td> <td>×</td> <td>○</td> <td>○</td> </tr> <tr> <td>3.9V ~ V_{CC}</td> <td>×</td> <td>×</td> <td>×</td> <td>×</td> </tr> </tbody> </table>	Pin Voltage	Demodulation	LED	Pilot Can.	VCO	0V ~ 1V	○	○	○	○	1.7V ~ 3.2V	×	×	○	○	3.9V ~ V _{CC}	×	×	×	×	High	
		Pin Voltage	Demodulation	LED	Pilot Can.	VCO																		
		0V ~ 1V	○	○	○	○																		
		1.7V ~ 3.2V	×	×	○	○																		
3.9V ~ V _{CC}	×	×	×	×																				
16	PLL L. P. F	$DC \approx 4.3V$	$R = 66k\Omega$																					
17	VCO (Ceramic resonator Pin)	 $f = 912kHz$ $AC \approx 3V_{p-p}$	High																					
19	Pi. Can. Quasi-sin	 $f = 19kHz$ $AC \approx 100mV_{p-p}$	—																					

ICs for Tuner

■ Pin Description (Cont.) (AN7292NSC)

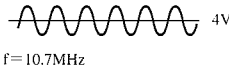
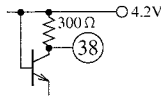
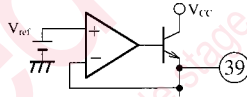
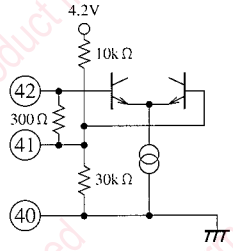
Pin No.	Pin Name	Pin Waveform, Voltage	I/O Impedance	Equivalent Circuit
20	AGC Amp. L. P. F	DC ≈ 3.5V AC is noise.	6.2k Ω	
21	Pulse Amp. L. P. F	DC ≈ 4.2V AC is noise.	2.7k Ω	
22	Gate Time Adj.		Usually High Low at Operation	
23	Noise Amp. AGC		10 Rise 15k Ω Fall High	
24	NC IN		500k Ω	
25	NC H. P. F	Level of low frequency band down from Pin 24 waveform. DC is determined by external voltage (4.2V).	High	
26	IF Det. OUT	 (Varies with input conditions)	3.3k Ω	
28	IF Count Out SD Out	DC ≈ 5V (at tuning) ≈ 0V (at detuning) 10.7MHz when DC ≈ 5V	1k Ω	

Pin Description (Cont.) (AN7292NSC)

Pin No.	Pin Name	Pin Waveform, Voltage	I/O Impedance	Equivalent Circuit
29	SCC [Seek Sence. Adj.]	Apply bias voltage from outside. IF counter stops when $V_{29} < 0.3V$, SD=L fixed	200k Ω	
30	AFC OUT	 4.2V f_{m-IF1}	50k Ω	
31	V _{cc}	8V	Low	
32	Quad. IN	DC=8V (Determined by external voltage) < 90° phase shift	High	
33	Limiter OUT	 7.6V $f = 10.7MHz$	500 Ω	
34	Soft Mute Adj.	Voltage input from outside 0V ~ V _{ref} (4.2V)	High	
35	LED Driver	At stereo DC=0V ~ 0.5V	Low	
		At monaural Determined by external voltage	High	
36	2nd IF IN	$\approx 0V$	300 Ω	

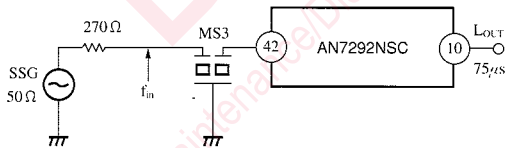
ICs for Tuner

■ Pin Description (Cont.) (AN7292NSC)

Pin No.	Pin Name	Pin Waveform, Voltage	I/O Impedance	Equivalent Circuit
37	System GND	0V	Low	—————
38	IF1 Limiter OUT	 4V f = 10.7MHz	300 Ω	
39	V _{ref}	4.2V constant voltage	Low	
40	IF GND	—————	Low	
41	IF Amp. Bypass	DC = 3.1V	7.5k Ω	
42	IF IN	DC = 3.1V AC = V _{in} (IF)	300 Ω	

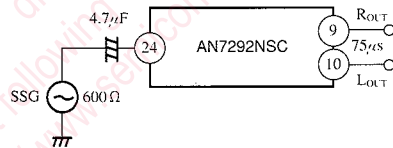
■ Characteristic Curve

① Measuring Condition at IF Input

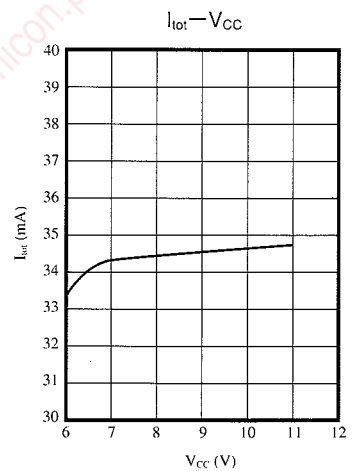
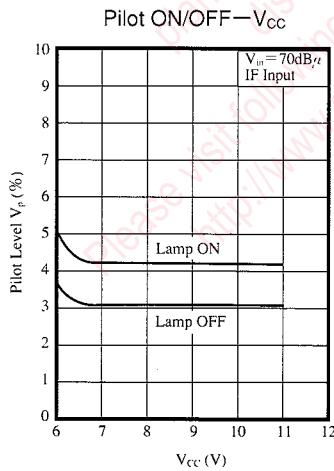
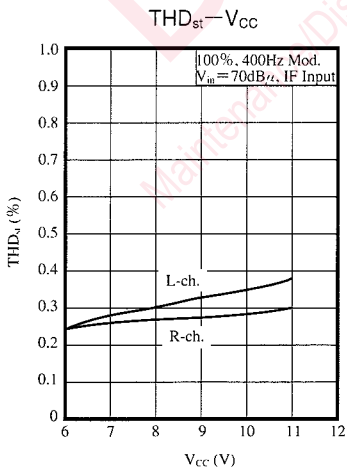
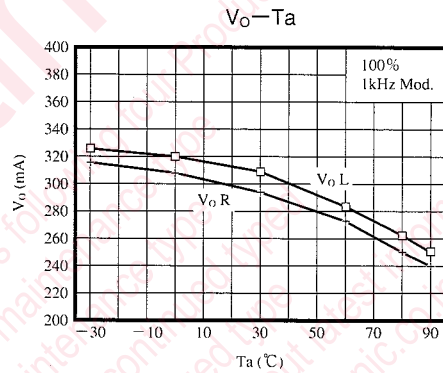
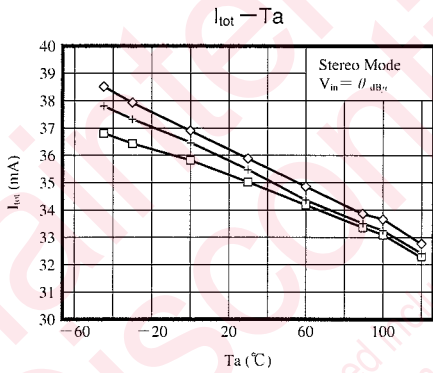
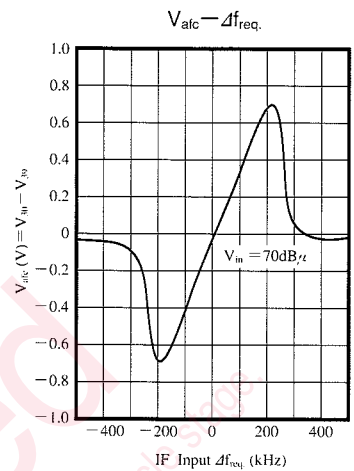
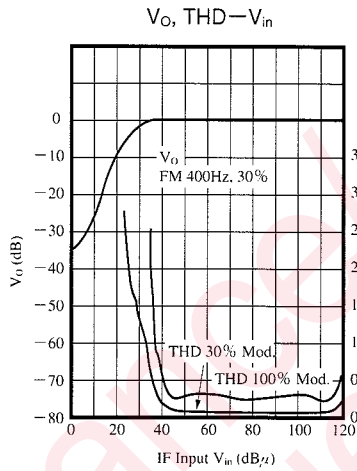
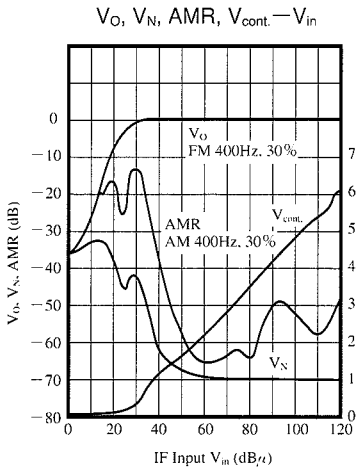


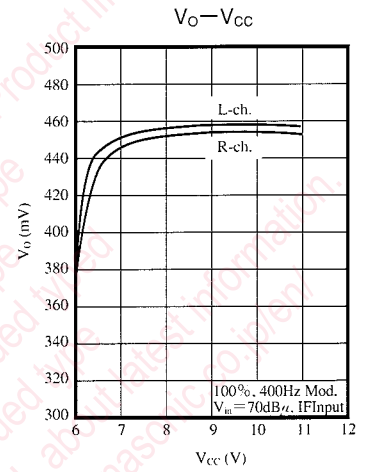
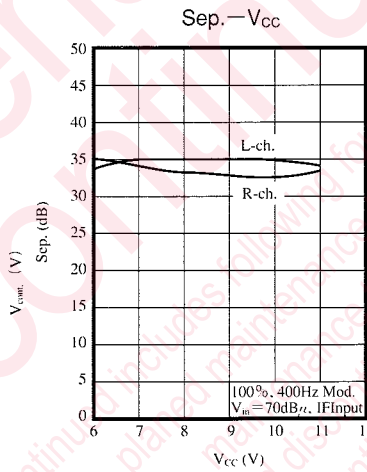
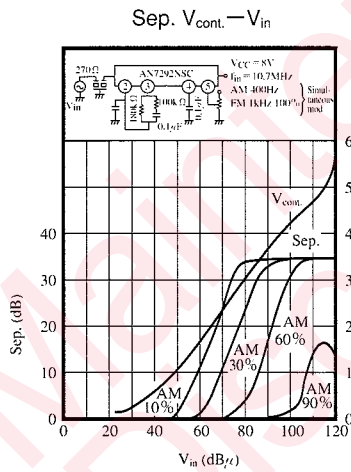
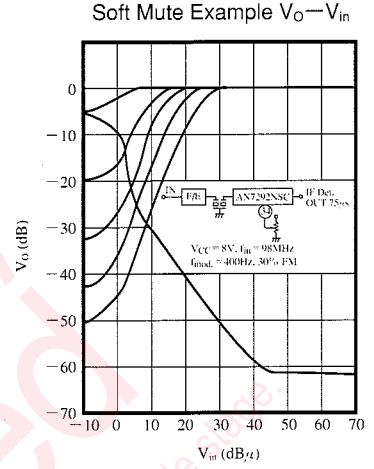
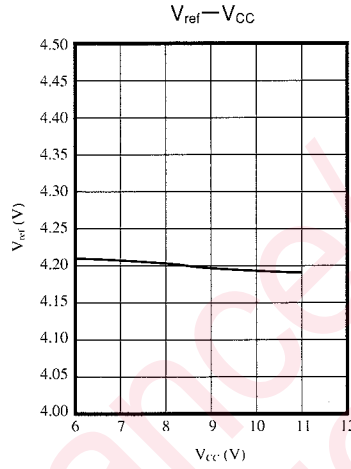
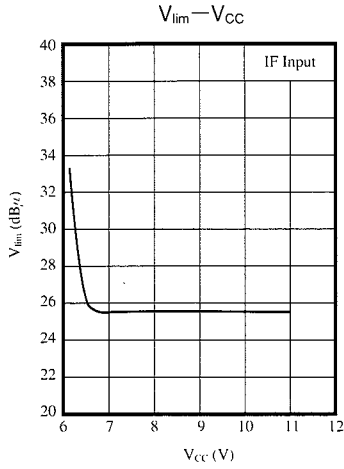
Unless otherwise specified,
 $V_{CC} = 8V$, $f_{in} = 10.7MHz$
 FM Modulation 30%, 400Hz, $V_{in} = 70dB_{\mu}$

② Measuring Condition at NC Input

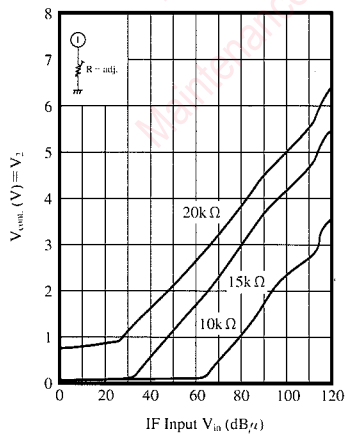


Unless otherwise specified, $V_{CC} = 8V$, $f_{in} = 1kHz$,
 $V_{in} = 400mV$ (Monaural)
 $L + R = 360mV$ (Stereo)
 $V_P = 40mV$ (Stereo)

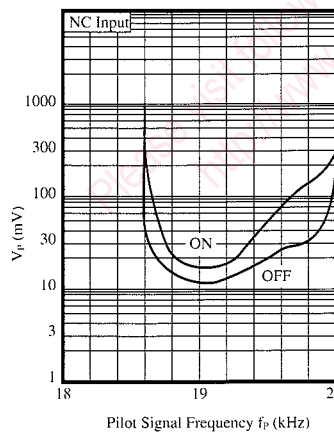




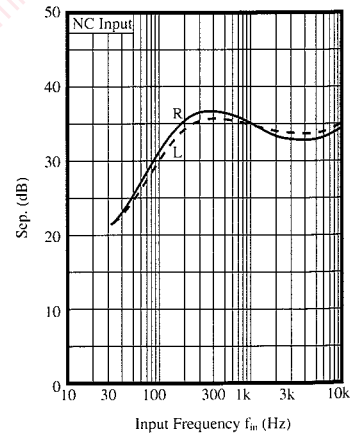
Control Voltage Control Example

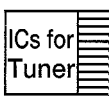
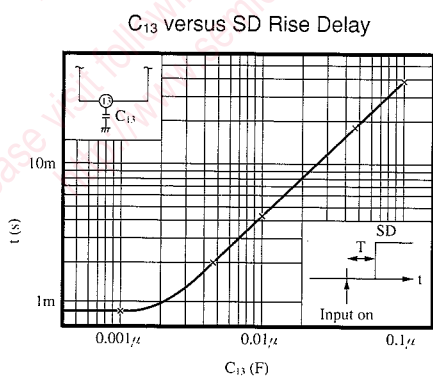
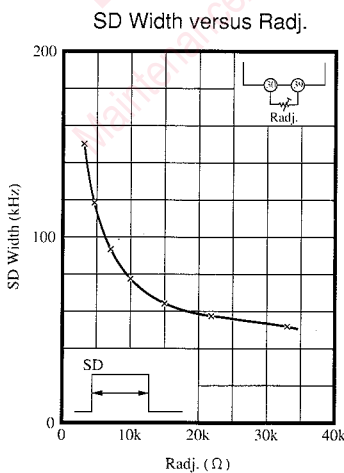
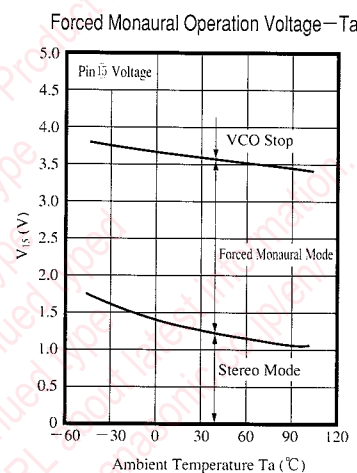
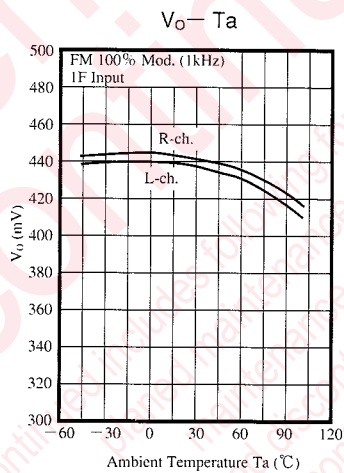
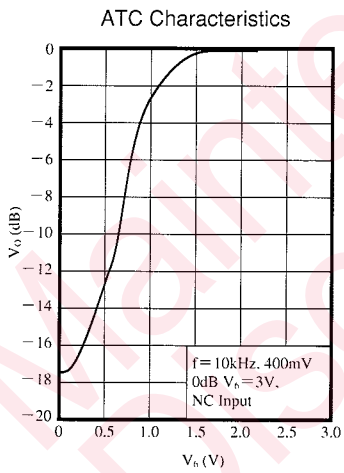
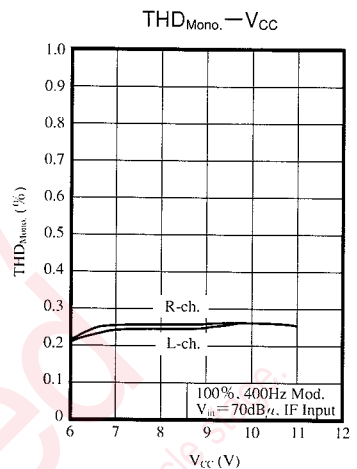
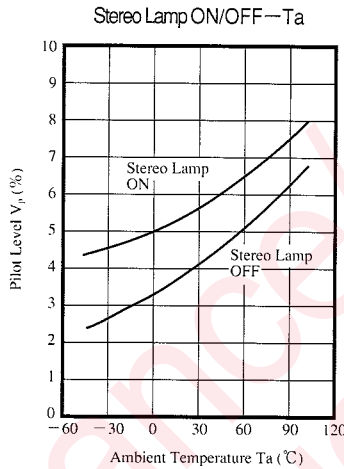
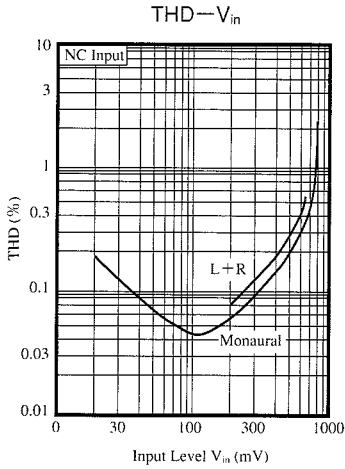


Lamp ON/OFF - f_p



Sep. - f_{in}





Supplementary Explanation

[1] On Multipath Distortion Preventive Circuit (AN7292NSC pin numbers are used below)

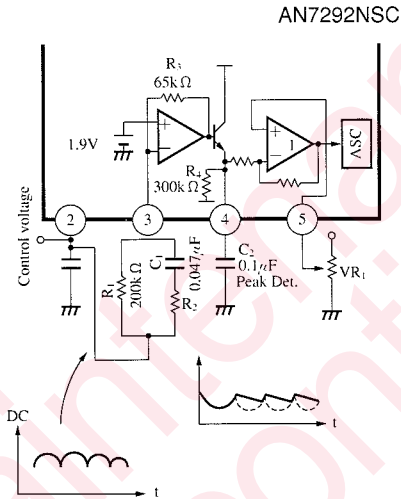
1. Principle

Multipath distortion is apt to increase especially in the stereo receiving mode. In consideration of this phenomenon, the AN7292NSC has been designed so as to suppress the feeling of physical disorder incidental to multipath noise by degrading the separation against multipath distortion.

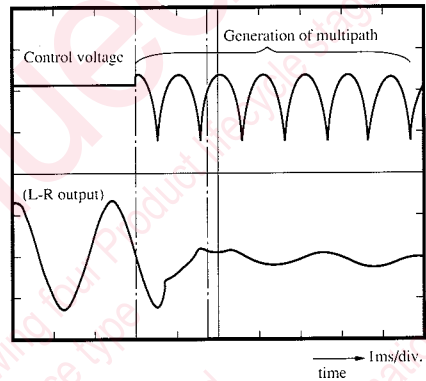
Detection method : Detection of AM components included in control voltage (level meter) output

Separation method : Operation of conventional ASC circuit by conversion of detected AM components into DC voltage

2. Circuit and Operation

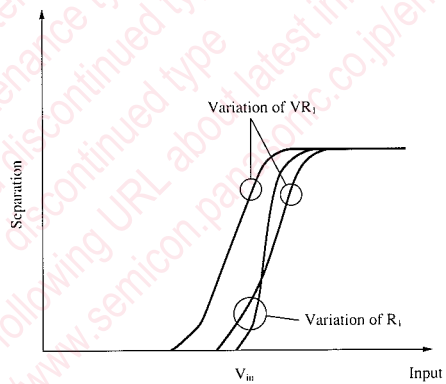


3. Actual Operation Example



(1) Operation in a state free from multipath
(Operation as ASC)

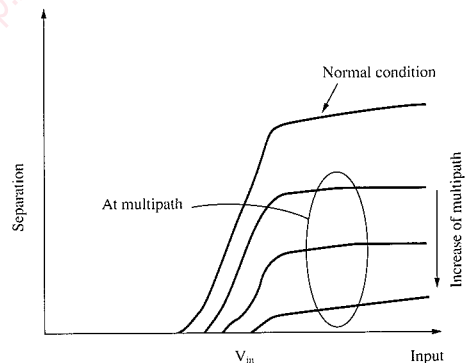
The control voltage of ② is sent to the ASC through the two operational amplifiers. The gradient of the characteristics curve can be set by R_3/R_1 , and the start point can be set by VR_1 .



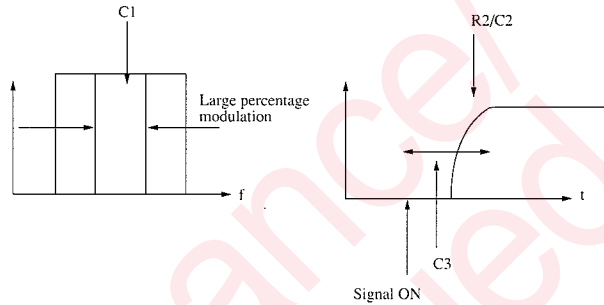
(2) Operation in a state exposed to multipath

The variation to appear in the control voltage on account of multipath distortion is put to AM detection, and the DC voltage to the ASC is suitably lowered to degrade the separation.

The frequency characteristics of the AM components are adjusted through C_1 shown in the sketch, and the AM components are put to peak value detection by R_4, C_2 .



- C1 of Pin⑩ relates to SD at large percentage modulation.($0.33\mu \sim 0.47\mu\text{F}$)
 ※It must be increased when THD in the low frequency band is deteriorated. (up to $3.3\mu\text{F}$)
- C3 of Pin⑬ determines the time to SD rise after signal input.
 The rise time is about 1ms at 1000pF and about 2ms at 4700pF.
- R2/C2 of Pin⑳ is a filter decreasing the IF counter components and relates to the speed of rise components.

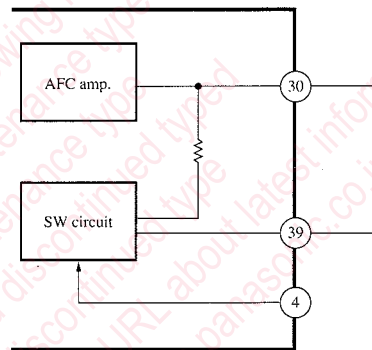


For these topics, refer to the data.

3. Miscellaneous

The SD of AN7292NSC has the function to narrow the band width when the voltage of Pin④ increases to 1.9V or more.

It works so as to increase the inclination of S-curve to operate the SD band mute more positively when signals are disrupted.



SD band variable

[3] Selection Standard of Noise Canceler Resistance Value

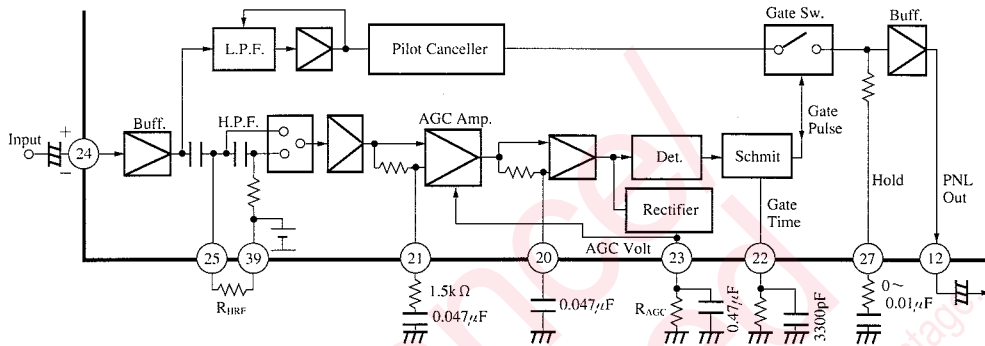


Fig.1 Pulse Noise Limiter (PNL) Block Diagram

(1) Relation to field strength

1. In weak electric field

In a weak electric field where noise is apt to increase, the AGC effectively controls the PNL operation.

a) In case operation error is frequently caused by white noise

Suitably increase the value of Pin²³ R_{AGC} (220k Ω to 1M Ω).

b) In case operation error is frequently caused by overmodulation.

Suitably increase the value of R_{HPF} between Pin²⁵ and ³⁹ R_{HPF} (47k Ω to 470k Ω).

2. In medium to strong electric field

In a medium to strong electric field relatively free from noise generation, the AGC becomes less effective and noise is detected almost at the maximum sensitivity.

a) In case the detection sensitivity is too high

Suitably decrease the value of Suitably decrease the value of R_{HPF} between Pin²⁵ and ³⁹ (10k Ω to 47k Ω).

3. In every electric filed

a) In case the detection sensitivity is excellent but the PNL effect deteriorated due to holding level fluctuation by noise, suitably increase the resistance value of the resistor connected in series with the Pin²⁷ holding capacitor (1k Ω to 4.7k Ω).b) In case noise of the gate pulse itself is conspicuous, suitably narrow the gate pulse width by decreasing the resistance value of the Pin²² resistor (3k Ω to 6.8k Ω).

(2) Selection of AGC Resistor R_{AGC} Pin 23

Pin 23 is the AGC LPF, and enables AGC effective level adjustment. The equivalent circuit in the vicinity of this pin has been so constituted as shown in Fig. 2, and the output impedance at the charging time is $15k\Omega$ while the input impedance at the discharging time is about $1M\Omega$.

The standard value of R_{AGC} is $330k\Omega$, but in case operation error is frequently caused in a weak electric field by white noise, selectively increase the value of R_{AGC} to a suitable level between $200k\Omega$ and $1M\Omega$. So long as the value of R_{AGC} was properly increased, the AGC voltage proportionally becomes higher to prolong the discharging time constant, and the rate of operation error sharply drops with decrease of the gain of the AGC Amp. (Though Pin 23, the noise components are put to peak (envelope) detection. Even if the value of R_{AGC} was increased, the charging time and voltage remain almost unchanged because $Z_O = 15k\Omega$.)

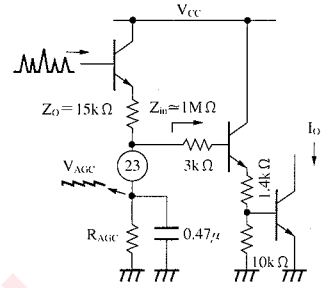
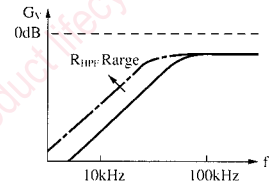


Fig. 2

(3) Selection of HPF Resistor R_{HPF} Pin 25

When the resistance value R_{HPF} of the resistor between Pin 25 and 30 was increased, the cut-off frequency of the HPF proportionally becomes lower.

The standard value of R_{HPF} is $330k\Omega$, but in case operation error is frequently caused in a weak electric field by white noise at the modulation time or non-modulation time, selectively increase this R_{HPF} to a suitable value not exceeding $470k\Omega$.



[4] Precautions on PNL Use

Care should be taken to use the PNL, because under the following conditions, in the PNL circuit of this IC, the output wave form may be distorted due to oscillation.

1. Oscillation conditions

When the PNL is used under the conditions described in the following items (1) to (3) and the PNL – AGC voltage (Pin 23 voltage) becomes 2.3V or more, oscillation may occur.

- (1) The PNL input frequency is 15kHz or more and $500mV_{rms}$ is exceeded.
- (2) The voltage of AGC pin (Pin 23) is forced to exceed the above voltage.
- (3) The voltage AC or DC of \pm several ten mV or more is directly applied to the PNL filter pins (Pin 20 and Pin 21). The oscillation occurrence depends on V_{CC} .

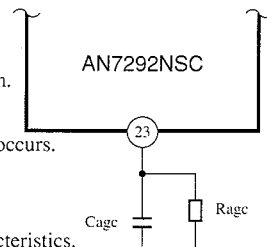
The oscillation can not be stopped unless V_{CC} is much increased, if it occurs. The above three conditions are not given under the normal operation, and therefore oscillation problems are not suffered in practical use.

However, in the review stage, keep in mind that oscillation may occur when the above conditions are given.

2. Effect by external components

The PNL circuit oscillation depends on an external resistor and capacitor of AGC pin.

- (1) C_{agc} is currently set to $0.47\mu F$. The larger it is, the less frequently oscillation occurs.
- (2) R_{agc} is $330k\Omega$. The smaller it is, the less frequently oscillation occurs.



When the above values are changed, take sufficient consideration for setting characteristics.

Also, when the use under the special conditions is expected, review the countermeasures against oscillation.

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