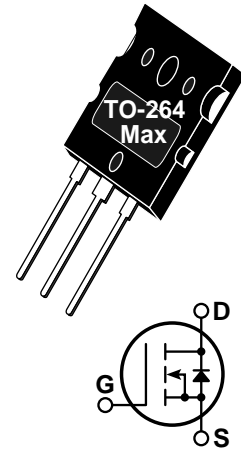


### POWER MOS 7™

Power MOS 7™ is a new generation of low loss, high voltage, N-Channel enhancement mode power MOSFETS. Both conduction and switching losses are addressed with Power MOS 7™ by significantly lowering  $R_{DS(ON)}$  and  $Q_g$ . Power MOS 7™ combines lower conduction and switching losses along with exceptionally fast switching speeds inherent with APT's patented metal gate structure.

- Lower Input Capacitance
- Lower Miller Capacitance
- Lower Gate Charge,  $Q_g$
- Increased Power Dissipation
- Easier To Drive
- Popular TO-264 MAX Package



#### MAXIMUM RATINGS

All Ratings:  $T_C = 25^\circ\text{C}$  unless otherwise specified.

Symbol	Parameter	APT12040L2LL	UNIT
$V_{DSS}$	Drain-Source Voltage	1200	Volts
$I_D$	Continuous Drain Current @ $T_C = 25^\circ\text{C}$	30	Amps
$I_{DM}$	Pulsed Drain Current <sup>①</sup>	120	
$V_{GS}$	Gate-Source Voltage Continuous	$\pm 30$	Volts
$V_{GSM}$	Gate-Source Voltage Transient	$\pm 40$	
$P_D$	Total Power Dissipation @ $T_C = 25^\circ\text{C}$	890	Watts
	Linear Derating Factor	7.12	W/°C
$T_J, T_{STG}$	Operating and Storage Junction Temperature Range	-55 to 150	°C
$T_L$	Lead Temperature: 0.063" from Case for 10 Sec.	300	
$I_{AR}$	Avalanche Current <sup>①</sup> (Repetitive and Non-Repetitive)	30	Amps
$E_{AR}$	Repetitive Avalanche Energy <sup>①</sup>	50	mJ
$E_{AS}$	Single Pulse Avalanche Energy <sup>④</sup>	3200	

#### STATIC ELECTRICAL CHARACTERISTICS

Symbol	Characteristic / Test Conditions	MIN	TYP	MAX	UNIT
$BV_{DSS}$	Drain-Source Breakdown Voltage ( $V_{GS} = 0V, I_D = 250\mu\text{A}$ )	1200			Volts
$I_{D(on)}$	On State Drain Current <sup>②</sup> ( $V_{DS} > I_{D(on)} \times R_{DS(on)}$ Max, $V_{GS} = 10V$ )	30			Amps
$R_{DS(on)}$	Drain-Source On-State Resistance <sup>②</sup> ( $V_{GS} = 10V, 0.5 I_{D(Cont.)}$ )			0.400	Ohms
$I_{DSS}$	Zero Gate Voltage Drain Current ( $V_{DS} = V_{DSS}, V_{GS} = 0V$ )			100	$\mu\text{A}$
	Zero Gate Voltage Drain Current ( $V_{DS} = 0.8 V_{DSS}, V_{GS} = 0V, T_C = 125^\circ\text{C}$ )			500	
$I_{GSS}$	Gate-Source Leakage Current ( $V_{GS} = \pm 30V, V_{DS} = 0V$ )			$\pm 100$	nA
$V_{GS(th)}$	Gate Threshold Voltage ( $V_{DS} = V_{GS}, I_D = 5\text{mA}$ )	3		5	Volts

 **CAUTION:** These Devices are Sensitive to Electrostatic Discharge. Proper Handling Procedures Should Be Followed.

APT Website - <http://www.advancedpower.com>

**DYNAMIC CHARACTERISTICS**

**APT12040L2LL**

Symbol	Characteristic	Test Conditions	MIN	TYP	MAX	UNIT
C <sub>iss</sub>	Input Capacitance	V <sub>GS</sub> = 0V V <sub>DS</sub> = 25V f = 1 MHz		8690		pF
C <sub>oss</sub>	Output Capacitance			1200		
C <sub>rss</sub>	Reverse Transfer Capacitance			908		
Q <sub>g</sub>	Total Gate Charge ③	V <sub>GS</sub> = 10V V <sub>DD</sub> = 0.5 V <sub>DSS</sub> I <sub>D</sub> = I <sub>D[Cont.]</sub> @ 25°C		306		nC
Q <sub>gs</sub>	Gate-Source Charge			37		
Q <sub>gd</sub>	Gate-Drain ("Miller") Charge			182		
t <sub>d(on)</sub>	Turn-on Delay Time	V <sub>GS</sub> = 15V V <sub>DD</sub> = 0.5 V <sub>DSS</sub> I <sub>D</sub> = I <sub>D[Cont.]</sub> @ 25°C R <sub>G</sub> = 0.6Ω		21		ns
t <sub>r</sub>	Rise Time			14		
t <sub>d(off)</sub>	Turn-off Delay Time			67		
t <sub>f</sub>	Fall Time			24		

**SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS**

Symbol	Characteristic / Test Conditions	MIN	TYP	MAX	UNIT
I <sub>S</sub>	Continuous Source Current (Body Diode)			30	Amps
I <sub>SM</sub>	Pulsed Source Current ① (Body Diode)			120	
V <sub>SD</sub>	Diode Forward Voltage ② (V <sub>GS</sub> = 0V, I <sub>S</sub> = -I <sub>D[Cont.]</sub> )			1.3	Volts
t <sub>rr</sub>	Reverse Recovery Time (I <sub>S</sub> = -I <sub>D[Cont.]</sub> , di <sub>S</sub> /dt = 100A/μs)		1250		ns
Q <sub>rr</sub>	Reverse Recovery Charge (I <sub>S</sub> = -I <sub>D[Cont.]</sub> , di <sub>S</sub> /dt = 100A/μs)		31.0		μC
dv/dt	Peak Diode Recovery dv/dt ⑤			10	V/ns

**THERMAL CHARACTERISTICS**

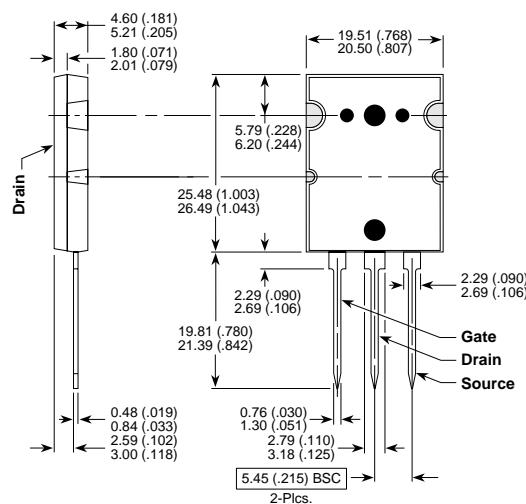
Symbol	Characteristic	MIN	TYP	MAX	UNIT
R <sub>θJC</sub>	Junction to Case			0.14	°C/W
R <sub>θJA</sub>	Junction to Ambient			40	

- ① Repetitive Rating: Pulse width limited by maximum junction temperature.
- ② Pulse Test: Pulse width < 380 μs, Duty Cycle < 2%

- ③ See MIL-STD-750 Method 3471
- ④ Starting T<sub>j</sub> = +25°C, L = 7.11mH, R<sub>G</sub> = 25Ω, Peak I<sub>L</sub> = 30A
- ⑤ dv/dt numbers reflect the limitations of the test circuit rather than the device itself. I<sub>S</sub> ≤ -I<sub>D[Cont.]</sub> di<sub>S</sub>/dt ≤ 700A/μs V<sub>R</sub> ≤ V<sub>DSS</sub> T<sub>J</sub> ≤ 150°C

APT Reserves the right to change, without notice, the specifications and information contained herein.

**TO-264 MAX™(L2) Package Outline**



Dimensions in Millimeters and (Inches)

APT's devices are covered by one or more of the following U.S. patents: 4,895,810 5,045,903 5,089,434 5,182,234 5,019,522 5,262,336  
5,256,583 4,748,103 5,283,202 5,231,474 5,434,095 5,528,058



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