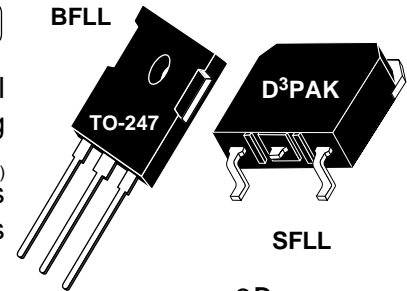
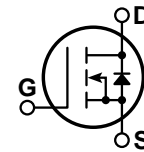


POWER MOS 7™
FREDFET
BFLL

SFLL


Power MOS 7™ is a new generation of low loss, high voltage, N-Channel enhancement mode power MOSFETS. Both conduction and switching losses are addressed with Power MOS 7™ by significantly lowering $R_{DS(ON)}$ and Q_g . Power MOS 7™ combines lower conduction and switching losses along with exceptionally fast switching speeds inherent with APT's patented metal gate structure.

- Lower Input Capacitance
- Lower Miller Capacitance
- Lower Gate Charge, Q_g
- Increased Power Dissipation
- Easier To Drive
- TO-247 or Surface Mount D³PAK Package
- **FAST RECOVERY BODY DIODE**

MAXIMUM RATINGS

 All Ratings: $T_C = 25^\circ\text{C}$ unless otherwise specified.

Symbol	Parameter	APT5024	UNIT
V_{DSS}	Drain-Source Voltage	500	Volts
I_D	Continuous Drain Current @ $T_C = 25^\circ\text{C}$	22	Amps
I_{DM}	Pulsed Drain Current ^①	88	
V_{GS}	Gate-Source Voltage Continuous	±30	Volts
V_{GSM}	Gate-Source Voltage Transient	±40	
P_D	Total Power Dissipation @ $T_C = 25^\circ\text{C}$	265	Watts
	Linear Derating Factor	2.12	W/°C
T_J, T_{STG}	Operating and Storage Junction Temperature Range	-55 to 150	°C
T_L	Lead Temperature: 0.063" from Case for 10 Sec.	300	
I_{AR}	Avalanche Current ^① (Repetitive and Non-Repetitive)	22	Amps
E_{AR}	Repetitive Avalanche Energy ^①	30	mJ
E_{AS}	Single Pulse Avalanche Energy ^④	960	

STATIC ELECTRICAL CHARACTERISTICS

Symbol	Characteristic / Test Conditions	MIN	TYP	MAX	UNIT
BV_{DSS}	Drain-Source Breakdown Voltage ($V_{GS} = 0V, I_D = 250\mu\text{A}$)	500			Volts
$I_{D(on)}$	On State Drain Current ^② ($V_{DS} > I_{D(on)} \times R_{DS(on)}$ Max, $V_{GS} = 10V$)	22			Amps
$R_{DS(on)}$	Drain-Source On-State Resistance ^② ($V_{GS} = 10V, 0.5 I_{D[Cont.]}$)			0.240	Ohms
I_{DSS}	Zero Gate Voltage Drain Current ($V_{DS} = V_{DSS}, V_{GS} = 0V$)			250	μA
	Zero Gate Voltage Drain Current ($V_{DS} = 0.8 V_{DSS}, V_{GS} = 0V, T_C = 125^\circ\text{C}$)			1000	
I_{GSS}	Gate-Source Leakage Current ($V_{GS} = \pm 30V, V_{DS} = 0V$)			±100	nA
$V_{GS(th)}$	Gate Threshold Voltage ($V_{DS} = V_{GS}, I_D = 1\text{mA}$)	3		5	Volts

 **CAUTION:** These Devices are Sensitive to Electrostatic Discharge. Proper Handling Procedures Should Be Followed.

APT Website - <http://www.advancedpower.com>

DYNAMIC CHARACTERISTICS

APT5024 BFLL - SFLL

Symbol	Characteristic	Test Conditions	MIN	TYP	MAX	UNIT
C_{iss}	Input Capacitance	$V_{GS} = 0V$		1910		pF
C_{oss}	Output Capacitance	$V_{DS} = 25V$		390		
C_{rss}	Reverse Transfer Capacitance	$f = 1\text{ MHz}$		30		
Q_g	Total Gate Charge ^③	$V_{GS} = 10V$		48		nC
Q_{gs}	Gate-Source Charge	$V_{DD} = 0.5 V_{DSS}$		13		
Q_{gd}	Gate-Drain ("Miller") Charge	$I_D = I_D [\text{Cont.}] @ 25^\circ\text{C}$		22		
$t_{d(on)}$	Turn-on Delay Time	$V_{GS} = 15V$		12		ns
t_r	Rise Time	$V_{DD} = 0.5 V_{DSS}$		10		
$t_{d(off)}$	Turn-off Delay Time	$I_D = I_D [\text{Cont.}] @ 25^\circ\text{C}$		30		
t_f	Fall Time	$R_G = 1.6\Omega$		7		

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

Symbol	Characteristic / Test Conditions	MIN	TYP	MAX	UNIT
I_S	Continuous Source Current (Body Diode)			22	Amps
I_{SM}	Pulsed Source Current ^① (Body Diode)			88	
V_{SD}	Diode Forward Voltage ^② ($V_{GS} = 0V, I_S = -I_D [\text{Cont.}]$)			1.3	Volts
dv/dt	Peak Diode Recovery dv/dt ^⑤			15	V/ns
t_{rr}	Reverse Recovery Time ($I_S = -I_D [\text{Cont.}], di/dt = 100A/\mu s$)	$T_j = 25^\circ\text{C}$		250	ns
		$T_j = 125^\circ\text{C}$		400	
Q_{rr}	Reverse Recovery Charge ($I_S = -I_D [\text{Cont.}], di/dt = 100A/\mu s$)	$T_j = 25^\circ\text{C}$		1.9	μC
		$T_j = 125^\circ\text{C}$		6	
I_{RRM}	Peak Recovery Current ($I_S = -I_D [\text{Cont.}], di/dt = 100A/\mu s$)	$T_j = 25^\circ\text{C}$		15	Amps
		$T_j = 125^\circ\text{C}$		26	

THERMAL CHARACTERISTICS

Symbol	Characteristic	MIN	TYP	MAX	UNIT
$R_{\theta JC}$	Junction to Case			0.47	$^\circ\text{C/W}$
$R_{\theta JA}$	Junction to Ambient			40	

① Repetitive Rating: Pulse width limited by maximum junction temperature.

② Pulse Test: Pulse width < 380 μs , Duty Cycle < 2%

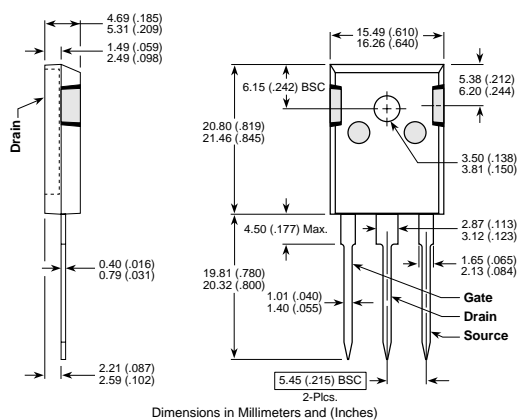
③ See MIL-STD-750 Method 3471

④ Starting $T_j = +25^\circ\text{C}$, $L = 3.97\text{mH}$, $R_G = 25\Omega$, Peak $I_L = 22\text{A}$

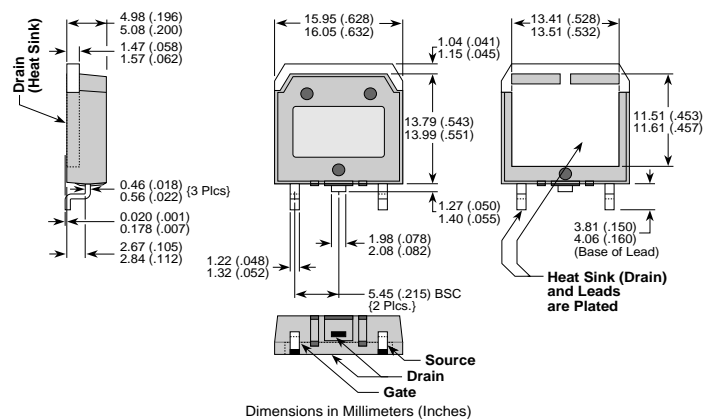
⑤ dv/dt numbers reflect the limitations of the test circuit rather than the device itself. $I_S \leq -I_D [\text{Cont.}]$ $di/dt \leq 700A/\mu\text{s}$ $V_R \leq V_{DSS}$ $T_j \leq 150^\circ\text{C}$

APT Reserves the right to change, without notice, the specifications and information contained herein.

TO-247 Package Outline



D³PAK Package Outline



050-7131 Rev - 10-2001

APT's devices are covered by one or more of the following U.S. patents: 4,895,810 5,045,903 5,089,434 5,182,234 5,019,522 5,262,336
5,256,583 4,748,103 5,283,202 5,231,474 5,434,095 5,528,058



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