

Features

- Fast Read Access Time - 120 ns
- Dual Voltage Range Operation
Unregulated Battery Power Supply Range, 2.7V to 3.6V
or Standard 5V ± 10% Supply Range
- Pin Compatible with JEDEC Standard AT27C4096
- Low Power CMOS Operation
20 µA max. (less than 1 µA typical) Standby for V_{CC} = 3.6V
29 mW max. Active at 5 MHz for V_{CC} = 3.6V
- JEDEC Standard Surface Mount Packages
44-Lead PLCC
40-Lead TSOP (10 x 14mm)
- High Reliability CMOS Technology
2,000V ESD Protection
200 mA Latchup Immunity
- Rapid™ Programming algorithm - 100 µs/word (typical)
- CMOS and TTL Compatible Inputs and Outputs
JEDEC Standard for LVTTTL and LVBO
- Integrated Product Identification Code
- Commercial and Industrial Temperature Ranges

Description

The AT27BV4096 is a high performance, low power, low voltage 4,194,304 bit one-time programmable read only memory (OTP EPROM) organized as 256K by 16 bits. It requires only one supply in the range of 2.7V to 3.6V in normal read mode operation. The by-16 organization makes this part ideal for portable and handheld 16 and 32 bit microprocessor based systems using either regulated or unregulated battery power.

(continued)

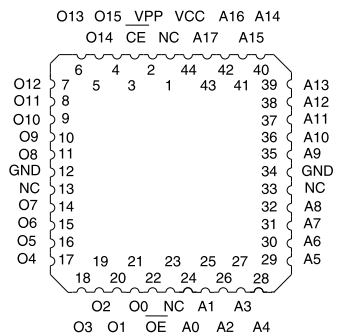
**4 Megabit
(256K x 16)
Unregulated
Battery-Voltage™
High Speed
OTP
CMOS EPROM**

Pin Configurations

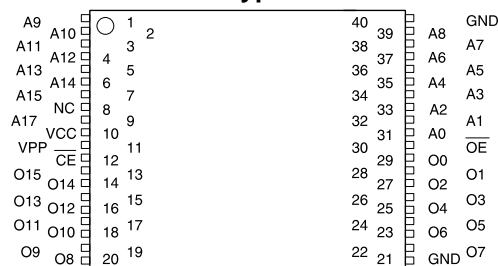
Pin Name	Function
A0 - A17	Addresses
O0 - O15	Outputs
\overline{CE}	Chip Enable
\overline{OE}	Output Enable
NC	No Connect

Note: Both GND pins must be connected.

PLCC Top View



TSOP Top View
Type 1



Note: 1. PLCC package pins 1 and 23 are DON'T CONNECT.

Description (Continued)

Atmel's innovative design techniques provide fast speeds that rival 5V parts while keeping the low power consumption of a 3V supply. At $V_{CC} = 2.7V$, any word can be accessed in less than 120 ns. With a typical power dissipation of only 18 mW at 5 MHz and $V_{CC} = 3V$, the AT27BV4096 consumes less than one fifth the power of a standard 5V EPROM.

Standby mode supply current is typically less than 1 μA at 3V. The AT27BV4096 simplifies system design and stretches battery lifetime even further by eliminating the need for power supply regulation.

The AT27BV4096 is available in industry standard JEDEC-approved one-time programmable (OTP) plastic PLCC and TSOP packages. All devices feature two-line control (CE, OE) to give designers the flexibility to prevent bus contention.

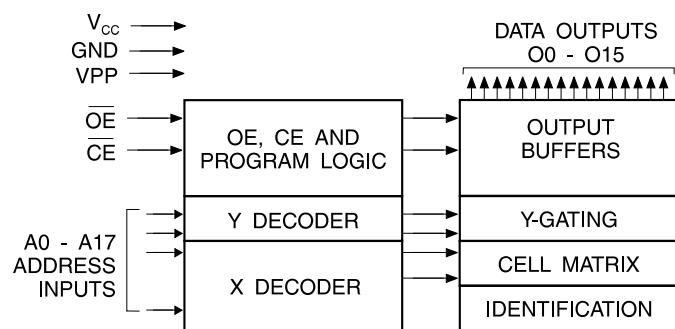
The AT27BV4096 operating with V_{CC} at 3.0V produces TTL level outputs that are compatible with standard TTL logic devices operating at $V_{CC} = 5.0V$. At $V_{CC} = 2.7V$, the part is compatible with JEDEC approved low voltage battery operation (LVBO) interface specifications. The device is also capable of standard 5-volt operation making it ideally suited for dual supply range systems or card products that are pluggable in both 3-volt and 5-volt hosts.

Atmel's AT27BV4096 has additional features to ensure high quality and efficient production use. The Rapid™ Programming Algorithm reduces the time required to program the part and guarantees reliable programming. Programming time is typically only 100 μs /word. The Integrated Product Identification Code electronically identifies the device and manufacturer. This feature is used by industry standard programming equipment to select the proper programming algorithms and voltages. The AT27BV4096 programs exactly the same way as a standard 5V AT27C4096 and uses the same programming equipment.

System Considerations

Switching between active and standby conditions via the Chip Enable pin may produce transient voltage excursions. Unless accommodated by the system design, these transients may exceed data sheet limits, resulting in device non-conformance. At a minimum, a 0.1 μF high frequency, low inherent inductance, ceramic capacitor should be utilized for each device. This capacitor should be connected between the V_{CC} and Ground terminals of the device, as close to the device as possible. Additionally, to stabilize the supply voltage level on printed circuit boards with large EPROM arrays, a 4.7 μF bulk electrolytic capacitor should be utilized, again connected between the V_{CC} and Ground terminals. This capacitor should be positioned as close as possible to the point where the power supply is connected to the array.

Block Diagram



Absolute Maximum Ratings*

Temperature Under Bias	-55°C to +125°C
Storage Temperature.....	-65°C to +150°C
Voltage on Any Pin with Respect to Ground.....	-2.0V to +7.0V ⁽¹⁾
Voltage on A9 with Respect to Ground	-2.0V to +14.0V ⁽¹⁾
V _{PP} Supply Voltage with Respect to Ground.....	-2.0V to +14.0V ⁽¹⁾

*NOTICE: Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note: 1. Minimum voltage is -0.6V dc which may undershoot to -2.0V for pulses of less than 20 ns. Maximum output pin voltage is V_{CC} + 0.75V dc which may overshoot to +7.0V for pulses of less than 20 ns.

Operating Modes

Mode \ Pin	\overline{CE}	\overline{OE}	A _i	V _{PP}	V _{CC}	Outputs
Read ⁽²⁾	V _{IL}	V _{IL}	A _i	X ⁽¹⁾	V _{CC} ⁽²⁾	DOUT
Output Disable ⁽²⁾	X	V _{IH}	X	X	V _{CC} ⁽²⁾	High Z
Standby ⁽²⁾	V _{IH}	X	X	X ⁽⁵⁾	V _{CC} ⁽²⁾	High Z
Rapid Program ⁽³⁾	V _{IL}	V _{IH}	A _i	V _{PP}	V _{CC} ⁽³⁾	DIN
PGM Verify ⁽³⁾	V _{IH}	V _{IL}	A _i	V _{PP}	V _{CC} ⁽³⁾	DOUT
PGM Inhibit ⁽³⁾	V _{IH}	V _{IH}	X	V _{PP}	V _{CC} ⁽³⁾	High Z
Product Identification ^(3, 5)	V _{IL}	V _{IL}	A ₉ = V _H ⁽⁴⁾ A ₀ = V _{IH} or V _{IL} A ₁ - A ₁₇ = V _{IL}	V _{CC}	V _{CC} ⁽³⁾	Identification Code

Notes: 1. X can be V_{IL} or V_{IH}.
 2. Read, output disable, and standby modes require, 2.7V ≤ V_{CC} ≤ 3.6V, or 4.5V ≤ V_{CC} ≤ 5.5V.
 3. Refer to Programming Characteristics. Programming modes require V_{CC} = 6.5V.

4. V_H = 12.0 ± 0.5V.
 5. Two identifier words may be selected. All A_i inputs are held low (V_{IL}), except A₉ which is set to V_H and A₀ which is toggled low (V_{IL}) to select the Manufacturer's Identification word and high (V_{IH}) to select the Device Code word.

DC and AC Operating Conditions for Read Operation

		AT27BV4096	
		-12	-15
Operating Temperature (Case)	Com.	0°C - 70°C	0°C - 70°C
	Ind.	-40°C - 85°C	-40°C - 85°C
V _{CC} Power Supply		2.7V - 3.6V	2.7V - 3.6V
		5V ± 10%	5V ± 10%

 = Preliminary Information

DC and Operating Characteristics for Read Operation

Symbol	Parameter	Condition	Min	Max	Units
V_{CC} = 2.7V to 3.6V					
I _{LI}	Input Load Current	V _{IN} = 0V to V _{CC}		±1	μA
I _{LO}	Output Leakage Current	V _{OUT} = 0V to V _{CC}		±5	μA
I _{PP1} ⁽²⁾	V _{PP} ⁽¹⁾ Read/Standby Current	V _{PP} = V _{CC}		10	μA
I _{SB}	V _{CC} ⁽¹⁾ Standby Current	I _{SB1} (CMOS), $\overline{CE} = V_{CC} \pm 0.3V$		20	μA
		I _{SB2} (TTL), $\overline{CE} = 2.0$ to V _{CC} + 0.5V		100	μA
I _{CC}	V _{CC} Active Current	f = 5 MHz, I _{OUT} = 0 mA, $\overline{CE} = V_{IL}$, V _{CC} = 3.6V		8	mA
V _{IL}	Input Low Voltage	V _{CC} = 3.0 to 3.6V	-0.6	0.8	V
		V _{CC} = 2.7 to 3.6V	-0.6	0.2 x V _{CC}	V
V _{IH}	Input High Voltage	V _{CC} = 3.0 to 3.6V	2.0	V _{CC} + 0.5	V
		V _{CC} = 2.7 to 3.6V	0.7 x V _{CC}	V _{CC} + 0.5	V
V _{OL}	Output Low Voltage	I _{OL} = 2.0 mA		0.4	V
		I _{OL} = 100 μA		0.2	V
		I _{OL} = 20 μA		0.1	V
V _{OH}	Output High Voltage	I _{OH} = -2.0 mA	2.4		V
		I _{OH} = -100 μA	V _{CC} - 0.2		V
		I _{OH} = -20 μA	V _{CC} - 0.1		V
V_{CC} = 4.5V to 5.5V					
I _{LI}	Input Load Current	V _{IN} = 0V to V _{CC}		±1	μA
I _{LO}	Output Leakage Current	V _{OUT} = 0V to V _{CC}		±5	μA
I _{PP1} ⁽²⁾	V _{PP} ⁽¹⁾ Read/Standby Current	V _{PP} = V _{CC}		10	μA
I _{SB}	V _{CC} ⁽¹⁾ Standby Current	I _{SB1} (CMOS), $\overline{CE} = V_{CC} \pm 0.3V$		100	μA
		I _{SB2} (TTL), $\overline{CE} = 2.0$ to V _{CC} + 0.5V		1	mA
I _{CC}	V _{CC} Active Current	f = 5 MHz, I _{OUT} = 0 mA, $\overline{CE} = V_{IL}$		40	mA
V _{IL}	Input Low Voltage		-0.6	0.8	V
V _{IH}	Input High Voltage		2.0	V _{CC} + 0.5	V
V _{OL}	Output Low Voltage	I _{OL} = 2.1 mA		0.4	V
V _{OH}	Output High Voltage	I _{OH} = -400 μA	2.4		V

Notes: 1. V_{CC} must be applied simultaneously with or before V_{PP}, and removed simultaneously with or after V_{PP}.

2. V_{PP} may be connected directly to V_{CC}, except during programming. The supply current would then be the sum of I_{CC} and I_{PP}.

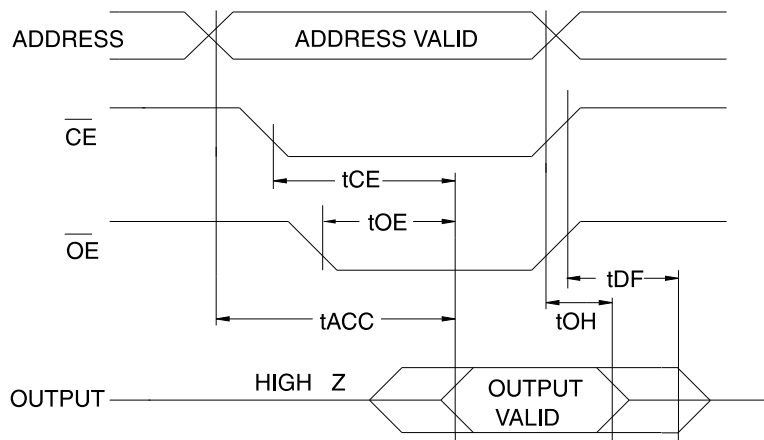
AC Characteristics for Read Operation ($V_{CC} = 2.7V$ to $3.6V$ and $4.5V$ to $5.5V$)

Symbol	Parameter	Condition	AT27BV4096				Units
			-12		-15		
			Min	Max	Min	Max	
t_{ACC} (3)	Address to Output Delay	$\overline{CE} = \overline{OE} = V_{IL}$		120		150	ns
t_{CE} (2)	\overline{CE} to Output Delay	$\overline{OE} = V_{IL}$		120		150	ns
t_{OE} (2, 3)	\overline{OE} to Output Delay	$\overline{CE} = V_{IL}$		35		50	ns
t_{DF} (4, 5)	\overline{OE} or \overline{CE} High to Output Float, whichever occurred first			30		40	ns
t_{OH}	Output Hold from Address, \overline{CE} or \overline{OE} , whichever occurred first		0		0		ns

Notes: 2, 3, 4, 5. - see AC Waveforms for Read Operation.

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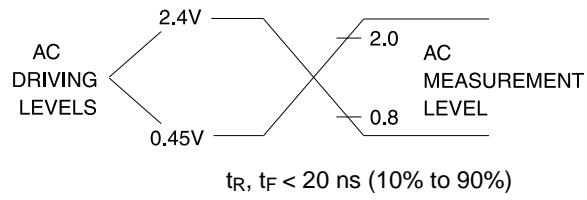
AC Waveforms for Read Operation ⁽¹⁾



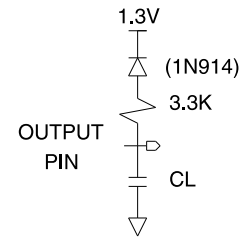
- Notes:
1. Timing measurement references are 0.8V and 2.0V. Input AC drive levels are 0.45V and 2.4V, unless otherwise specified.
 2. \overline{OE} may be delayed up to $t_{CE} - t_{OE}$ after the falling edge of \overline{CE} without impact on t_{CE} .
 3. \overline{OE} may be delayed up to $t_{ACC} - t_{OE}$ after the address is valid without impact on t_{ACC} .

4. This parameter is only sampled and is not 100% tested.
5. Output float is defined as the point when data is no longer driven.
6. When reading a 27BV4096, a 0.1 μF capacitor is required across V_{CC} and ground to suppress spurious voltage transients.

Input Test Waveforms and Measurement Levels



Output Test Load



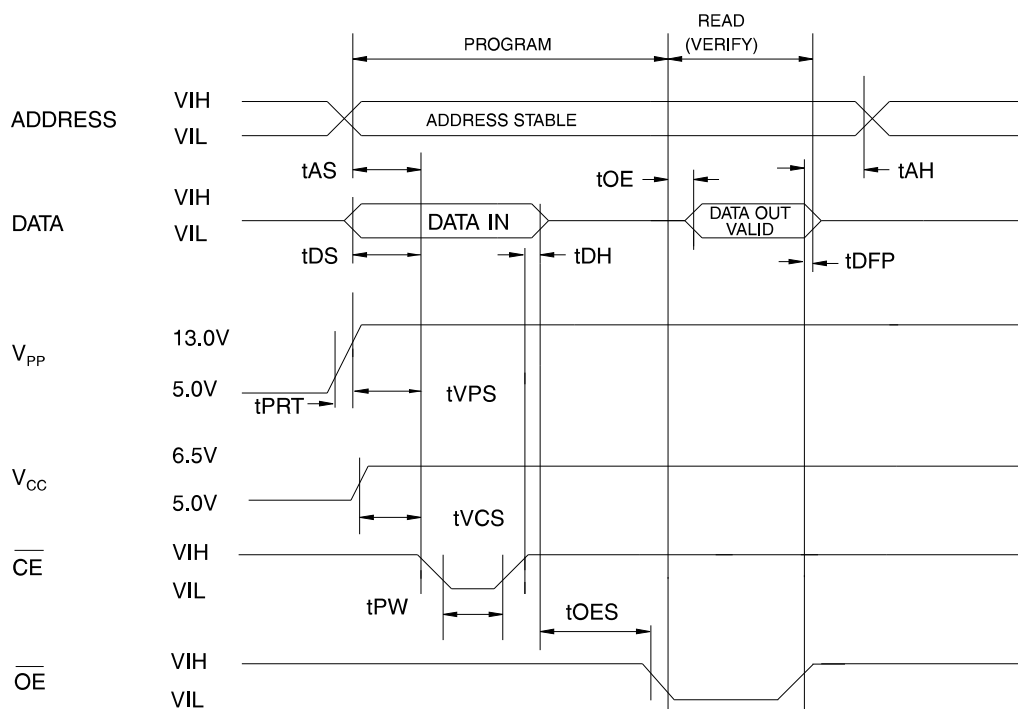
Note: CL = 100 pF including jig capacitance.

Pin Capacitance ($f = 1 \text{ MHz}$ $T = 25^\circ\text{C}$)⁽¹⁾

	Typ	Max	Units	Conditions
C_{IN}	4	10	pF	$V_{IN} = 0V$
C_{OUT}	8	12	pF	$V_{OUT} = 0V$

Note: 1. Typical values for nominal supply voltage. This parameter is only sampled and is not 100% tested.

Programming Waveforms ⁽¹⁾



- Notes: 1. The Input Timing Reference is 0.8V for V_{IL} and 2.0V for V_{IH}.
 2. t_{OE} and t_{DFP} are characteristics of the device but must be accommodated by the programmer.

3. When programming the AT27BV4096 a 0.1 μ F capacitor is required across V_{PP} and ground to suppress spurious voltage transients.

DC Programming Characteristics

TA = 25 \pm 5°C, V_{CC} = 6.5 \pm 0.25V, V_{PP} = 13.0 \pm 0.25V

Symbol	Parameter	Test Conditions	Limits		Units
			Min	Max	
I _{LI}	Input Load Current	V _{IN} = V _{IL} , V _{IH}		± 10	μ A
V _{IL}	Input Low Level		-0.6	0.8	V
V _{IH}	Input High Level		2.0	V _{CC} + 0.1	V
V _{OL}	Output Low Voltage	I _{OL} = 2.1 mA		0.4	V
V _{OH}	Output High Voltage	I _{OH} = -400 μ A	2.4		V
I _{CC2}	V _{CC} Supply Current (Program and Verify)			50	mA
I _{PP2}	V _{PP} Supply Current	\overline{CE} = V _{IL}		30	mA
V _{ID}	A9 Product Identification Voltage		11.5	12.5	V

AC Programming Characteristics

TA = 25 ± 5°C, VCC = 6.5 ± 0.25V, VPP = 13.0 ± 0.25V

Sym- bol	Test Parameter	Test Conditions* (1)	Limits		Units
			Min	Max	
tAS	Address Setup Time		2		μs
tCES	$\overline{\text{CE}}$ Setup Time		2		μs
tOES	$\overline{\text{OE}}$ Setup Time		2		μs
tDS	Data Setup Time		2		μs
tAH	Address Hold Time		0		μs
tDH	Data Hold Time		2		μs
tDFP	$\overline{\text{OE}}$ High to Out-put Float Delay (2)		0	130	ns
tVPS	VPP Setup Time		2		μs
tVCS	VCC Setup Time		2		μs
tPW	PGM Program Pulse Width (3)		47.5	52.5	μs
tOE	Data Valid from $\overline{\text{OE}}$			150	ns
tPRT	VPP Pulse Rise Time During Programming		50		ns

*AC Conditions of Test:

Input Rise and Fall Times (10% to 90%).....20 ns
 Input Pulse Levels..... 0.45V to 2.4V
 Input Timing Reference Level0.8V to 2.0V
 Output Timing Reference Level0.8V to 2.0V

- Notes: 1. VCC must be applied simultaneously or before VPP and removed simultaneously or after VPP.
 2. This parameter is only sampled and is not 100% tested. Output Float is defined as the point where data is no longer driven — see timing diagram.
 3. Program Pulse width tolerance is 50 μsec ± 5%.

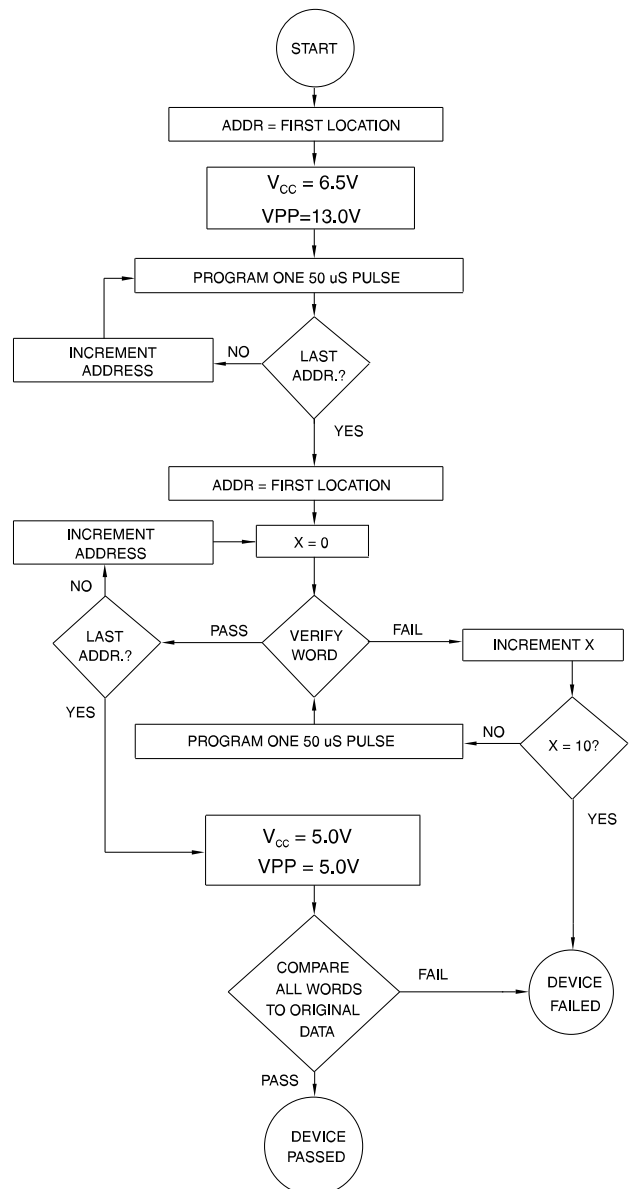
Atmel's 27BV4096 Integrated Product Identification Code (1)

Codes	Pins										Hex Data
	A0	015-08	O7	O6	O5	O4	O3	O2	O1	O0	
Manufacturer	0	0	0	0	0	1	1	1	1	0	001E
Device Type	1	0	1	1	1	1	0	1	0	0	00F4

- Note: 1. The AT27BV4096 has the same Product Identification Code as the AT27C4096. Both are programming compatible.

Rapid Programming Algorithm

A 50 μs $\overline{\text{CE}}$ pulse width is used to program. The address is set to the first location. VCC is raised to 6.5V and VPP is raised to 13.0V. Each address is first programmed with one 50 μs $\overline{\text{CE}}$ pulse without verification. Then a verification / reprogramming loop is executed for each address. In the event a word fails to pass verification, up to 10 successive 50 μs pulses are applied with a verification after each pulse. If the word fails to verify after 10 pulses have been applied, the part is considered failed. After the word verifies properly, the next address is selected until all have been checked. VPP is then lowered to 5.0V and VCC to 5.0V. All words are read again and compared with the original data to determine if the device passes or fails.



Ordering Information

t _{ACC} (ns)	I _{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
120	8	0.02	AT27BV4096-12JC AT27BV4096-12VC	44J 40V	Commercial (0°C to 70°C)
	8	0.02	AT27BV4096-12JI AT27BV4096-12VI	44J 40V	Industrial (-40°C to 85°C)
150	8	0.02	AT27BV4096-15JC AT27BV4096-15VC	44J 40V	Commercial (0°C to 70°C)
	8	0.02	AT27BV4096-15JI AT27BV4096-15VI	44J 40V	Industrial (-40°C to 85°C)

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Package Type	
44J	44 Lead, Plastic J-Leaded Chip Carrier (PLCC)
40V	40 Lead, Plastic Thin Small Outline Package (TSOP) 10 x 14 mm

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