



Description

The ATF20V8B is a high performance CMOS (Electrically Erasable) Programmable Logic Device (PLD) which utilizes Atmel's proven electrically erasable Flash memory technology. Speeds down to 7.5 ns and power dissipation as low as 10 mA are offered. All speed ranges are specified over the full $5V \pm 10\%$ range for industrial temperature ranges, and $5V \pm 5\%$ for commercial temperature ranges.

Several low power options allow selection of the best solution for various types of power-limited applications. Each of

these options significantly reduces total system power and enhances system reliability.

The ATF20V8Bs incorporate a superset of the generic architectures, which allows direct replacement of the 20R8 family and most 24-pin combinatorial PLDs. Eight outputs are each allocated eight product terms. Three different modes of operation, configured automatically with software, allow highly complex logic functions to be realized.

Absolute Maximum Ratings*

Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin with Respect to Ground	-2.0V to +7.0V ⁽¹⁾
Voltage on Input Pins with Respect to Ground During Programming.....	-2.0V to +14.0V ⁽¹⁾
Programming Voltage with Respect to Ground	-2.0V to +14.0V ⁽¹⁾

***NOTICE:** Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note: 1. Minimum voltage is -0.6V DC which may undershoot to -2.0V for pulses of less than 20 ns. Maximum output pin voltage is $V_{CC} + 0.75V$ DC which may overshoot to 7.0V for pulses of less than 20 ns.

DC and AC Operating Conditions

	Commercial	Industrial
Operating Temperature (Case)	0°C - 70°C	-40°C - 85°C
V_{CC} Power Supply	$5V \pm 5\%$	$5V \pm 10\%$

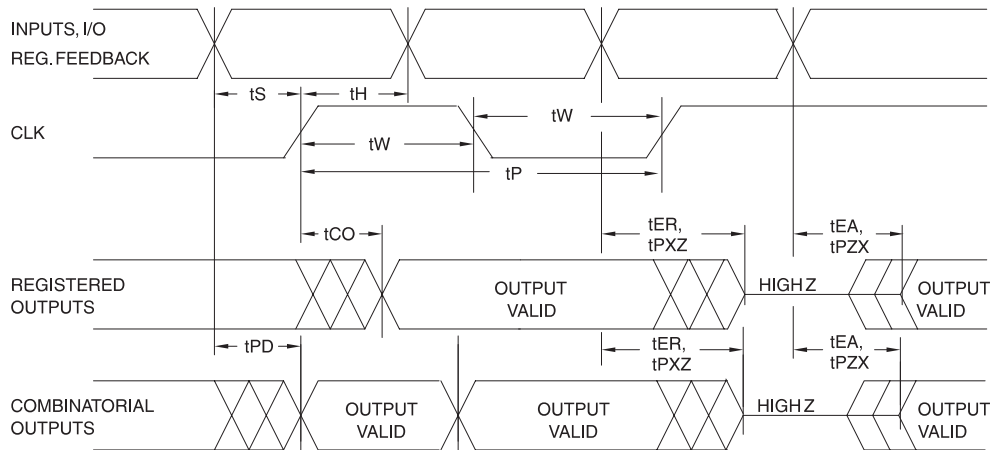
DC Characteristics

Symbol	Parameter	Condition		Min	Typ	Max	Units	
I_{IL}	Input or I/O Low Leakage Current	$0 \leq V_{IN} \leq V_{IL}(MAX)$			-35	-100	μA	
I_{IH}	Input or I/O High Leakage Current	$3.5 \leq V_{IN} \leq V_{CC}$				10	μA	
I_{CC}	Power Supply Current, Standby	$V_{CC} = MAX,$ $V_{IN} = MAX,$ Outputs Open	B-7, -10	Com.		60	90	mA
				Ind.		60	100	mA
			B-15, -25	Com.		60	80	mA
				Ind.		60	90	mA
			BQ-10	Com.		35	55	mA
			BQL-15, -25	Com.		5	10	mA
Ind.		5		15	mA			
I_{CC2}	Clocked Power Supply Current	$V_{CC} = MAX,$ Outputs Open, $f = 15 \text{ MHz}$	B-7, -10	Com.		80	110	mA
				Ind.		80	125	mA
			B-15, -25	Com.		60	90	mA
				Ind.		60	105	mA
			BQ-10	Com.		40	55	mA
			BQL-15, -25	Com.		20	35	mA
Ind.		20		40	mA			
$I_{OS}^{(1)}$	Output Short Circuit Current	$V_{OUT} = 0.5V$				-130	mA	
V_{IL}	Input Low Voltage			-0.5		0.8	V	
V_{IH}	Input High Voltage			2.0		$V_{CC} + 0.75$	V	
V_{OL}	Output Low Voltage	$V_{IN} = V_{IH} \text{ or } V_{IL},$ $V_{CC} = MIN$	$I_{OL} = 24 \text{ mA}$	Com., Ind.		0.5	V	
			$I_{OL} = 16 \text{ mA}$			0.5	V	
V_{OH}	Output High Voltage	$V_{IN} = V_{IH} \text{ or } V_{IL},$ $V_{CC} = MIN$	$I_{OH} = -4.0 \text{ mA}$		2.4		V	

Note: 1. Not more than one output at a time should be shorted. Duration of short circuit test should not exceed 30 sec.



AC Waveforms⁽¹⁾



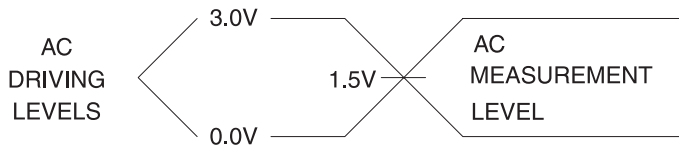
Note: 1. Timing measurement reference is 1.5V. Input AC driving levels are 0.0V and 3.0V, unless otherwise specified.

AC Characteristics⁽¹⁾

Symbol	Parameter	-7		-10		-15		-25		Units		
		Min	Max	Min	Max	Min	Max	Min	Max			
t_{PD}	Input or Feedback to Non-Registered Output	8 outputs switching		3	7.5	3	10	3	15	3	25	ns
		1 output switching			7							ns
t_{CF}	Clock to Feedback		3		6		8		10		ns	
t_{CO}	Clock to Output	2	5	2	7	2	10	2	12		ns	
t_S	Input or Feedback Setup Time	5		7.5		12		15			ns	
t_H	Hold Time	0		0		0		0			ns	
t_P	Clock Period	8		12		16		24			ns	
t_W	Clock Width	4		6		8		12			ns	
F_{MAX}	External Feedback $1/(t_S + t_{CO})$		100		68		45		37		MHz	
	Internal Feedback $1/(t_S + t_{CF})$		125		74		50		40		MHz	
	No Feedback $1/(t_P)$		125		83		62		41		MHz	
t_{EA}	Input to Output Enable — Product Term	3	9	3	10	3	15	3	20		ns	
t_{ER}	Input to Output Disable — Product Term	2	9	2	10	2	15	2	20		ns	
t_{PZX}	\overline{OE} pin to Output Enable	2	6	2	10	2	15	2	20		ns	
t_{PXZ}	\overline{OE} pin to Output Disable	1.5	6	1.5	10	1.5	15	1.5	20		ns	

Note: 1. See ordering information for valid part numbers and speed grades.

Input Test Waveforms and Measurement Levels



$t_R, t_F < 5 \text{ ns}$ (10% to 90%)

Pin Capacitance

$f = 1 \text{ MHz}, T = 25^\circ\text{C}^{(1)}$

	Typ	Max	Units	Conditions
C_{IN}	5	8	pF	$V_{IN} = 0V$
C_{OUT}	6	8	pF	$V_{OUT} = 0V$

Note: 1. Typical values for nominal supply voltage. This parameter is only sampled and is not 100% tested.

Power Up Reset

The registers in the ATF20V8Bs are designed to reset during power up. At a point delayed slightly from V_{CC} crossing V_{RST} , all registers will be reset to the low state. As a result, the registered output state will always be high on power-up.

This feature is critical for state machine initialization. However, due to the asynchronous nature of reset and the uncertainty of how V_{CC} actually rises in the system, the following conditions are required:

1. The V_{CC} rise must be monotonic,
2. After reset occurs, all input and feedback setup times must be met before driving the clock pin high, and
3. The clock must remain stable during t_{PR} .

Preload of Registered Outputs

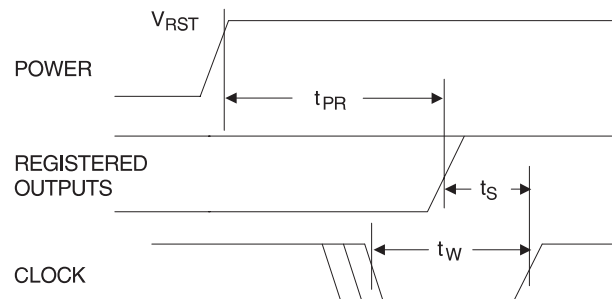
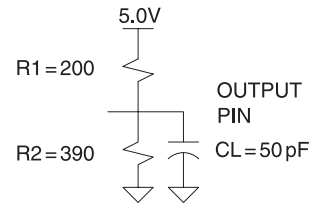
The ATF16V8B's registers are provided with circuitry to allow loading of each register with either a high or a low. This feature will simplify testing since any state can be forced into the registers to control test sequencing. A JEDEC file with preload is generated when a source file with vectors is compiled. Once downloaded, the JEDEC file preload sequence will be done automatically by most of the approved programmers after the programming.

Electronic Signature Word

There are 64 bits of programmable memory that are always available to the user, even if the device is secured. These bits can be used for user-specific data.

Output Test Loads

Commercial



Parameter	Description	Typ	Max	Units
t_{PR}	Power-Up Reset Time	600	1,000	ns
V_{RST}	Power-Up Reset Voltage	3.8	4.5	V

Security Fuse Usage

A single fuse is provided to prevent unauthorized copying of the ATF20V8B fuse patterns. Once programmed, fuse verify and preload are inhibited. However, the 64-bit User Signature remains accessible.

The security fuse should be programmed last, as its effect is immediate.

Programming/Erasing

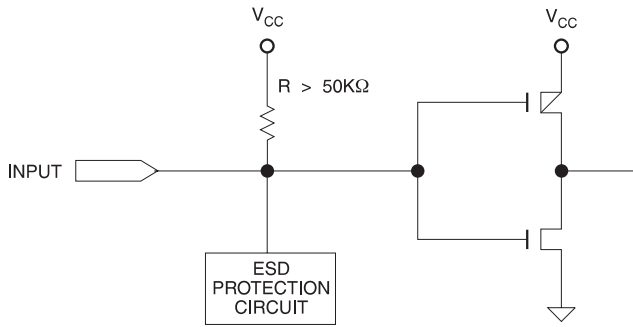
Programming/erasing is performed using standard PLD programmers. For further information, see the Configurable Logic Databook, section titled, "CMOS PLD Programming Hardware and Software Support."

Input and I/O Pull-Ups

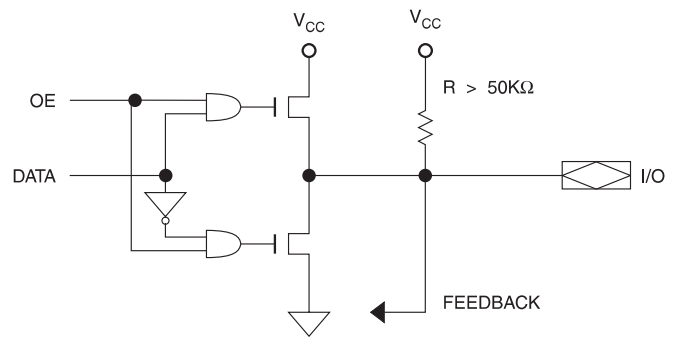
All ATF20V8B family members have internal input and I/O pull-up resistors. Therefore, whenever inputs or I/Os are not being driven externally, they will float to V_{CC} . This ensures that all logic array inputs are at known states.

These are relatively weak active pull-ups that can easily be overdriven by TTL-compatible drivers (see input and I/O diagrams below).

Input Diagram



I/O Diagram



Functional Logic Diagram Description

The Logic Option and Functional Diagrams describe the ATF20V8B architecture. Eight configurable macrocells can be configured as a registered output, combinatorial I/O, combinatorial output, or dedicated input.

The ATF20V8B can be configured in one of three different modes. Each mode makes the ATF20V8B look like a different device. Most PLD compilers can choose the right mode automatically. The user can also force the selection by supplying the compiler with a mode selection. The determining factors would be the usage of register versus combinatorial outputs and dedicated outputs versus outputs with output enable control.

The ATF20V8B universal architecture can be programmed to emulate many 24-pin PAL devices. These architectural

subsets can be found in each of the configuration modes described in the following pages. The user can download the listed subset device JEDEC programming file to the PLD programmer, and the ATF20V8B can be configured to act like the chosen device. Check with your programmer manufacturer for this capability.

Unused product terms are automatically disabled by the compiler to decrease power consumption. A Security Fuse, when programmed, protects the content of the ATF20V8B. Eight bytes (64 fuses) of User Signature are accessible to the user for purposes such as storing project name, part number, revision, or date. The User Signature is accessible regardless of the state of the Security Fuse.

Compiler Mode Selection

	Registered	Complex	Simple	Auto Select
ABEL, Atmel-ABEL	P20V8R	P20V8C	P20V8	P20V8
CUPL	G20V8MS	G20V8MA	G20V8	G20V8A
LOG/iC	GAL20V8_R ⁽¹⁾	GAL20V8_C7 ⁽¹⁾	GAL20V8_C8 ⁽¹⁾	GAL20V8
OrCAD-PLD	"Registered"	"Complex"	"Simple"	GAL20V8
PLDesigner	P20V8	P20V8	P20V8	P20V8
Tango-PLD	G20V8	G20V8	G20V8	G20V8

Note: 1. Only applicable for version 3.4 or lower.

ATF20V8B Registered Mode

PAL Device Emulation / PAL Replacement

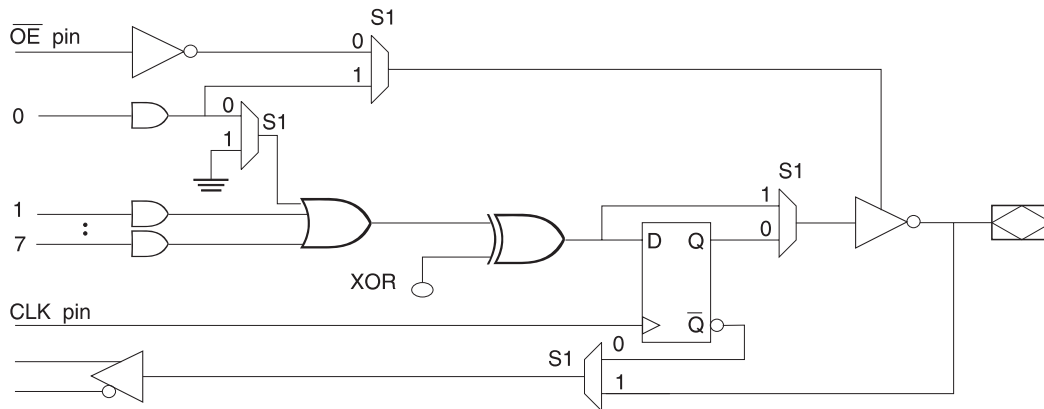
The registered mode is used if one or more registers are required. Each macrocell can be configured as either a registered or combinatorial output or I/O, or as an input. For a registered output or I/O, the output is enabled by the \overline{OE} pin, and the register is clocked by the CLK pin. Eight product terms are allocated to the sum term. For a combinatorial output or I/O, the output enable is controlled by a product term, and seven product terms are allocated to the

sum term. When the macrocell is configured as an input, the output enable is permanently disabled.

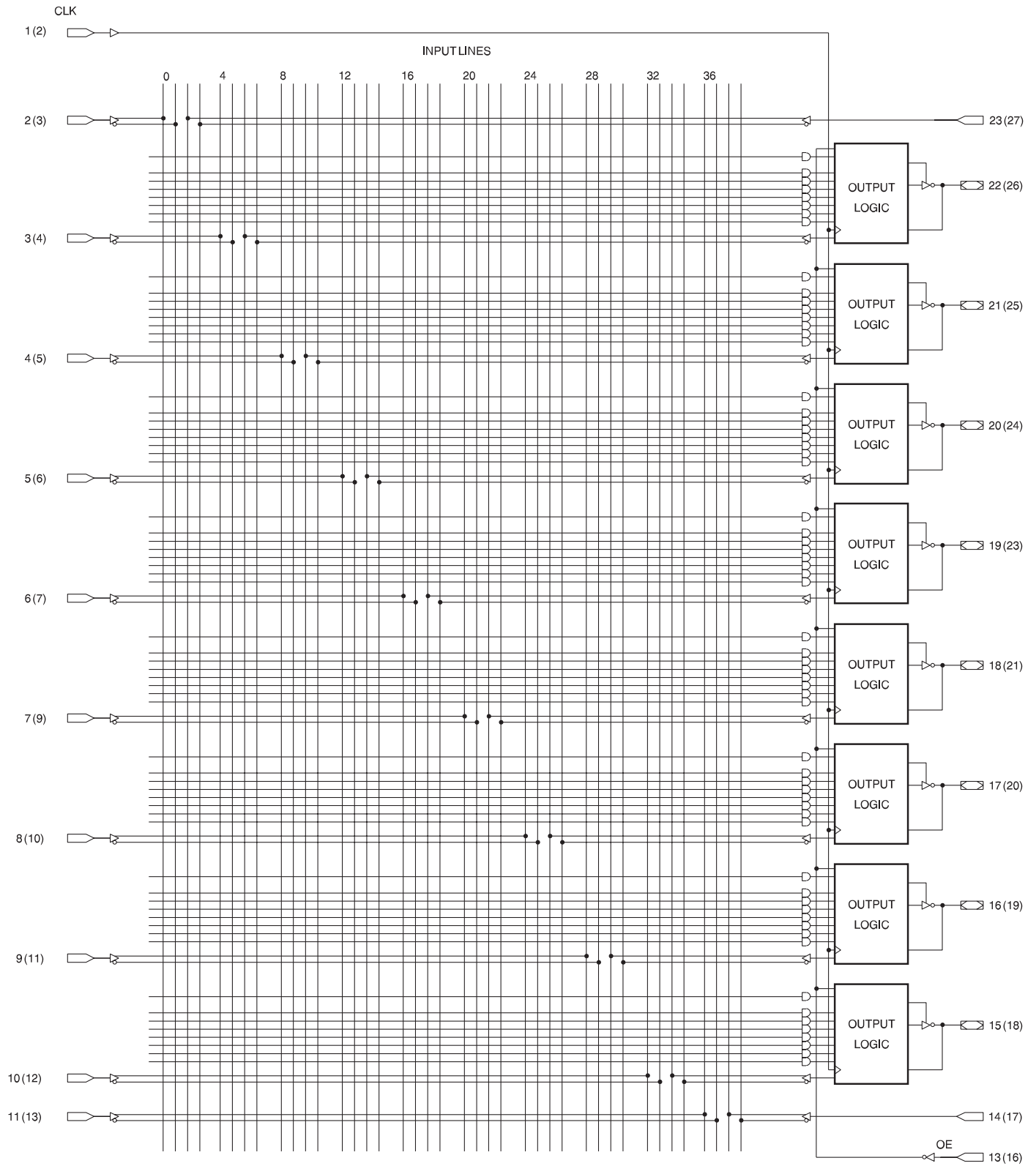
Any register usage will make the compiler select this mode. The following registered devices can be emulated using this mode:

20R8 20RP8
 20R6 20RP6
 20R4 20RP4

Registered Mode Operation



Registered Mode Logic Diagram



ATF20V8B Complex Mode

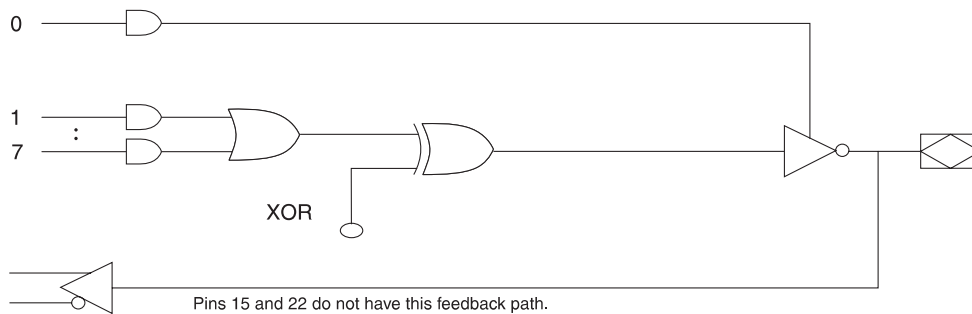
PAL Device Emulation/PAL Replacement

In the Complex Mode, combinatorial output and I/O functions are possible. Pins 1 and 11 are regular inputs to the array. Pins 13 through 18 have pin feedback paths back to the AND-array, which makes full I/O capability possible. Pins 12 and 19 (outermost macrocells) are outputs only. They do not have input capability. In this mode, each macrocell has seven product terms going to the sum term and one product term enabling the output.

Combinatorial applications with an OE requirement will make the compiler select this mode. The following devices can be emulated using this mode:

20L8
20H8
20P8

Complex Mode Operation



ATF20V8B Simple Mode

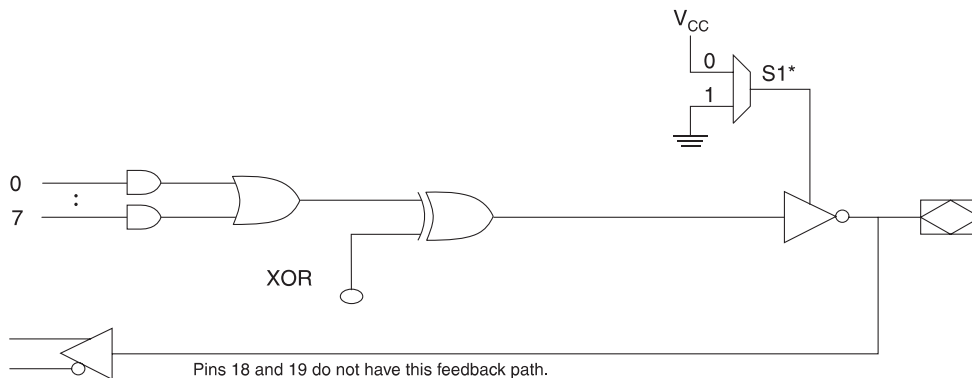
PAL Device Emulation / PAL Replacement

In the Simple Mode, 8 product terms are allocated to the sum term. Pins 15 and 16 (center macrocells) are permanently configured as combinatorial outputs. Other macrocells can be either inputs or combinatorial outputs with pin feedback to the AND-array. Pins 1 and 11 are regular inputs.

The compiler selects this mode when all outputs are combinatorial without OE control. The following simple PALs can be emulated using this mode:

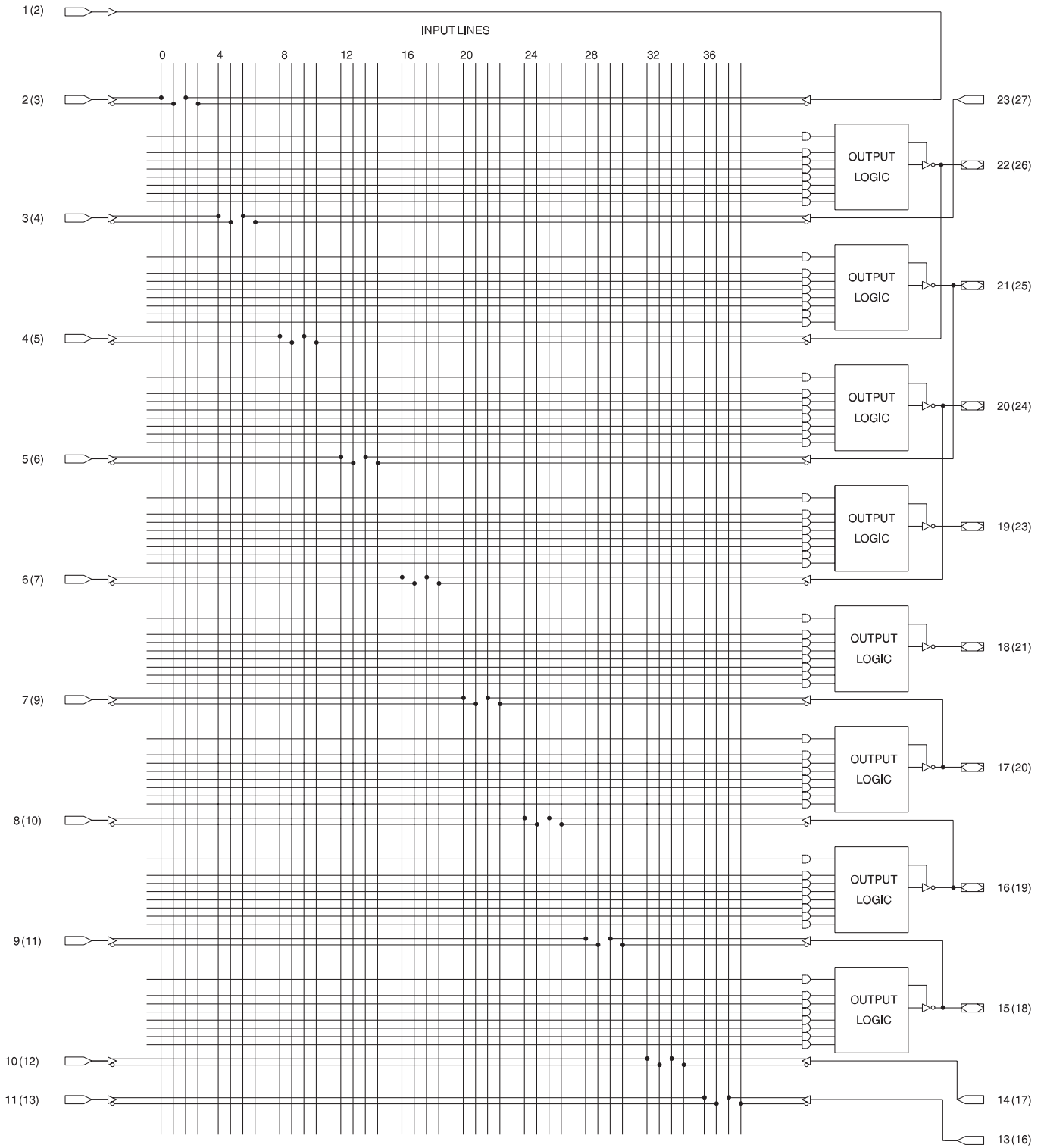
14L8 14H8 14P8
16L6 18H6 16P6
18L4 18H4 18P4
20L2 20H2 20P2

Simple Mode Option

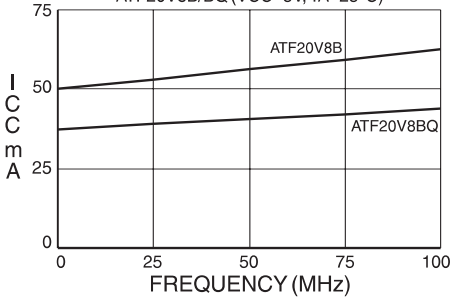


* - Pins 18 and 19 are always enabled.

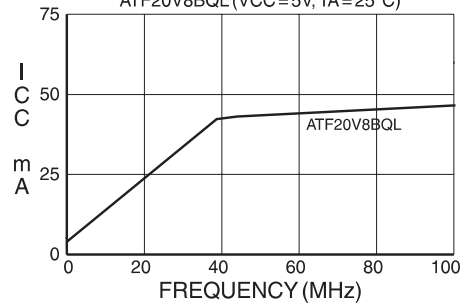
Simple Mode Logic Diagram



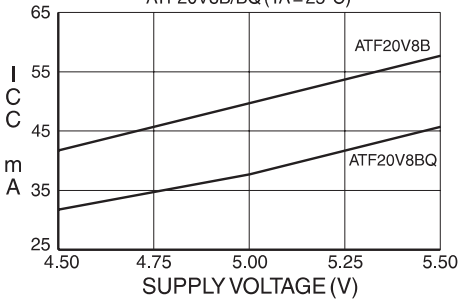
SUPPLY CURRENT vs. INPUT FREQUENCY
ATF20V8B/BQ (VCC=5V, TA=25°C)



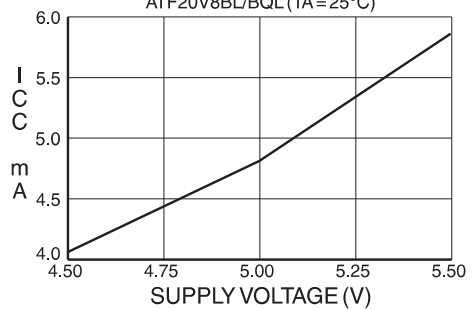
SUPPLY CURRENT vs. INPUT FREQUENCY
ATF20V8BQL (VCC=5V, TA=25°C)



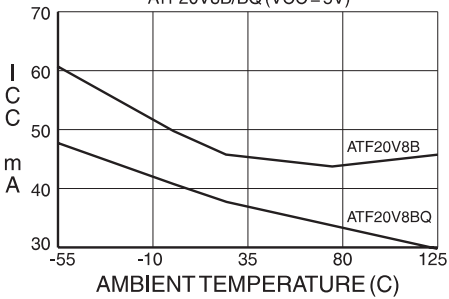
SUPPLY CURRENT vs. SUPPLY VOLTAGE
ATF20V8B/BQ (TA=25°C)



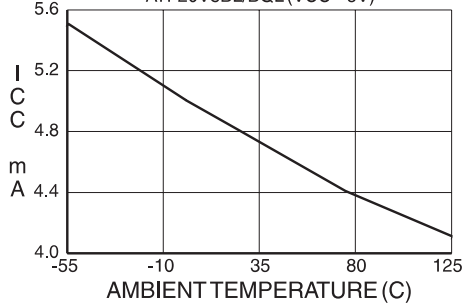
SUPPLY CURRENT vs. SUPPLY VOLTAGE
ATF20V8BL/BQL (TA=25°C)



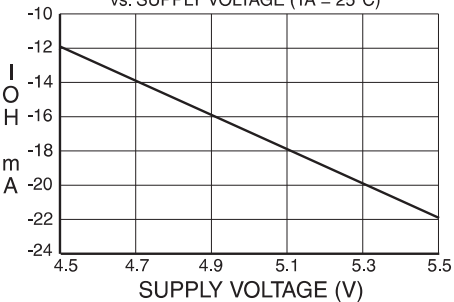
SUPPLY CURRENT vs. AMBIENT TEMPERATURE
ATF20V8B/BQ (VCC=5V)



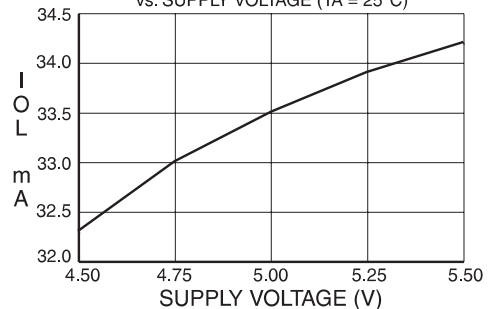
SUPPLY CURRENT vs. AMBIENT TEMPERATURE
ATF20V8BL/BQL (VCC=5V)

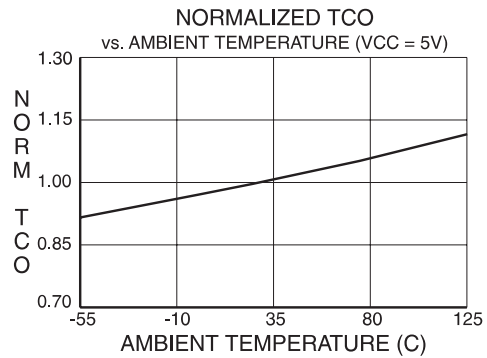
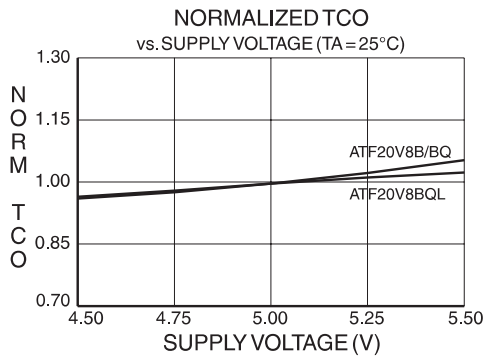
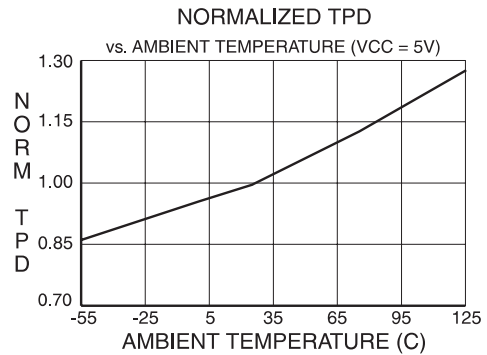
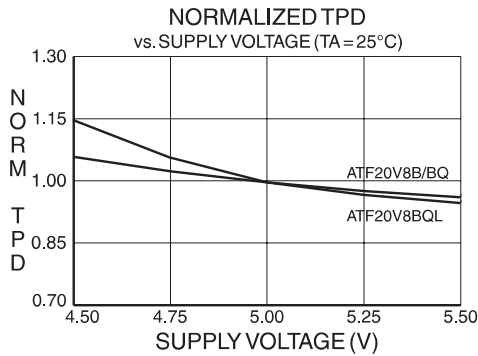
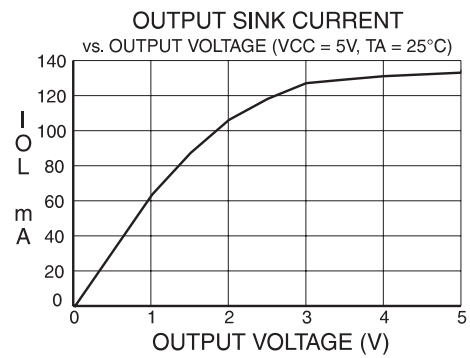
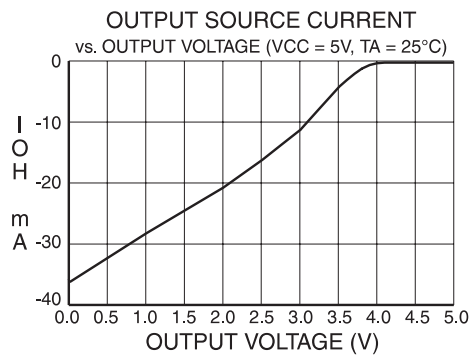
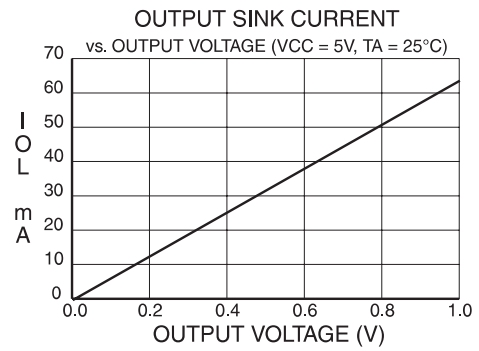
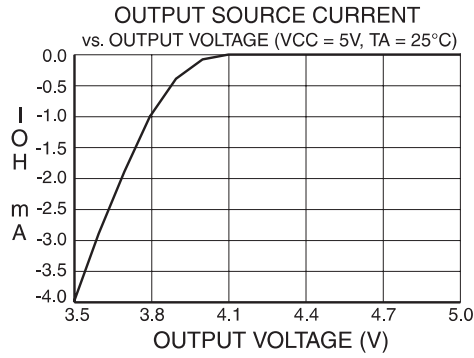


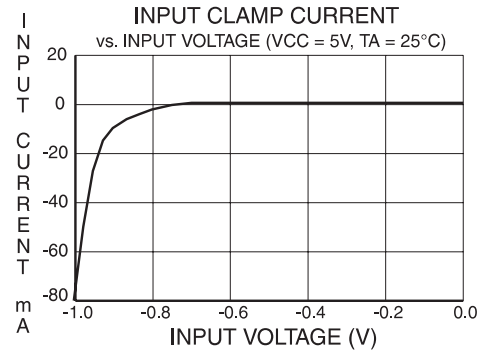
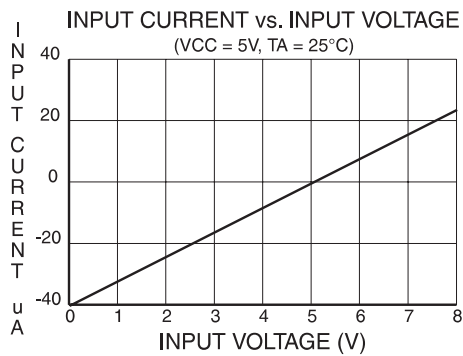
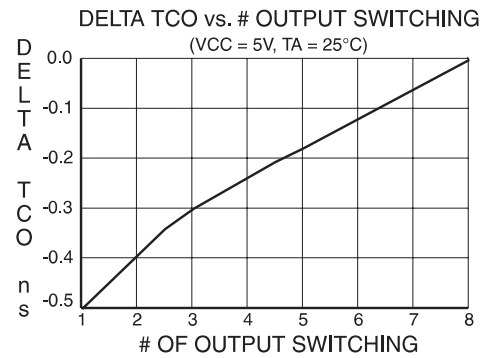
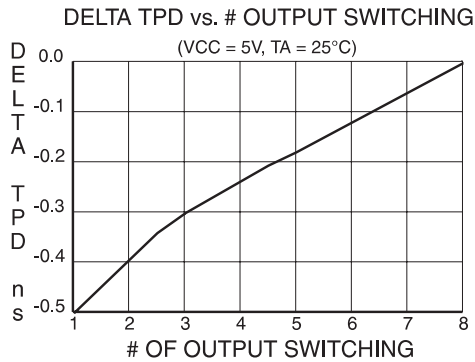
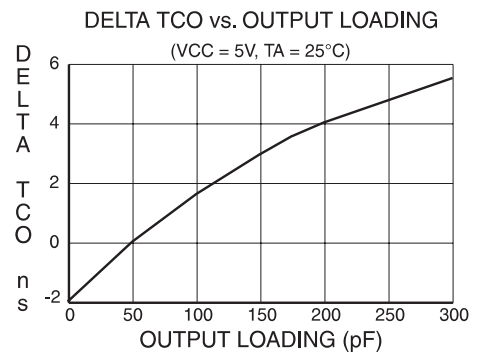
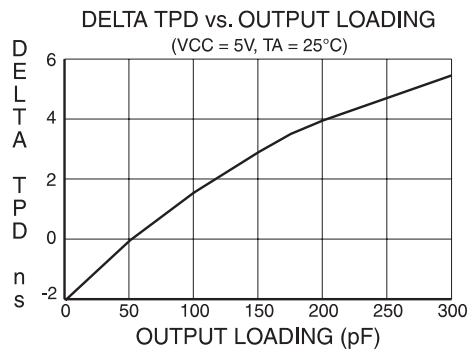
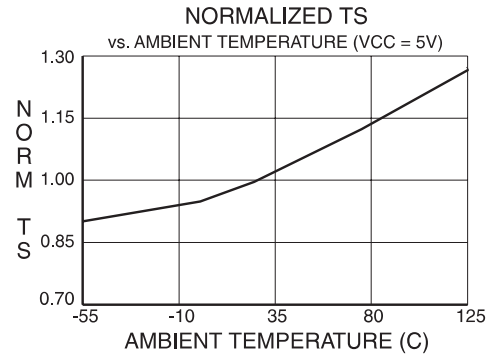
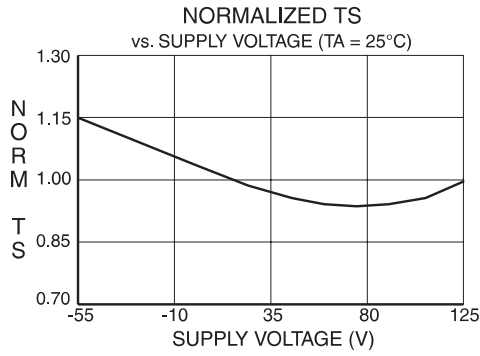
OUTPUT SOURCE CURRENT
vs. SUPPLY VOLTAGE (TA = 25°C)



OUTPUT SINK CURRENT
vs. SUPPLY VOLTAGE (TA = 25°C)







Ordering Information

t_{PD} (ns)	t_s (ns)	t_{CO} (ns)	Ordering Code	Package	Operation Range		
7.5	5	5	ATF20V8B-7JC	28J	Commercial (0°C to 70°C)		
			ATF20V8B-7PC	24P3			
			ATF20V8B-7SC	24S			
			ATF20V8B-7XC	24X			
10	7.5	7	ATF20V8B-10JC	28J	Commercial (0°C to 70°C)		
			ATF20V8B-10PC	24P3			
			ATF20V8B-10SC	24S			
			ATF20V8B-10XC	24X			
					ATF20V8B-10JI	28J	Industrial (-40°C to 85°C)
					ATF20V8B-10PI	24P3	
					ATF20V8B-10SI	24S	
					ATF20V8B-10XI	24X	
15	12	10	ATF20V8B-15JC	28J	Commercial (0°C to 70°C)		
			ATF20V8B-15PC	24P3			
			ATF20V8B-15SC	24S			
			ATF20V8B-15XC	24X			
					ATF20V8B-15JI	28J	Industrial (-40°C to 85°C)
					ATF20V8B-15PI	24P3	
					ATF20V8B-15SI	24S	
					ATF20V8B-15XI	24X	
25	15	12	ATF20V8B-25JC	28J	Commercial (0°C to 70°C)		
			ATF20V8B-25PC	24P3			
			ATF20V8B-25SC	24S			
			ATF20V8B-25XC	24X			
					ATF20V8B-25JI	28J	Industrial (-40°C to 85°C)
					ATF20V8B-25PI	24P3	
					ATF20V8B-25SI	24S	
					ATF20V8B-25XI	24X	

(continued)

Package Type	
28J	28-Lead, Plastic J-Leaded Chip Carrier (PLCC)
24P3	24-Lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)
24S	24-Lead, 0.300" Wide, Plastic Gull Wing Small Outline (SOIC)
24X	24-Lead, 4.4 mm Wide, Plastic Thin Shrink Small Outline (TSSOP)



Ordering Information

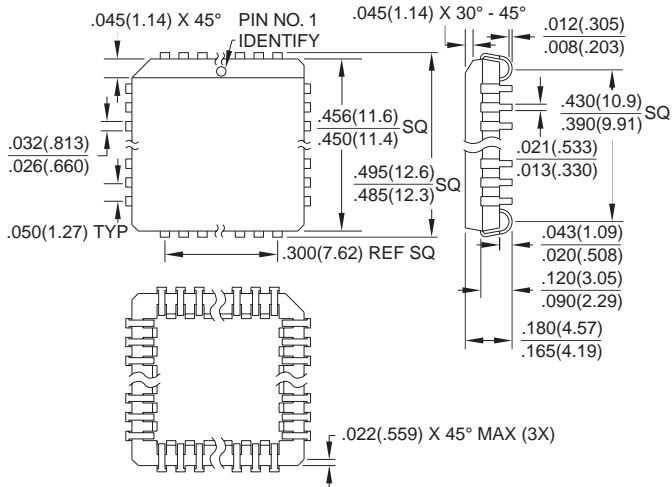
t_{PD} (ns)	t_S (ns)	t_{CO} (ns)	Ordering Code	Package	Operation Range
10	7.5	7	ATF20V8BQ-10JC	28J	Commercial (0°C to 70°C)
			ATF20V8BQ-10PC	24P3	
			ATF20V8BQ-10XC	24X	
15	12	10	ATF20V8BQL-15JC	28J	Commercial (0°C to 70°C)
			ATF20V8BQL-15PC	24P3	
			ATF20V8BQL-15SC	24S	
			ATF20V8BQL-15XC	24X	
25	15	12	ATF20V8BQL-25JC	28J	Commercial (0°C to 70°C)
			ATF20V8BQL-25PC	24P3	
			ATF20V8BQL-25SC	24S	
			ATF20V8BQL-25XC	24X	
		12	ATF20V8BQL-25JI	28J	Industrial (-40°C to 85°C)
			ATF20V8BQL-25PI	24P3	
			ATF20V8BQL-25SI	24S	
			ATF20V8BQL-25XI	24X	

Package Type

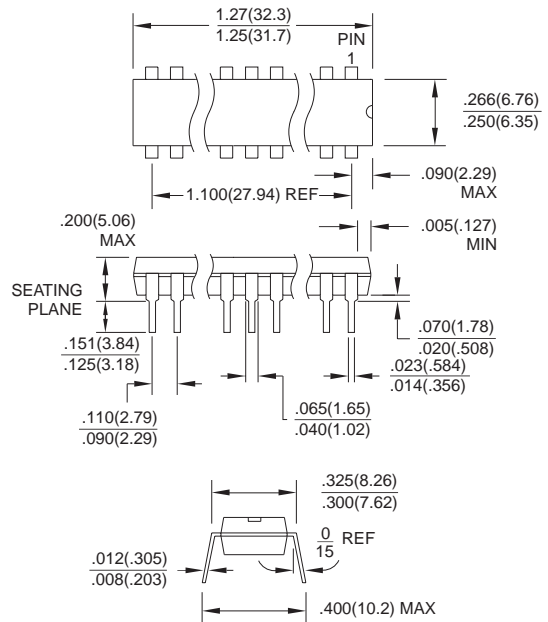
28J	28-Lead, Plastic J-Leaded Chip Carrier (PLCC)
24P3	24-Lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)
24S	24-Lead, 0.300" Wide, Plastic Gull Wing Small Outline (SOIC)
24X	24-Lead, 4.4 mm Wide, Plastic Thin Shrink Small Outline (TSSOP)

Packaging Information

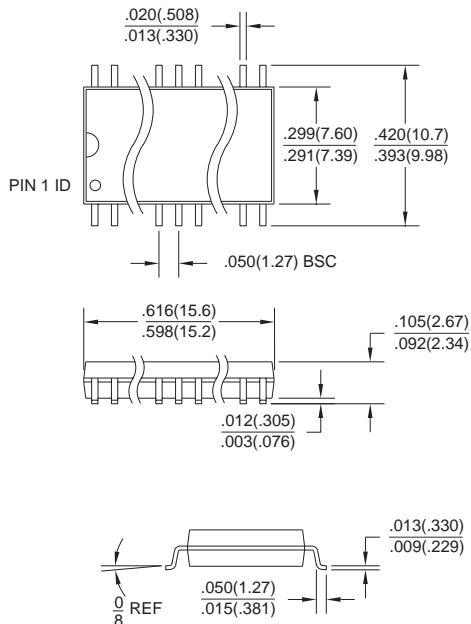
28J, 28-Lead, Plastic J-Leaded Chip Carrier (PLCC)
 Dimensions in Inches and (Millimeters)
 JEDEC STANDARD MS-018 AB



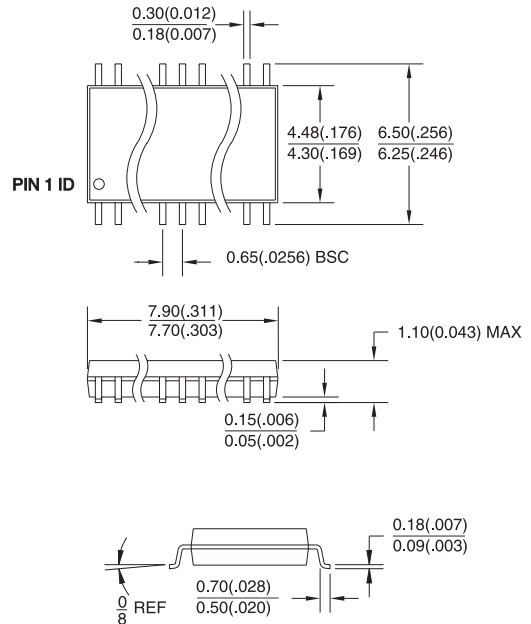
24P3, 24-Lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)
 Dimensions in Inches and (Millimeters)
 JEDEC STANDARD MS-001 AF



24S, 24-Lead, 0.300" Wide, Plastic Gull Wing Small Outline (SOIC)
 Dimensions in Inches and (Millimeters)



24X, 24-Lead, 4.4 mm Wide, Plastic Thin Shrink Small Outline (TSSOP)
 Dimensions in Millimeters and (Inches)



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