

**FEATURES**

- High Output Intercept Point
- High Linearity
- True Surface Mount Package
- Internal Bias Circuit Requiring Nominal Input Voltages  $\pm 10\%$
- Low Cost
- Off Chip Output Matching Circuit Allows Application Optimization

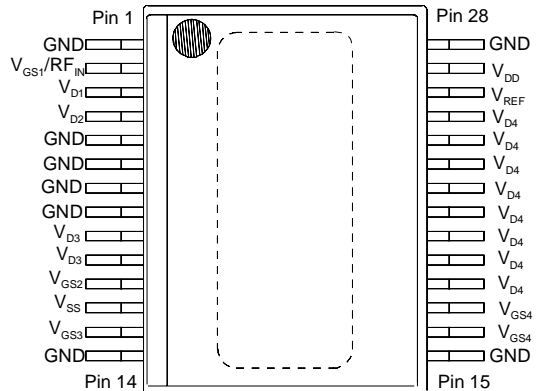
**PRODUCT DESCRIPTION**

The AWT1921 is a four stage monolithic amplifier for use in communication systems that require high gain and output intercept point. The device has been specifically designed for fixed satellite access equipment and handset booster amplifier applications.



**Table 1: Pin Description**

PIN	NAME	DESCRIPTION
1,14,1-5,28, slug	GND	AC and RF Ground
2	$V_{GS1}$ & $RF_{IN}$	First Stage Gate terminal & RF Input
27	$V_{DD}$	Positive Supply of Bias Circuit(+5V)
4	$V_{D2}$	Second Stage drain supply (+9V)
3	$V_{D1}$	First Stage drain supply (+9V)
5,6,7,8	GND	First and Second Stage Source ground
9,10	$V_{D3}$	Third Stage drain supply (+9V)
11	$V_{GS2}$	Second Stage Gate Terminal
26	$V_{REF}$	Bias control Pin (+5V)
12	$V_{SS}$	Negative Supply for Bias Circuit (-5V)
13	$V_{GS3}$	Third Stage Gate terminal
16,17	$V_{GS4}$	Fourth Stage Gate terminal
18-25	$V_{D4}$	Fourth Stage drain supply (+9V) & RF out



**Figure 1: Pin Layout**

## ELECTRICAL CHARACTERISTICS

Table 2: Electrical Specifications<sup>(1)</sup>

(Pin with CDMA modulation,  $f_o = 1610 - 1626.5$  MHz,  $V_{DS1} = V_{DS2} = V_{DS3} = V_{DS4} = 9.0V$ ,  $V_{SS} = -5V$ ,  $V_{REF} = +5V$ ,  $V_{DD} = +5V$ ,  $T_c = 25C$ ,  $50 \Omega$  System<sup>(2)</sup>)

PARAMETER	MIN	TYP	MAX	UNIT
Frequency	1610		1626.5	MHz
Power Output	35	36		dBm
Power Added Efficiency	-	25		%
Gain <sup>(3)</sup>	27	30		dB
ACPR <sup>(3)</sup> 0.730 MHz 1.23 MHz	- -	25 -28	100	dBc
Harmonics 2nd 3rd 4th	- - -	-45 -52 -45		dBc
Stability: - 60 dBc all spurious outputs relative to desired signal	-	-	3:1	VSWR load, all phase angles
Bias Supply Currents $I_{SS}$ $I_{REF}$ $I_{DD}$	- - -	15 5 15		mA
Quiescent Currents $I_{DQ1}$ $I_{DQ2}$ $I_{DQ3}$ $I_{DQ4}$	- - - -	60 90 150 200	- - -	mA
Input Return Loss	-	11	-	dB
Gain Flatness <sup>(3)</sup> @ $P_{OUT} = +35$ dBm	-	0.8	-	dB
Thermal Resistance <sup>(4)</sup>	-	4.5	-	C/W

## Notes:

- As measured in ANADIGICS test fixture, see application section.
- $50\Omega$  Measurement system after off chip matching circuit, input terminated in  $50\Omega$ .
- Measured at  $P_{OUT} = +35$  dBm
- Thermal Resistance for junction to bottom of slug

$$\Theta_{jc} = \frac{T_j - T_c}{(I_{D1} + I_{D2} + I_{D3} + I_{D4})V_{SUP} - P_{OUT}}$$

Table 3: Absolute Max Ratings

PIN	NAME	MAX RATING	PIN	NAME	MAX RATING
2	$V_{DD}$	+7VDC	11	$V_{REF}$	+7 VDC
3	$RF_{IN}$	+20 dBm	12	$V_{SS}$	-7 VDC
4,5	$V_{D1}$	+10 VDC	18,19,- 20,21,- 22,23,- 24,25	$V_{D3}$	+10 VDC
8,9	$V_{D2}$	+10 VDC			

Stresses in excess of the absolute ratings may cause permanent damage. Functional operation is not implied under these conditions. Exposure to absolute ratings for extended periods of time may adversely affect reliability.

Operating Temperature: - 30 to + 85 °C

Storage Temperature: - 55 to +100 °C

PERFORMANCE DATA

Figure 2: ACPR @  $P_{OUT} = 35$  dBm

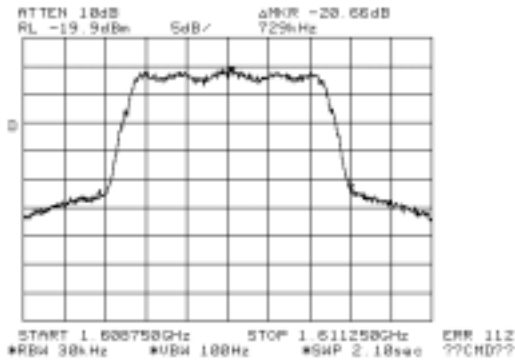


Figure 3: ACPR @  $P_{OUT} = 35$  dBm

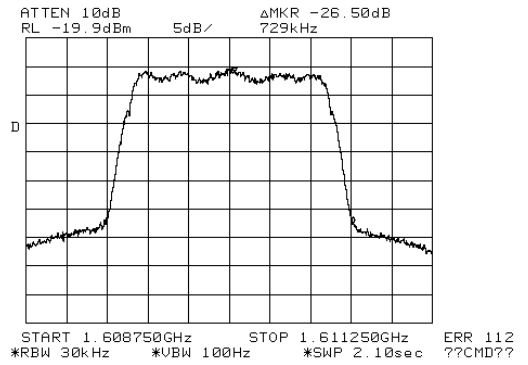
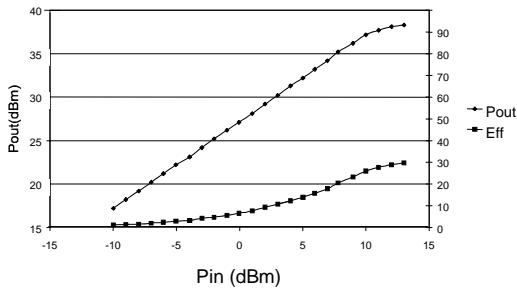
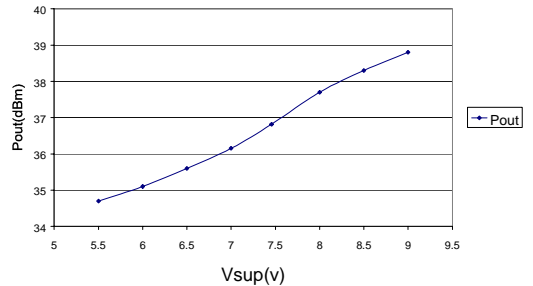


Figure 4:  $P_{OUT}$  & Eff vs  $P_{IN}$



\*  $P_{OUT}$  with CDMA Modulation

Figure 5:  $P_{OUT}$  vs Supply Voltage



$P_{IN} = 10$  dBm, with CDMA Modulation

Figure 6: S11 Forward Reflection Impedance

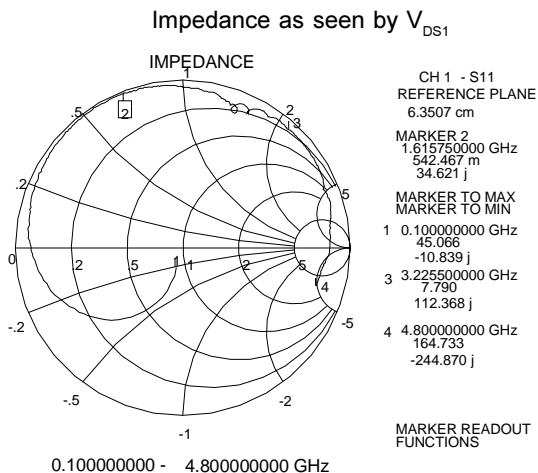


Figure 7: S11 Forward Reflection Impedance

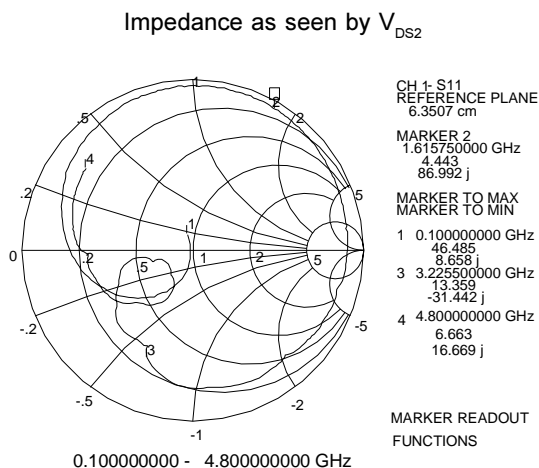


Figure 8: S11 Forward Reflection Impedance

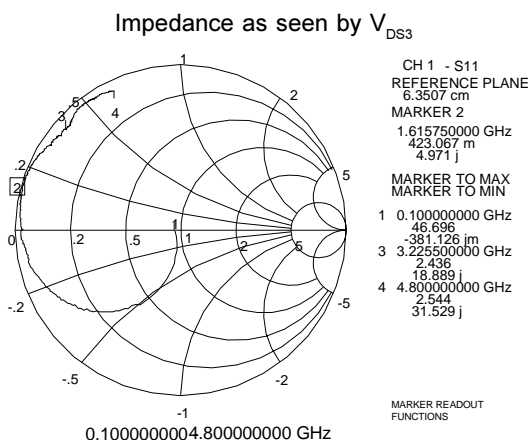
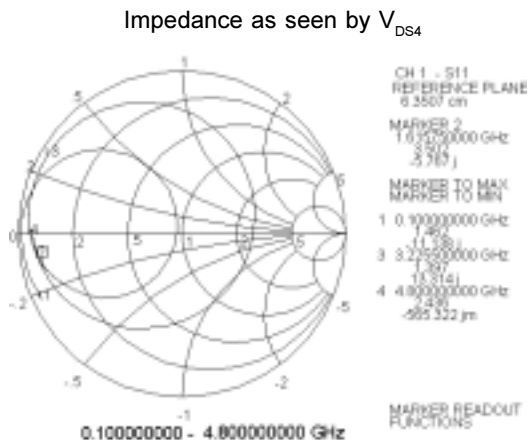


Figure 9: S11 Forward Reflection Impedance



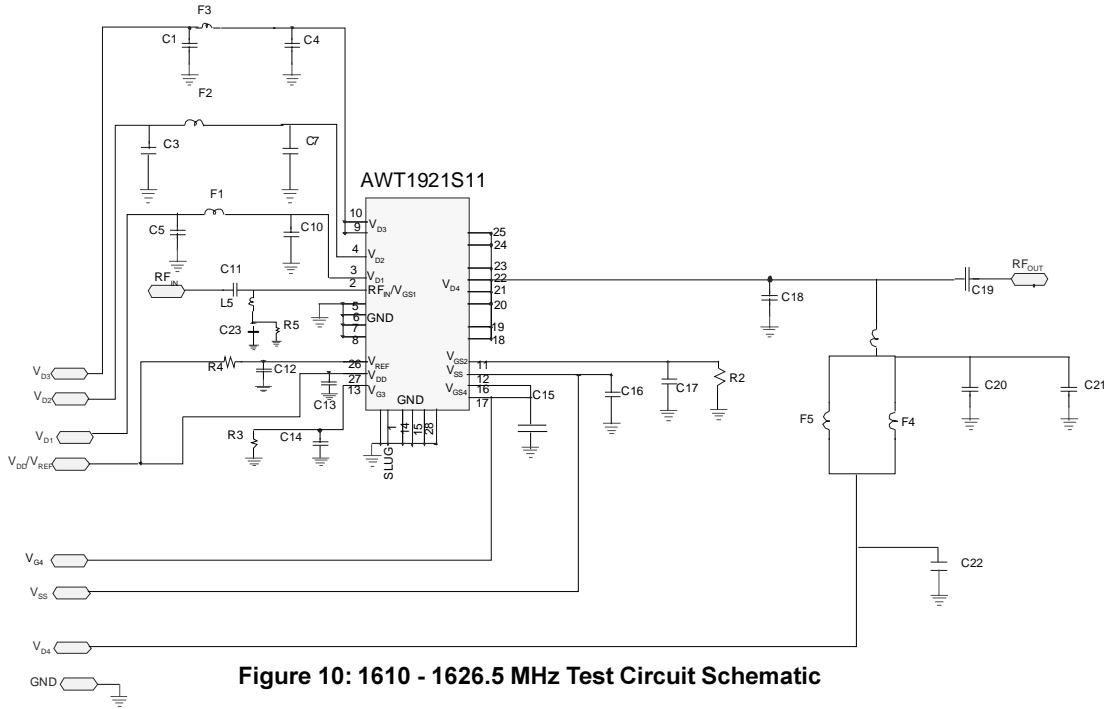


Figure 10: 1610 - 1626.5 MHz Test Circuit Schematic

Table 4: Pin Designations

DESIGNATION	VALUE
C1,C3,C5,C22	2.2 F
C2,C7,C9,C24	Not Used
C4	15 pF
C6, C10	10 pF
C11,C19	27 pF
C12,C13,C20,C21	33 pF
C14,C16,C17,C23	0.01 uF
C15	22 pF
C18	4.7 pF
F1,F2,F3,F4,F5	Feritte
L1,L3	Shim
L2	2.7 nH
L4	8 nH
L5	47 nH
R2, R5	5600
R3	1500
R4	2200

**Procedure for Amplifier Operation and Test**

- 1) Slug must be thermally and electrically connected to obtain rated performance.
- 2) The  $V_{SS}$  voltage should be applied first to the amplifier prior to  $V_{D1}$ ,  $V_{D2}$ ,  $V_{D3}$ , or  $V_{D4}$  voltages.
- 3)  $V_{GS1}$ ,  $V_{GS2}$ ,  $V_{GS3}$ ,  $V_{GS4}$  may be used as monitor points to verify that the bias circuit is working properly. These pins should measure as negative voltage potential, after  $V_{SS}$  is applied.
- 4) The Bias Pins  $V_{DD}$  and  $V_{REF}$  may be applied with no  $V_{SS}$  voltage present.
- 5) Always follow ESD precautions when handling these devices.

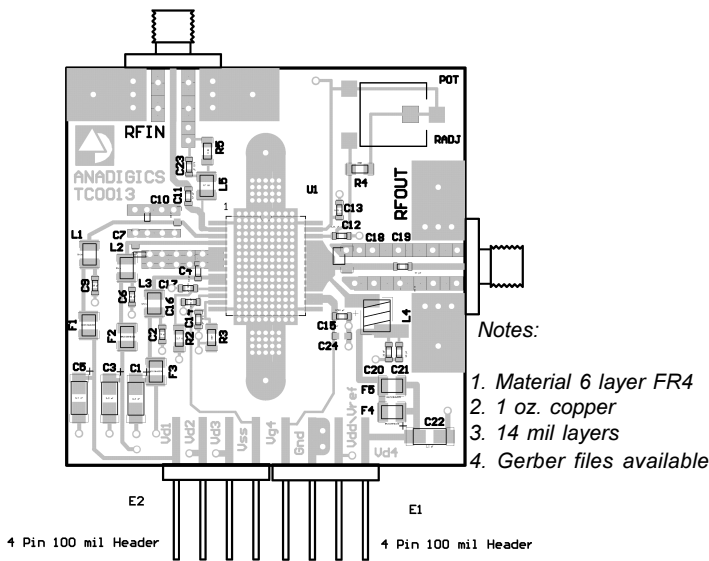
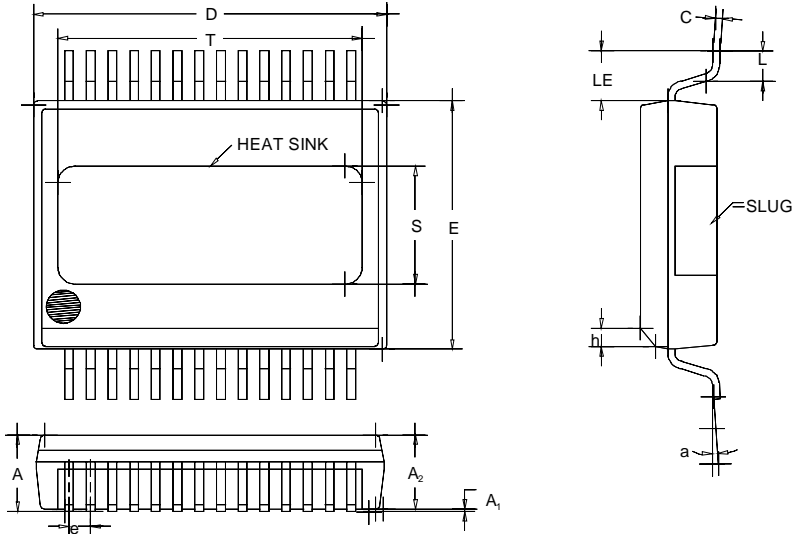


Figure 11: 1610 - 1626.5 MHz Test Circuit Layout

Table 5: Parts List Table

DESIGNATION	VALUE	MANUFACTURE	MANUFACTURE PART #	WEB ADDRESS
C1,C3,C5,C22	2.2 $\mu$ F	Panasonic	ECS-H1AY225R	<a href="http://www.panasonic.com">www.panasonic.com</a>
C2,C7,C9,C24	Not Used			
C4	15 pF	Murata	GRM36COG150J50	<a href="http://www.murata.com">www.murata.com</a>
C6,C10	10 pF	Murata	GRM36COG100J50	
C11,C19	27 pF	Murata	GRM36COG270J50	<a href="http://www.murata.com">www.murata.com</a>
C12,C13,C20,C21	33 pF	Murata	GRM36COG330J50	<a href="http://www.murata.com">www.murata.com</a>
C14,C16,C17, C23	0.01 uF	Murata	GRM36X7R103K16	<a href="http://www.murata.com">www.murata.com</a>
C15	22 pF	Murata	GRM36COG220J50	<a href="http://www.murata.com">www.murata.com</a>
C18	4.7 pF	American Technical Ceramics	ATC100A4R7CW150X	<a href="http://www.atc-cap.com">www.atc-cap.com</a>
F1,F2,F3,F4,F5	Ferrite 47 $\Omega$ @ 100 MHz, 1A Rating	Taiyo Yuden	BK2125HS470	<a href="http://www.t-yuden.com">www.t-yuden.com</a>
L1, L3	Shim			
L2	2.7 nH	Toko	LL2012-F2N7S	<a href="http://www.tokoam.com">www.tokoam.com</a>
L4	8 nH	Coilcraft	A03T	<a href="http://www.coilcraft.com">www.coilcraft.com</a>
L5	47 nH	Coilcraft	0805CS470XMBC	<a href="http://www.coilcraft.com">www.coilcraft.com</a>
R2,R5	5600 $\Omega$	Panasonic	ERJ-36SYJ562V	<a href="http://www.panasonic.com">www.panasonic.com</a>
R3	1500 $\Omega$	Panasonic	ERJ-36SYJ302V	<a href="http://www.panasonic.com">www.panasonic.com</a>
R4	2200 $\Omega$	Panasonic	ERJ-36SYJ512V	<a href="http://www.panasonic.com">www.panasonic.com</a>



Notes:

1. Controlling dimensions : inches
2. Dimension "d" does not include mold flash, protrusions or gate burrs. Mold flash, protrusions and gate burrs shall not exceed 0.006 (0.16mm)
3. Dimension "e" does not include inter-lead or protrusions. Inter-lead flash and protrusions shall not exceed 0.010 (0.25mm) per side.
5. Maximum lead twist/skew to be 0.002 (0.05mm)
6. Mold flash shall not extend more than 0.010 (0.25mm) on any edge of heat slug

Figure 12: Package Outline Drawing

SYMBOL	INCHES		MILLIMETERS		NOTE
	MIN	MAX	MIN	MAX	
A	0.087	0.093	2.21	2.36	
A1	0.000	0.004	0.00	0.10	
A2	0.087	0.089	2.21	2.25	
B	0.008	0.012	0.36	0.46	
C	0.007	0.009	0.18	0.25	
D	0.400	0.408	10.16	10.36	2
E	0.292	0.296	7.42	7.52	2
e	0.025	BSC	0.64	BSC	4
H	0.410	0.418	10.41	40.62	
h	0.018	0.024	0.48	0.61	
L	0.034	0.038	0.86	0.97	
LE	0.84		1.37		
a	0	8	0	8	
S	0.139	0.141	3.54	3.55	5
T	0.349	0.351	8.86	8.92	5

NOTES

AWT1921

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## ORDERING INFORMATION

ORDER NUMBER	PACKAGE DESCRIPTION	COMPONENT PACKAGING
AWT1921S11	S11	28 Pin Body with Heat Slug

**ANADIGICS, Inc.**

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